

CSCI 6461 – Computer Systems Architecture

Assignment 1

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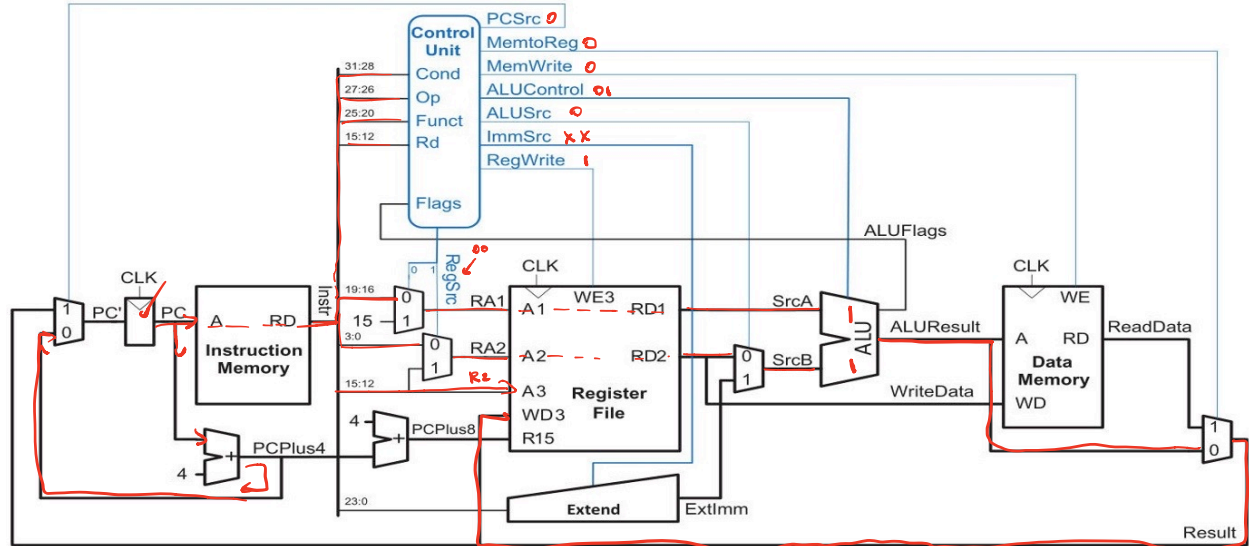
data - processing instruction

1. SUB R2, R4, R5

destination

1st source

2nd source

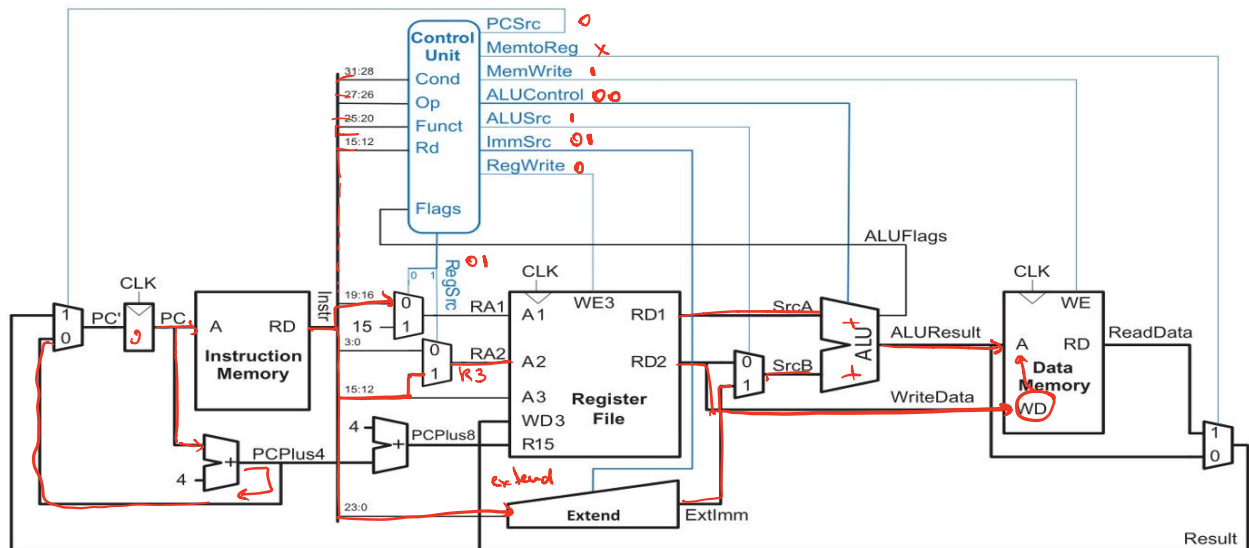


memory instruction

4. STR R3, [R4, #16]

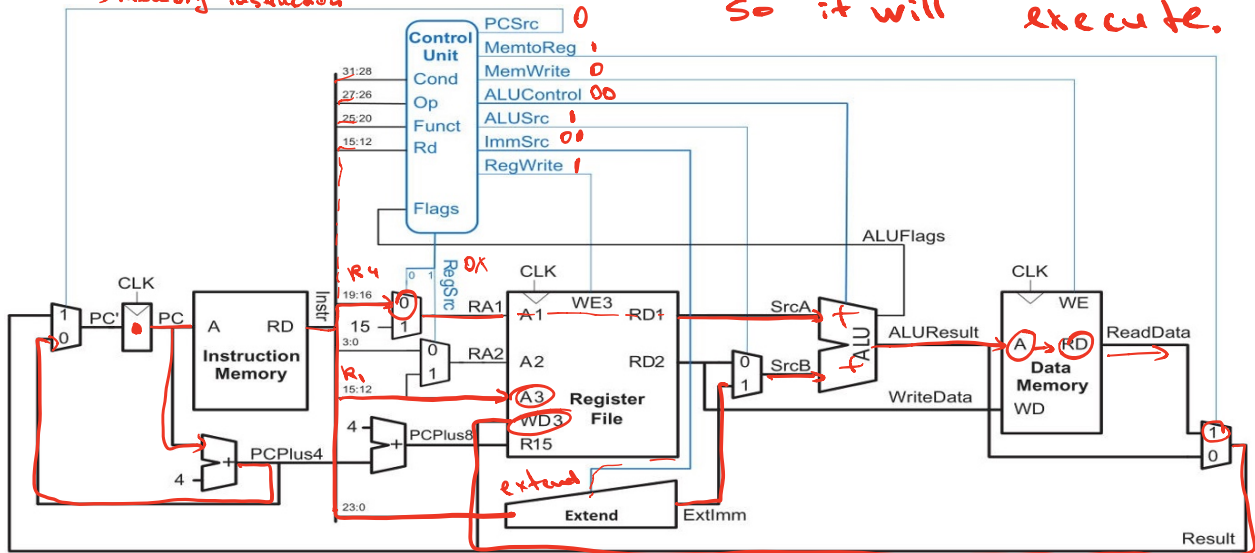
base

immediate

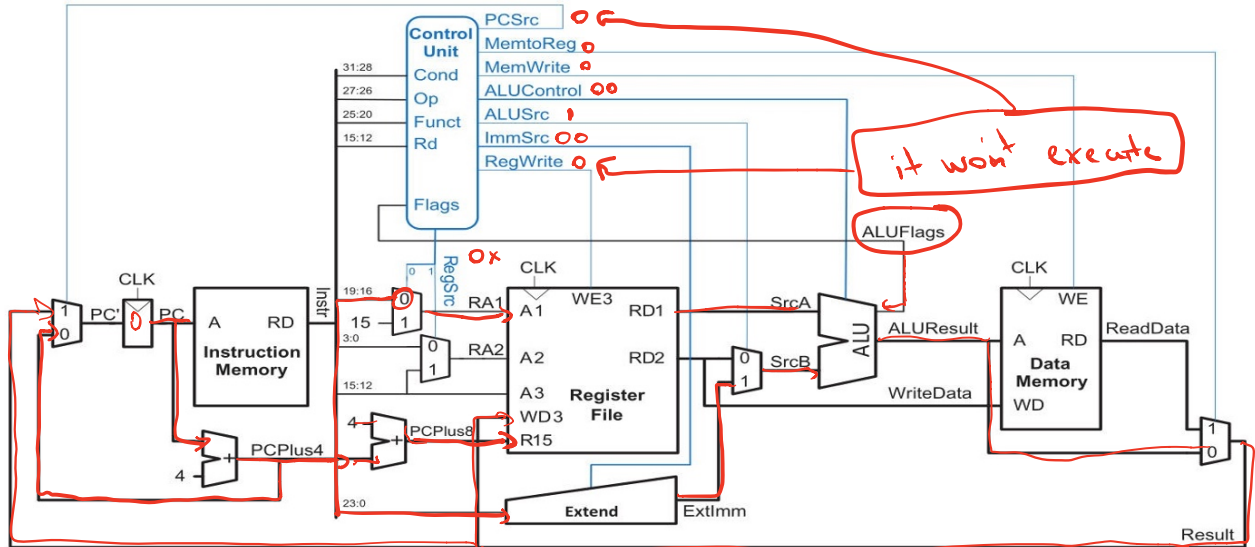


Equal requires Z flag to be 1
 3. LDREQ R1, [R4, #4] with NZCV = 0100
 ↳ memory instruction

EQ requires Z to be 1.
 So it will execute.



↳ requires Z flag to be set
 5. ADDEQ R15, R4, #16.
 ↳ writing R15 updates the PC.
 data-processing instruction.



2, **BNE** TARGET NZCV = 0010.
Not equal requires Z flag to be zero.
Branch

