COA - Tut - 08

Date
Page

(1) 6 segments
8 tasks.

Total time slots = 8 + 6 - 1 = 13

Space-time Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Segment 1	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8						
2		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8					
3			T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8				
4				T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8			
5					T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8		
6						T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	

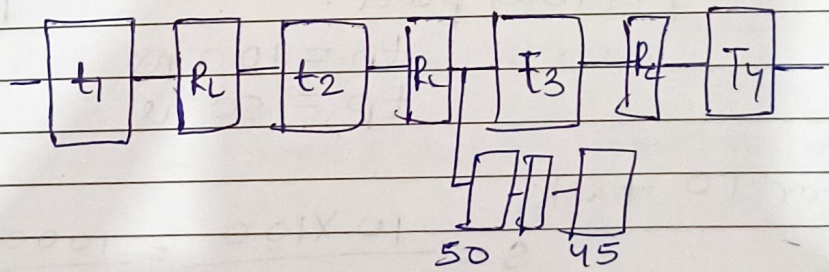
→ clock cycles

(2) $t_1 = 50$ ns $t_2 = 30$ ns, $T_3 = 95$ ns
$t_4 = 45$ ns. $T_r = 5$ ns

(i) Time $= (100 + 4 - 1) \times (T_{min} + T_r)$
$= 103\ T_{min} + T_r$
$= 103 \times (95 + 5)$
$= 10300$ ns

T_{min} = max time in all given = 95 ns

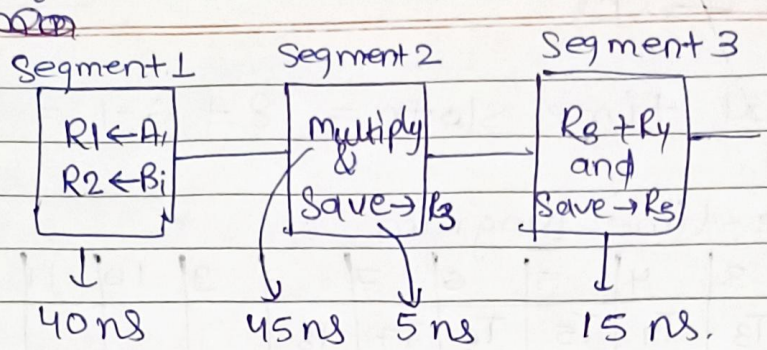
(ii) To convert it into 1/2 of 10300 ns



Now Time $= (100 + (5-1)) \times (50 + 5)$
104×55
$= 5720$ approx.

③

(i)



(i) T_{min} = maximum Time slot in all segment.

$= 45 + 5 = 50$ ns.

(ii) Suppose R3 and R4 Removed.

without pipeline -

Time $= 40\,ns + 45\,ns + 15\,ns = 100\,ns.$

(iii) Speed up factor ⇒

$$S = \frac{n\,t_n}{(n+k-1)\,t_p}$$

t_n ← Min Time without pipelining

t_p ← minTime with pipelining.

from previous part.

$t_n = 100$ ns

$t_p = 50$ ns

For 10 task,

$$S = \frac{10 \times 100}{(10+3-1)50} = \frac{1000}{12 \times 50} = \frac{1000}{600} = \boxed{1.67}$$

For 100 task

$$S = \frac{100 \times 100}{(100+3-1)\,50} = \frac{10000}{102 \times 50} = \boxed{1.96}$$

Date
Page

(iv) maximum speedup ratio

$$= \frac{t_n}{t_p} = \frac{100}{50} = 2$$

(4) Total operations = 250 billion

$= 250 \times 10^9$ operations.

Speed = 100 megaflops / second.

$= 100 \times 10^6$ seconds

$$\text{Time} = \frac{250 \times 10^9}{100 \times 10^6} = 2500 \text{ sec.}$$

$= 41.6$ minutes,

(5)

(i) $40 \times 40 = 1600$ inner products

(ii) $40 \times 40 \times 40 = 64{,}000$ operations.

(6) Time taken

$$= \frac{400}{4} \times 40 \text{ ns} = 4000 \text{ ns}$$

$= \boxed{4 \mu s}$

using single pipeline processor

$400 \times 10 \text{ ns} = 4000 \text{ ns} = \boxed{4 \mu s}$

Date
Page

Tut - 09

① 2 GB RAM = $2 \times 2^{10} \times 2^{10} \times 2^{10}$

Data bit = 32
$= 2^5$

~~$2^{31} = 2^{26}$ Address lines~~

~~64 bit = 8 byte~~

~~address = 8 bit~~

$= 2^{31}$ address lines
(address + data)

32 bit computer
d. = 4 byte.
So bits required to represent 4 byte

$= \frac{2^{31}}{2^2} = \boxed{2^{29}}$ address lines

~~② Address bits × Data bits~~
~~= 16 × 8 = 128 bits~~
~~data bytes = $\frac{128}{8}$ = 16 bytes~~

② 16 address bits
$= 2^{16}$ address and each of 8 bit
$= 2^{16} \times 8 = 2^{16} \times 2^3 = 2^{19}$ bit

in byte $= \frac{2^{19}}{8} = \frac{2^{19}}{2^3} = 2^{16}$ bytes data

$= 65,536$ bytes

Date
Page

(3) Rom = 2KB X 8
Memory = 16 KB X 8

No of Roms = $\frac{16}{2}$ = (8)

or

$\frac{16 \times 2^{10} \times 8 \times 8}{2 \times 2^{10} \times 8 \times 8}$ = (8)

(4) (a) disk capacity

= 8 X 512 X 64 X 1 KB

= $\frac{262,144}{1024}$ KB

= 256 MB

(b)

average rotational delay

= $\frac{1}{\frac{3600}{60}} \times \frac{1}{2} \times 60$ sec.

= $\frac{1}{120}$ sec = 8.33 ms

(c) tracks required for 5 MB file.

= memory stored in 1 track

= 64 KB.

tracks = $\frac{5 \times 1024 \text{ KB}}{64 \text{ KB}}$ = 80 tracks.

No of cylinders = $\frac{80}{8}$ = 10 cylinders.

surface

Date
Page

(d) Time required to transfer 5 MB file.

No of Sector use in read of 5 MB file.

$= 5 \times 1024$ KB / 1 KB $= 5120$ Sectors

There are two Approaches to find,

(i) Sequential access
(ii) Random Access.

(i) using sequential access approach,

No of tracks $= \frac{5120}{64} = 80$ tracks

Time read to first track is

Average seek	:	8 ms
Average rotational delay	:	8.33 ms
Read 64 sectors (1 track)	:	8 ms
Total	=	24.33 ms

8 ms because, it is sequential distribution So we suppose seek time (8 ms) is sufficient to read 64 sectors or 1 track.

~~(ii) using random access approach~~

Now for other tracks no need of Average seek, So

Date
Page

each track except first one.

Read time = 8.33 + 8 ms = 16.33 ms.

for all remaining Tracks

= 79 X 16.33

= 1,290 ms

Total time

= time of 1st track + time of all 79 track

= 24.33 + 1290

= 1314.33 ms

or

1.31 sec

(ii) using Random access,

time required for 1 sector =

average seek	:	8 ms
average Rotational delay	:	8.33 ms
Read 1 sector	:	0.125 ms
	total	16.455 ms

$\frac{8 \text{ ms}}{64}$

Total time

= total sectors X time of 1 sec

5120 X 16.45 ms

= 84,224 ms

= 84.22 sec

Date
Page

(e) data (burst) transfer rate,

in sequential access,

$$= \frac{5\ MB}{1.31\ s} = \boxed{3.8\ MB/s}$$

in Random access, $\frac{5 \times 1024\ KB}{84.22\ sec}$

$$= \boxed{60.7\ KB/s}$$

(5) we have 2500 sectors.

(i) using ~~random~~ sequential.

for 1st track or 500 sectors

1st track = 4 ms + 2 ms + 4 ms
= 10 ms

average Rotational delay
$= \frac{1 \times 60}{15000}$
$= \frac{4\ ms}{2}$
$= 2\ ms$

total $= \frac{2500}{500} = 5$ sectors

Remaining 4 sectors = 2 + 4 ms = 6 ms
= 4 × 6 = 24 ms

Total = 10 ms + 24 ms = 34 ms
= 0.034 sec

(ii) using Random access approach,

for time of 1 sector

$$= 4ms + 2ms + \frac{4ms}{500}$$

$$= 4ms + 2ms + 0.008ms$$

$$= 6.008 ms.$$

for total 2500 sectors

$$2500 \times 6.008 \ ms = 15,020 \ ms$$

$$= \underline{\underline{15.02 \ sec}}$$

Tut -10

(1)

(a) 2048 bytes.

$$= \frac{2048 \times 8 \text{ bits}}{128 \times 8}$$

$$= 16 \text{ RAM chips}$$

(b) address lines → ?

2048 bytes

$= 2048 \times 8$ bits.

let data = 8 bit or 1 byte.

$$\text{total address} = \frac{2048 \times 8}{8} = 2048 \text{ add.}$$

for 2048 we want

2^{11}, 11 address lines.

for 16 RAM chips, we need 4 lines.

So common lines = 11 − 4 = 7

(c) Since, 7 lines are common to each chip, we need ~~8 lines for 16~~.

$\log 7 = \boxed{3}$ lines.

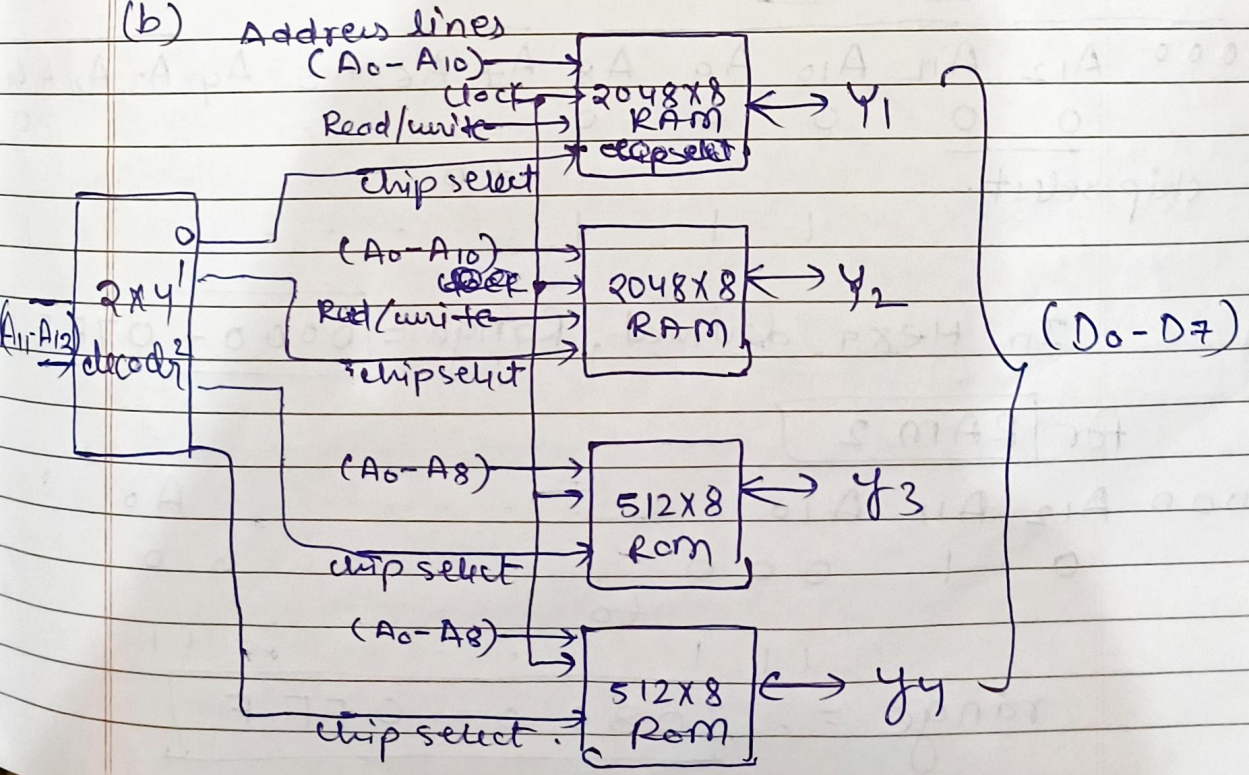
and for 16 chips we will need $\boxed{4 \times 16}$ decoder

(2)

(a) Ram chips $= \dfrac{4 \times 1024 \times 8 \text{ bit}}{2048 \times 8} = \underline{2 \text{ RAM}}$

Rom chips $= \dfrac{1 \times 1024 \times 8}{512 \times 8} = \underline{2 \text{ Rom}}$

(b)



(c) Address Map Ranges,

For $\boxed{\text{RAM 1}}$

	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
000 chip select.	0	0	0	0	0	.	.	.	.				0
						to							
	1	1	1	.	.	.	.	.	.				1

In Hexa decimal, Range = $\boxed{0000 - 07FF}$

for $\boxed{\text{RAM 2}}$

	A_{12}	A_{11}	A_{10}	. . . .	A_0
000	0	1	000	 00	0
			to		
	1	1	1	. . . .	11

range = $\boxed{0800 - 0FFF}$

Date _____
Page _____

For $\boxed{\text{ROM1}}$

There can many ranges.

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	X	X	0	0	. . .	. . .				0	0
							to					
				1	1	. . .	. . .				1	1

There are two dont care.
So 4 possibilities

A_{12}	A_{11}	A_{10}	A_9									
1	0	0	0	0	0	0	. . .	0	0	to	1	1
1	0	0	1									
1	0	1	0									
1	0	1	1									

~~Ranges~~ = 1000 - 1FFF
1200 - 13FF

0 0	→	1000 - 11FF
0 1	→	1200 - 13FF
1 0	→	1400 - 15FF
1 1	→	1600 - 17FF

For $\boxed{\text{ROM2}}$

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	. . .	A_0
1	1	X	X	0/1	0/1	. . .	0/1

0 0	→	1800 - 19FF
0 1	→	1A00 - 1BFF
1 0	→	1C00 - 1DFF
1 1	→	1D00 - 1FFF

Date
Page

(3) average access time $= (0.8 \times 5) + (0.2 \times 50)$
$= 4 + 10$
$= 14$ ns

(4) 1000 memory reference..

In L1 → 40 miss means
960 hit

hit ratio in L1 $= 0.96 \left(\frac{960}{1000}\right)$

hit ratio in L2 $= \frac{990}{1000} = 0.99$

using formula

time $= 0.96 \times 1 + 0.04 \times (0.99 \times 15 + 0.01 \times 215)$

This answer can be wrong so if you know correct one, than try to answer & contact me
Aniruddha

why we are taking 215 ?

→ given L2 penalty = 200 clock cycle

miss = penalty + hit
$= 200 + 15 = 215$ clock cycle

time $= 0.96 + 0.04 \times (14.85 + 2.15)$
$= 0.96 + 0.04 \times 17$
$= 0.96 + 0.68$
$= 1.64$ clock cycles.

time $= \frac{1.64}{10^9 \text{ Hz}} = 1.64$ ns

1 GHz

Date
Page

(5) fetch operation is type of read operations

time ~~to~~ in 1000 fetch operations

$= 1000 \times (0.8 \times 2 + 0.2 \times 6)$
$= 1000 \times 2.8$
$= 2800$ ns.

time in 600 read operations
$= 600 \times (0.8 \times 2 + 0.2 \times 6)$
$= 600 \times 2.8$
$= 1680$ ns.

time in 400 write operations
$= 400 \times (0.8 \times 4 + 0.2 \times 10)$
$= 400 \times 5.2$
$= 2080$ ns.

Average memory access time.

$$= \frac{\text{Total time}}{\text{Total instruction}}$$

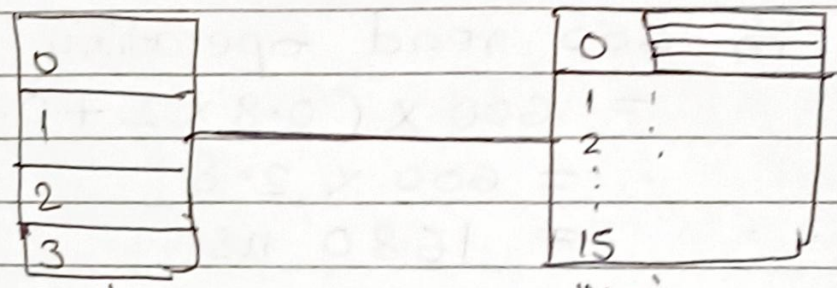
$$= \frac{2800 + 1680 + 2080}{1000 + 600 + 400} = \frac{6560 \text{ ns}}{2000}$$

$$= \boxed{3.28 \text{ ns}}$$

Tut - 11

① Total 6 bit means $2^6 = 64$ ~~bit~~ address memory bit

word bit = 2 $\quad 2^2 = 4$ words.



Cache = 4 Blocks.

Main memory $64/4 = 16$ ~~address~~ Blocks.

Tag	Block	word	
01	01	00	miss (Block 5 copy into Block 1)
01	01	01	hit
01	10	10	miss (Block 6 copy into Bl. 2)
01	10	11	hit

$$\text{hit ratio} = \frac{2}{2+2} = \boxed{0.5}$$

② Main memory → 32 bit

Question is wrong (it is Direct mapping not fully associative)

Date
Page

In 1 Block = 32 words or

word bit = 5

No of Blocks in cache = $\frac{16K}{32}$

= 512 Blocks

So Block bit = 9

Remaining is Tag bit = 32 - (9 + 5)

= 18.

Tag bit	Block bits	word bits
18	9	5

3

Tag bits = 4

word bits = 4

means 1 Block have 2^4 words

= 16 words.

No of Blocks in cache = $\frac{512}{16}$ = 32

There are 32 total blocks in cache.

it is 8 way set associative.

So $\frac{32}{8}$ = 4 sets = 2^2 (2 bit)

Tag bits = 4

Set bits = 2

Blocks in main memory

2^6 = 64 Blocks.

Maximum Block can reside = 32

Date
Page

(4) Total word length = 20 bit

1 Block have 128 words.

means $2^7 \Rightarrow 7$ bits for word

$20 - (9+7) = 4$ bit

Set bit = 4

So there are $\boxed{16 \text{ sets}}$

and cache is 4-way ~~so~~ 1 set = 4 Blocks

~~to 4 sets have~~

(5)

Memory address = 16 bit

1 Block have 2^6 words (64 B)

word bit = 6

No of Blocks = $\frac{2 \text{ KB}}{64} = 32$

Block bits = 5

Tag bits = $16 - (6+5) = 5$

128 - miss (Block 2 copy in block 2)
144 - hit
2176 - miss (Block 34 replace in block 2)
128 - miss (Block 2 replace in block 2)
2180 - miss (Block 34 replace " 2)
128 - miss (" ")
2176 - miss (" ")

hit ratio = $1/7 = \boxed{0.14}$

Date
Page

(6) using fully associative,

Tag bits = 10
word bits = 6

128 - miss (Block 2 copy in somewhere)
144 - hit
2176 - miss (Block 34 copy) in somewhere
128 - hit
2180 - hit
128 - hit
2176 - hit

hit ratio = 5/7 = $\boxed{0.71}$

using 4-way set associative.

word bits = 6

No of Blocks = $\frac{2KB}{64}$ = 32

No of sets = $\frac{32}{4}$ = 8 sets

Set bits = 3
Tag bits = 16 - (6 + 3) = 7

128 - miss (Block 2 copy in Block 2)
144 - hit
2176 - miss (Block 34 copy in Block 2)
128 - hit
2180 - hit
128 - hit
2176 - hit

hit ratio = 5/7 = $\boxed{0.71}$

Date
Page

Tut - 12

① Can't determined.

② 1024 words = 10 bits

$2^7 = 128$

Logical address bits = 7 + 10 = 17 bits

physical address bits = 5 + 10 = 15 bits

$2^5 = 32$

③

Segment bits	page bits	word bit
128	32	4K
2^7 (7)	2^5 (5)	2^{12} (12)

logical address :

0100100	01111	0001111111
36	15	255

= 01001000111100001111111

④ FIFO

2 1 2 0 3 0 4 5 3

2	2	2	3	3	3			
	1	1	1	4	4			
		0	0	0	5			
PF	PF	NPF	PF	PF	NPF	PF	PF	NPF

hit ratio $= \frac{3}{9} = \boxed{0.33}$

Date
Page

(5) using LRU

2	1	2	0	3	0	4	5	3
2	2		2	2		4	4	4
	1		1	3		3	5	5
			0	0		0	0	3
		NPF			NPF			

hit ratio $= \frac{2}{9} = \boxed{0.22}$