

I2C

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Caracterísiticas Hardware Signal and Dat

I2C Mode I2C Duty Transacción

Transacción STM

Config CC

#### .. . .. . . . . . .

#### Protocolo I2C

Inter-Integrated Circuit communication

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Universidad Nacional de Colombia

2023



# Agenda

I2C

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12C

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Hardware

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I2C Duty

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## Breve explicación

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I2C (Inter-Integrated Circuit) is an on-board communication protocol, which is ideal for short distances and low bandwidth. It has a master-slave architecture in which all slaves are connected to the master via two wires: the serial data wire (SDA) and the serial clock wire (SCL). I2C is typically used for attaching lower-speed peripherals such as sensors to processors and microcontrollers over short distances within an integrated circuit.

Tomado de: I2C-vs-SPI



#### Caracterísitcas básicas

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Caracterísiticas

	I2C
Pin drive	Open drain
Signal lines	2
Max speed	400 kbps in fast mode (3.4 Mbps is possible with high-speed mode)
No. of peripherals	112 with 7-bit addressing
Multi-master	Yes
Flow control	Yes

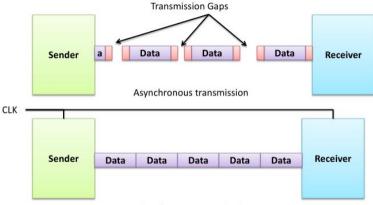


### Comunicación Sincrona

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Caracterísiticas





## Conexión Hardware

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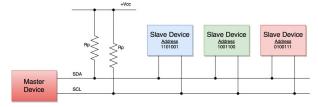
I2C Mod

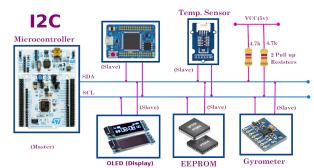
I2C Duty

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# Trama de datos del I2C (1)

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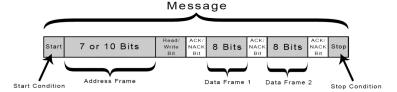
Start Stop

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Contig CCI





# Trama de datos del I2C (2)

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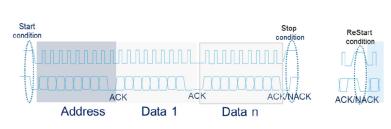
12C Duty

Transacc

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I<sup>2</sup>C protocol



## Condición Start y Stop

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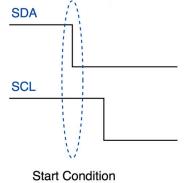
Start Stop I2C Mode

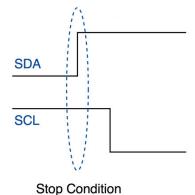
I2C Mode I2C Duty

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### **I2C** Mode

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Caracterísiticas Hardware Signal and Dat

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Es la velocidad a la que la interface de I2C va a funcionar. Existen 4 modos definidos en la especificación de I2C:

- Standart mode (Sm): 100KHz (Clock)
- Fast mode (Fm): 400KHz (Clock)
- Fast mode plus (Fm +): 1MHz (Clock)
- High-Speed mode : 3.4MHz (Clock)



## **I2C Duty**

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I2C Duty

Especifica la relación del tiempo en bajo ( $T_{LOW}$ ) y tiempo en alto  $(T_{HIGH})$ , de la señal de reloj (SCL) Se tienen especificados dos posibles valores:

- I2C Duty cicle 2:1
- I2C Duty cicle 16:9



## Transacción I2C

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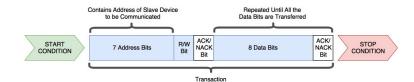
I2C Mode

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## Transacción I2C - Maestro a Esclavo

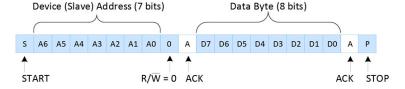
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Transacción

Master Controls SDA Line

Slave Controls SDA Line





## Transacción I2C - Esclavo a Maestro

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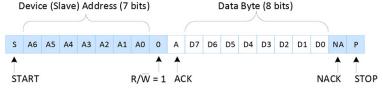
Start Stop I2C Mode

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Transacción STM

STM Config CCF Master Controls SDA Line

Slave Controls SDA Line





## Implementación en STM

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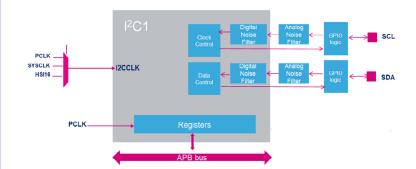
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## Configuración del Reloj

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La siguiente página presenta una excelente explicación de las consideraciones necesarias para configurar adecuadamente los registros que generan la señal de reloj del protocolo I2C:

**I2C** clock settings with explanmations