- ***mpc_imsgn_e***

  SOLUTION:

  - Signal ***mpc_imsgn_e*** is computed in an OR gate. Let's focus on the first input (for non-atomic load instructions), as the second input is for atomic load instructions.
  - Bit 15 of the Instruction Register (mpc_ir_e) is used, as this is the MSB of the Immediate (i.e. the sign bit) that we have to extend. Note that for the ***lw*** instructions we are analyzing here, bit 31 of IR is 1.

- ***mpc_dcba_w***

  SOLUTION:

  - This signal is registered from the E-Stage (*m14k_mpc_dec* module), signal ***pbus_type_e***[2:0]. This signal is encoded as: *0-nil, 1-load, 2-store, 3-pref, 4-sync, 5-ICacheOp, 6-DCacheOp*. Thus, when (***pbus_type_e*** *== 3'h1*), ***mpc_dcba_w***=1, and the data from the *lw* is selected.