• EXPLANATION:

Detailed explanation: All changes related to the new instruction are tagged with comment: // LWPC in the soft-core. We must perform the following actions:

• Inhibit "Reserved Instruction Exception":

Comment:

```
assign maj_ri_e = ... (mpc_ir_e[31:26] == 6'047) \parallel
```

- New signal:
 - *Iwpc_instr*: Set to 1 when Iwpc found:

```
assign\ lwpc\_instr = (mpc\_ir\_e[31:26] == 6'o47);
```

- Incorporate new functionality:
 - b. We must insert the new operands as an input to the *lw* adder. **aop_e** and **dva_offset_e** are the inputs to the adder that calculates the Effective Address:
 - c. **aop_e**: Incorporate the PC as an input. The PC is already available at E-Stage in signal **iva_e**.

```
assign aop_e[31:0] = <a href="mailto:line">lwpc_instr ? iva_e : (icc_pcrel_e ? (iva_e & ~{30'b0, {2{icc_pcrel_e}}}) : edp_abus_e); // LWPC</a>
```

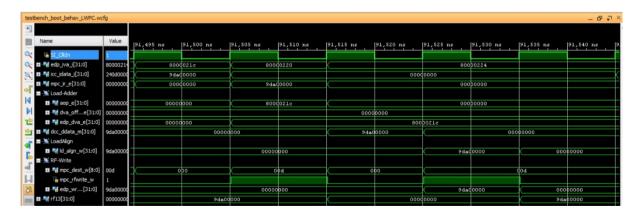
d. **dva_offset_e**: Incorporate the SignExt(Imm<<2) as an input.

```
assign dva_offset_e[31:0] = lwpc_instr ? {
{11{mpc_ir_e[18]}}, mpc_ir_e[18:0], 2'b0} :
{32{mpc_subtract_e}} ^ bbus_imm_e; // LWPC
```

We must select Rs as Destination Register:

```
assign dest_e [5:0] = lwpc_instr ? { 1'b0, mpc_ir_e[25:21] } : ((special_e | spec2_e | mpc_cnvt_e | rwpgpr_e | dest_cnvt_dsp_e | lx_e) ? { rwpgpr_e & ~rdpgpr_e, pdest_e } : ((lnk31_e) ? 6'h1f : { 1'b0, src_b_e[4:0] })); // LWPC
```

• EXAMPLE - SIMULATION:



Observe that in the fifth cycle rf13 is written to 0x9da00000, which corresponds to the opcode of the instruction stored at PC=0x8000021c.

• EXECUTION ON THE BOARD:

When the program is downloaded on the board, you should see on the 7-seg displays:

7-seg displays=\$t5, which in our example is 0x9da00000

Then, when you debug the program following the steps stated in the document, you should observe the following:

```
X
 mips-mti-elf-gdb -q program.elf -x C:\Users\Dani\Desktop\Scripts\Ne...
                                                                                  bols from program.elf...done.
0x000000000 in ?? ()
The target is assumed to be little endian
semihosting is enabled
JTAG tap: mAUP.cpu tap/device found: 0x00000001 (mfg: 0x000 (<invalid>), part: 0x0000, ver: 0x0)
target halted in MIPS32 mode due to debug-request, pc: 0xbfc00000
Loading section .exception_vector, size 0x200 lma 0x80000000
oading section .text, size 0x34 lma 0x80000200
oading section .bootrom, size 0x1b0 lma 0xbfc00000
Start address 0xbfc00000, load size 996
ransfer rate: 30 KB/sec, 332 bytes/write.
Program received signal SIGINT, Interrupt.
0x80000228 in main () at main.c:23
                  MFP 7SEGEN = 0 \times 00;
(gdb) monitor reset halt

JTAG cap: mwaur.cpu cap/uevice found: 0x00000001 (mfg: 0x000 (<invalid>), part: 0x0000, ver: 0x0)

target balted in MIDS32 mode due to debug-request, pc: 0xbfc00000
    point 1 at 0x80000221c: file main.c, line 8.
3real
(gdb) c
Continuing.
Remote target] #1 stopped.
0x8000021c in main () at main.c:8
           asm volatile
(gdb)
                           v0
                                            a0
     00000000 00000000 00000000 80000250 00000000 00000002 80001000 00000000
          t0
                   t1
                           t2
                                    t3
R8
     00000000
                                                        0000000
                                                               00000000
          50
                           52
                                    s3
                                                             56
R16
     t9
                           k0
          t8
                                            gp
     00000000 00000000 00000000 00000000 80008250 8003fff0 00000000 9fc001a4
                           hi badvaddr
       status
                   10
                                         cause
             00000100 00000000 00000000 00000000 8000021c
(gd)) stepi
   000220
                         asm volatile
(gd)) i r
     zero at v0 v1 a0 a1 a2
00000000 00000000 00000000 80000250 00000000 00000000 80001000
                           t2
     9da00000
                                                        00000000 00000000
                   s1
                                   s3
          50
                           52
                                                            s6
R16
     t9
                           k0
          t8
                                            gp
                                                    sp
     00000000 00000000 00000000 00000000 80008250 8003fff0 00000000 9fc001a4
                   10
                           hi badvaddr
       status
                                         cause
     gdb)
```