- ***mpc_alufunc_e***.

  <u>SOLUTION</u>:

  - ***mpc_alufunc_e***, is computed within module *m14k_mpc*_dec. Note that, for special logic instructions (for which ***mpc_ir_e****[5]=1*):
    mpc_alufunc_e=***mpc_ir_e****[1:0]*.
    According to Table A.3 in document "MIPS Architecture For Programmers Volume II-A: The MIPS32 Instruction Set (MD00086)":
    - ***mpc_ir_e****[1:0]*=00 for an AND instruction.
    - ***mpc_ir_e****[1:0]*=01 for an OR instruction.
    - ***mpc_ir_e****[1:0]*=10 for an XOR instruction.
    - ***mpc_ir_e****[1:0]*=11 for an NOR instruction.

    which is perfectly coherent with multiplexer "_logic_out_e_31_0_" in Figure 14.
- ***mpc_sellogic_m***.

  <u>SOLUTION</u>:

  - ***mpc_sellogic_m*** is computed within module *m14k_mpc_ctl*. This signal is registered from the E-Stage through the Pipeline Registers (***ie_pipe_in***[`M14K_IE_SELLOG] → ***ie_pipe_out***[`M14K_IE_SELLOG]). It comes from signal ***sel_logic_e***, computed within module *m14k_mpc_dec*. This signal is 1 for special logic instructions (***mpc_ir_e***[5:2] == 4'b100_1), and 0 for arithmetic instructions, which is perfectly coherent with multiplexer "_edp_alu_m_31_0_" in Figure 14.