- ***mpc_dest_w***

  SOLUTION:

  - This signal is assigned through the Control Pipeline Registers in module *m14k_mpc_ctl*, from the E-Stage, signal ***dest_e***.
  - Signal ***dest_e*** is computed in a similar way to the simple pipelined processor from [2], in module *m14k_mpc_dec*, at line 1458, as follows:

    ```
    assign dest_e [5:0] = (special_e | spec2_e | mpc_cnvt_e | rwpgpr_e |
    dest_cnvt_dsp_e | lx_e) ? { rwpgpr_e & ~rdpgpr_e, pdest_e } : ((lnk31_e) ?
    6'h1f : { 1'b0, src_b_e[4:0] });
    ```

    - When the instruction being executed is any of: ***special_e***, ***spec2_e***, ***mpc_cnvt_e***, ***rwpgpr_e***, ***dest_cnvt_dsp_e***, ***lx_e***, then the destination register is assigned from signal ***pdest_e***, which is obtained in module *m14k_mpc_dec*, line 1451, as follows:

      ```
      assign pdest_e [4:0] = (spec2_e && (mpc_ir_e[5:4] == 2'b01)) ?
      edp_udi_wrreg_e[4:0] : mpc_ir_e[15:11];
      ```

      For example, an *add* instruction, which has a *special* opcode (signal ***special_e***=1), matches this case.
    - When the instruction being executed is a jump&link instruction, the destination register is $ra (register 31).
    - Finally, in any other case (such as a lw instruction), the destination register is assigned from signal ***src_b_e***, which is obtained in module *m14k_mpc_dec*, line 1445, as follows:

      ```
      assign src_b_e [5:0] = { rdpgpr_e, mpc_ir_e[20:16]};
      ```

- ***mpc_rfwrite_w***.

  SOLUTION:

  - ***mpc_rfwrite_w*** depends on ***pvd_w***, which is registered from the E-Stage through the Pipeline Registers. ***pvd_w*** depends on ***vd_e***.
    At the E-Stage, in the Decoding Module (*m14k_mpc_dec*), signal ***vd_e*** is computed. This signal is set to 1 for all instructions that will write to the RF at the W-Stage.
  - ***mpc_rfwrite_w*** also depends on ***mpc_exc_w***, which is 1 when an exception is triggered at the W-Stage. In case there is an exception, the RF write is inhibited.
  - ***mpc_rfwrite_w*** also depends on ***mpc_run_w***, which is 1 when an instruction is executing in the W-Stage. In case W-Stage is not executing, RF write is inhibited.