LRU:

Examining set *a* for one iteration (a_1 a_2 a_1 a_3 a_2 a_3): The first two accesses miss. After these two accesses, the LRU block is a_1. The third access hits, and sets a_2 as the LRU block. The fourth access misses: a_3 replaces a_2. The fifth access misses: a_2 replaces a_1. The sixth access hits. This results in 4 misses and 2 hits per iteration and per block. Thus, 4*4*2 = 32 misses.

EXPERIMENTAL STUDY:

- D$ Accesses: 48
- D$ Misses: 32

FIFO:

ANALITICAL STUDY: Examining set *a* for one iteration (a_1 a_2 a_1 a_3 a_2 a_3): The first two accesses miss. The third access hits. The fourth access misses: a_3 replaces a_1 (which was inserted before a_2). The fifth access hits. The sixth access hits. This results in 3 misses and 3 hits per iteration and per block. Thus, 3*4*2 = 24 misses.

EXPERIMENTAL STUDY:

- D$ Accesses: 48
- D$ Misses: 24