For computing the miss penalty of a D$ miss, we analyze the simulation shown in Figure 7 and Figure 5 of Lab22-B:

- In the cycle when the miss is detected, the processor is still running.
- After the miss detection, the processor must pay **1 cycle** for initializing the transfer (i.e. notifying the miss to the Bus, generate the pulses for the request, arbitrate requests, etc.).
- Then, **1 cycle** is needed for sending the address through the Bus to Main Memory (***HADDR***=0x00001f30).
- Then, **1 cycle** in needed for sending the first requested word (which is the *critical word*) from Main Memory to the CPU.
- Then, **1 cycle** in needed for bypassing the critical word to the *lw* instruction, which is waiting at the A-Stage.
- In the next cycle, the processor starts execution again.

Miss Penalty = **4 cycles**