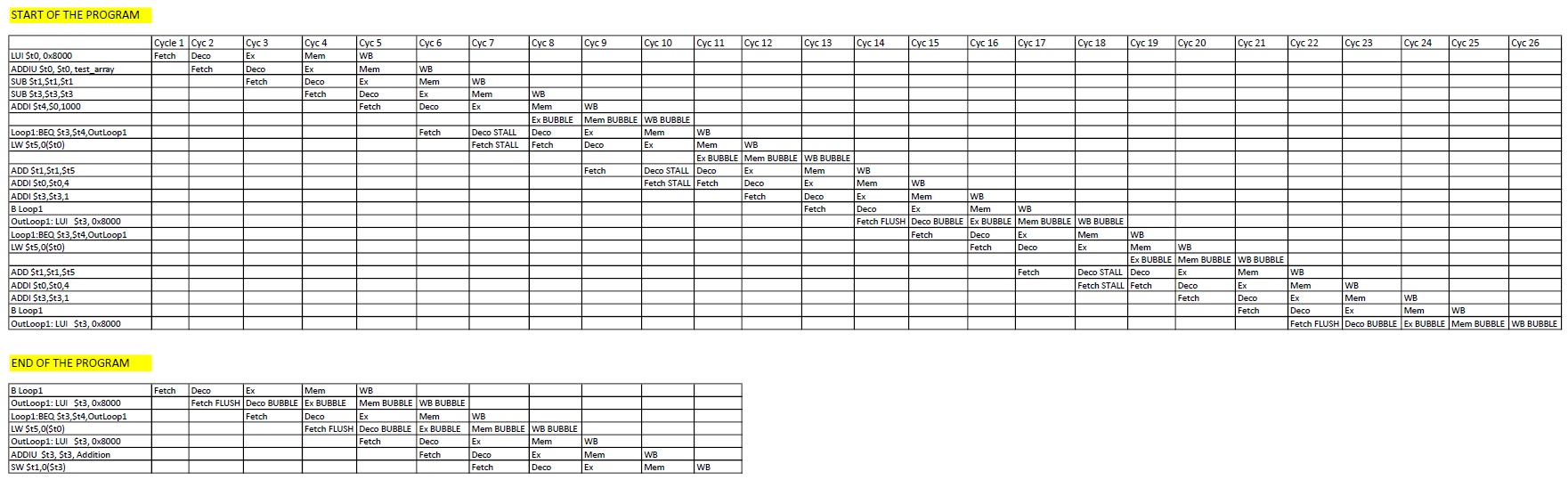
# Analytical study in the pipelined processor from [2]

**Timing diagram:**



**Detailed analysis:**

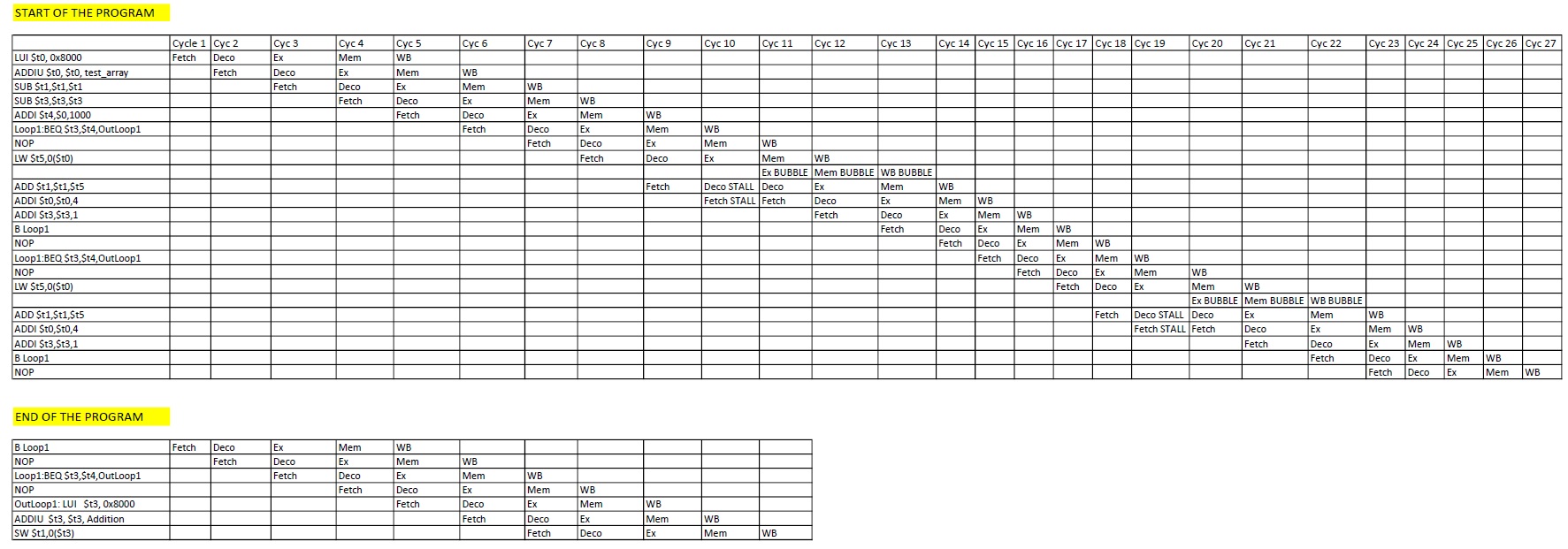
* The first instruction is fetched in cycle 1.
* The first iteration starts in cycle 6 and ends in cycle 18. Thus, the first iteration takes 13 cycles.
* The remaining 999 iterations take 8 cycles (for example, the second iteration starts in cycle 19 and ends in cycle 26).
* The end of the loop (beq and flushed lw) plus the three external instructions takes 5 more cycles.

Taking all this into account we have:

* Number of cycles = 5 + 13 + 999\*8 + 5 = 8015 cycles
* Number of instructions = 5 + 1000\*6 + 4 = 6009 instructions
* **CPI** = 8015/6009 **≈** **1.33**

# Analytical study in MIPSfpga

**Timing diagram:**

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**Detailed analysis:**

* The first instruction is fetched in cycle 1.
* The first iteration starts in cycle 6 and ends in cycle 18. Thus, the first iteration takes 13 cycles.
* The remaining 999 iterations take 9 cycles (for example, the second iteration starts in cycle 19 and ends in cycle 27).
* The end of the loop (beq and nop) plus the three external instructions takes 5 more cycles.

Taking all this into account we have:

* Number of cycles = 5 + 13 + 999\*9 + 5 = 9014 cycles
* Number of instructions = 5 + 1000\*6 + 4 = 6009 instructions
* **CPI** = 9014/6009 **≈** **1.5**

# Empirical study in MIPSfpga

## Original program (no optimizations)

The results provided by the performance counters are the following:

* **Number of cycles = 9047**
* **Number of instructions =** 8017 – 2000 (2 nops per iteration) **= 6017**
* **CPI =** 9047/6017 **≈ 1.5**

## Original program (-O3 option)

The results provided by the performance counters are the following:

* **Number of cycles = 8046**
* **Number of instructions =** 7011 – 1000 = **6011**
* **CPI =** 8046 / 6011 **≈ 1.34**

Note that the compiler fills the delay slot of the b instruction, but not the delay slot of the beq.

## Reordered program

New program:

".set noreorder;"

"LUI $t0, 0x8000;"

"ADDIU $t0, $t0, V;"

"SUB $t1,$t1,$t1;"

"SUB $t3,$t3,$t3;"

"ADDI $t4,$0,1000;"

"Loop1: BEQ $t3,$t4,OutLoop1;"

"ADDI $t3,$t3,1;"

"LW $t5,0($t0);"

"ADDI $t0,$t0,4;"

"B Loop1;"

"ADD $t1,$t1,$t5;"

"OutLoop1: LUI $t3, 0x8000;"

"ADDIU $t3, $t3, Addition;"

"SW $t1,0($t3);"

".set reorder;"

The results provided by the performance counters are the following:

* **Number of cycles = 6043**
* **Number of instructions = 6016**
* **CPI =** 6043 / 6016 **≈ 1**