* ***mpc\_dest\_w***

SOLUTION:

* + This signal is assigned through the Control Pipeline Registers in module *m14k\_mpc\_ctl*, from the E-Stage, signal ***dest\_e***.
  + Signal ***dest\_e*** is computed in a similar way to the simple pipelined processor from [2], in module *m14k\_mpc\_dec*, at line 1458, as follows:

assign dest\_e [5:0] = (special\_e | spec2\_e | mpc\_cnvt\_e | rwpgpr\_e | dest\_cnvt\_dsp\_e | lx\_e) ? { rwpgpr\_e & ~rdpgpr\_e, pdest\_e } : ((lnk31\_e) ? 6'h1f : { 1'b0, src\_b\_e[4:0] });

* + - When the instruction being executed is any of: ***special\_e***, ***spec2\_e***, ***mpc\_cnvt\_e***, ***rwpgpr\_e***, ***dest\_cnvt\_dsp\_e***, ***lx\_e***, then the destination register is assigned from signal ***pdest\_e***, which is obtained in module *m14k\_mpc\_dec*, line 1451, as follows:

assign pdest\_e [4:0] = (spec2\_e && (mpc\_ir\_e[5:4] == 2'b01)) ? edp\_udi\_wrreg\_e[4:0] : mpc\_ir\_e[15:11];

For example, an *add* instruction, which has a *special* opcode (signal ***special\_e***=1), matches this case.

* + - When the instruction being executed is a jump&link instruction, the destination register is $ra (register 31).
    - Finally, in any other case (such as a lw instruction), the destination register is assigned from signal ***src\_b\_e***, which is obtained in module *m14k\_mpc\_dec*, line 1445, as follows:

assign src\_b\_e [5:0] = { rdpgpr\_e, mpc\_ir\_e[20:16]};

* ***mpc\_rfwrite\_w***.

SOLUTION:

* + ***mpc\_rfwrite\_w*** depends on ***pvd\_w***, which is registered from the E-Stage through the Pipeline Registers. ***pvd\_w*** depends on ***vd\_e***.

At the E-Stage, in the Decoding Module (*m14k\_mpc\_dec*), signal ***vd\_e*** is computed. This signal is set to 1 for all instructions that will write to the RF at the W-Stage.

* + ***mpc\_rfwrite\_w*** also depends on ***mpc\_exc\_w***, which is 1 when an exception is triggered at the W-Stage. In case there is an exception, the RF write is inhibited.
  + ***mpc\_rfwrite\_w*** also depends on ***mpc\_run\_w***, which is 1 when an instruction is executing in the W-Stage. In case W-Stage is not executing, RF write is inhibited.