* **EXPLANATION**:

Detailed explanation: All changes related to the new instruction are tagged with comment: *// LWPC* in the soft-core. We must perform the following actions:

* Inhibit “*Reserved Instruction Exception*”:

Comment:

*assign maj\_ri\_e = … (mpc\_ir\_e[31:26] == 6'o47) ||*

* New signal:
  + - * ***lwpc\_instr***: Set to 1 when lwpc found:

*assign lwpc\_instr = (mpc\_ir\_e[31:26] == 6'o47);*

* Incorporate new functionality:
  1. We must insert the new operands as an input to the *lw* adder. ***aop\_e*** and ***dva\_offset\_e*** are the inputs to the adder that calculates the Effective Address:
  2. ***aop\_e***: Incorporate the PC as an input. The PC is already available at E-Stage in signal ***iva\_e***.

*assign* ***aop\_e****[31:0] = lwpc\_instr ? iva\_e : (icc\_pcrel\_e ? (iva\_e & ~{30'b0, {2{icc\_pcrel\_e}}}) : edp\_abus\_e); // LWPC*

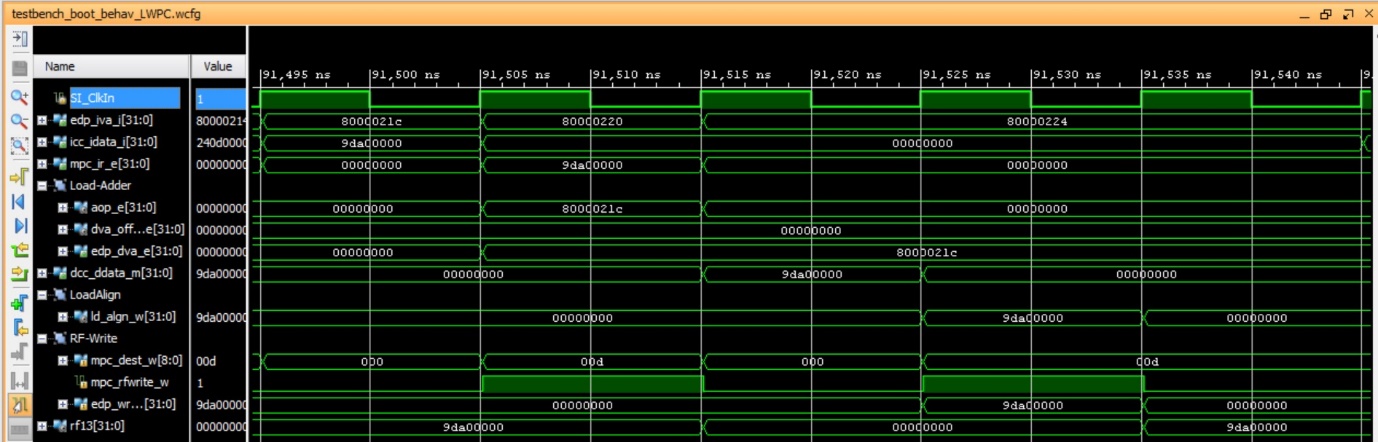
* 1. ***dva\_offset\_e***: Incorporate the SignExt(Imm<<2) as an input.

*assign* ***dva\_offset\_e****[31:0] = lwpc\_instr ? { {11{mpc\_ir\_e[18]}}, mpc\_ir\_e[18:0], 2'b0} : {32{mpc\_subtract\_e}} ^ bbus\_imm\_e; // LWPC*

* We must select Rs as Destination Register:

*assign dest\_e [5:0] = lwpc\_instr ? { 1'b0, mpc\_ir\_e[25:21] } : ((special\_e | spec2\_e | mpc\_cnvt\_e | rwpgpr\_e | dest\_cnvt\_dsp\_e | lx\_e) ? { rwpgpr\_e & ~rdpgpr\_e, pdest\_e } : ((lnk31\_e) ? 6'h1f : { 1'b0, src\_b\_e[4:0] })); // LWPC*

* **EXAMPLE - SIMULATION**:



Observe that in the fifth cycle rf13 is written to 0x9da00000, which corresponds to the opcode of the instruction stored at PC=0x8000021c.

* **EXECUTION ON THE BOARD**:

When the program is downloaded on the board, you should see on the 7-seg displays:

* 7-seg displays=$t5, which in our example is 0x9da00000

Then, when you debug the program following the steps stated in the document, you should observe the following:

