**LRU:**

Examining set *a* for one iteration (a1 a2 a1 a3 a2 a3): The first two accesses miss. After these two accesses, the LRU block is a1. The third access hits, and sets a2 as the LRU block. The fourth access misses: a3 replaces a2. The fifth access misses: a2 replaces a1. The sixth access hits. This results in 4 misses and 2 hits per iteration and per block. Thus, 4\*4\*2 = 32 misses.

EXPERIMENTAL STUDY:

* D$ Accesses: 48
* D$ Misses: 32

**FIFO:**

ANALITICAL STUDY: Examining set *a* for one iteration (a1 a2 a1 a3 a2 a3): The first two accesses miss. The third access hits. The fourth access misses: a3 replaces a1 (which was inserted before a2). The fifth access hits. The sixth access hits. This results in 3 misses and 3 hits per iteration and per block. Thus, 3\*4\*2 = 24 misses.

EXPERIMENTAL STUDY:

* D$ Accesses: 48
* D$ Misses: 24