AcroPack Series AP323
16-Bit High Density Analog Input Module

USER'S MANUAL

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1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Radio Frequency Interference Statement

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

AP323 OVERVIEW

The AcroPack Series AP323 module is a precision 16-bit analog input module, with the capability to monitor 20 differential or 40 single-ended analog input channels. The AP323 offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

Ordering Information

The AcroPack ordering options are given in the following table:

Model	Operating Temperature Range
AP323E-LF[1]	-40 to +85°C

1. Applications requiring operating temperatures of 70°C to 85°C will require purchase of **AP-CC-01 AcroPack Conduction Cool Kit** (See APPENDIX for installation instructions) with a minimum airflow of 400LFM. For temperatures below 70°C the module will require a minimum airflow of 200LFM.

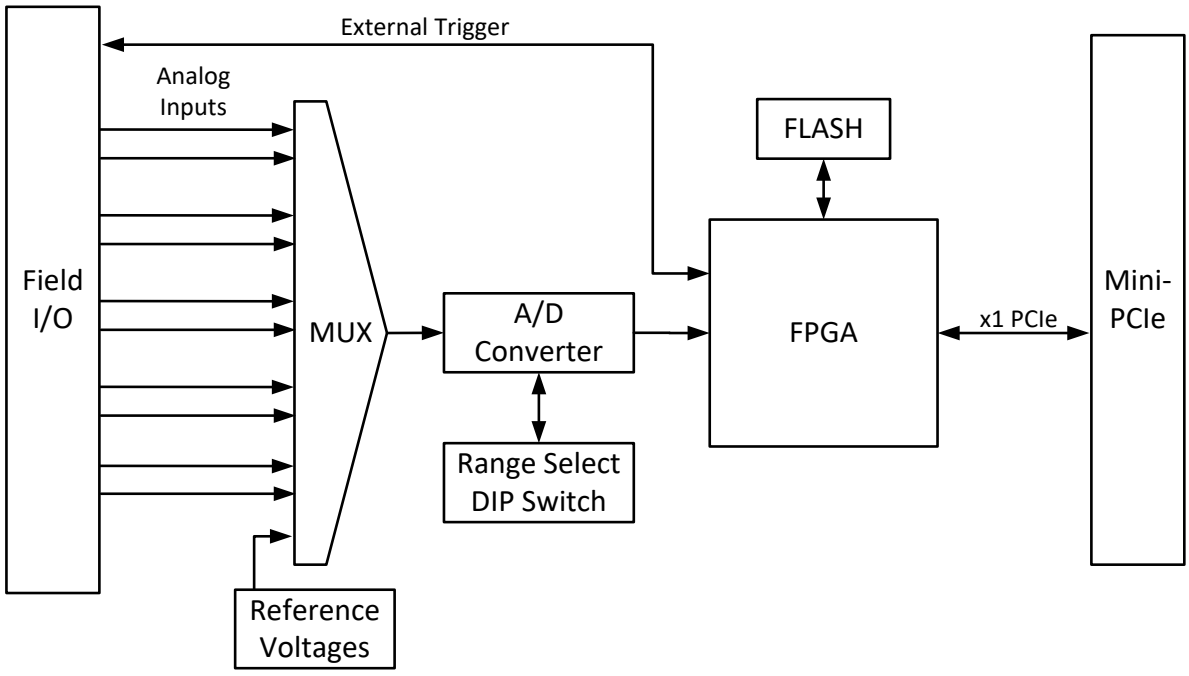


Figure 1 AP323 Block Diagram

KEY FEATURES

A/D 16-Bit Resolution - 16-bit capacitor-based successive approximation Analog to Digital Converter (ADC) with integral sample and hold and reference.

8µsec Conversion Time - A maximum conversion rate of 125KHz is supported. Maximum recommended conversion rate for specified accuracy is 67KHz.

High Density - Monitors up to 20 differential or 40 single-ended analog inputs (acquisition mode and channels are selected via programmable control registers).

Deep Sample FIFO – holds 16K samples. This permits a relaxed real-time requirement of the host system.

Flexible Scan Control – Channels are scanned in the order specified by a user defined scan list. This provides the option to sample selected channels at higher frequency than others, or to sample selected channels multiple times per scan group to provide increased settling time or greater effective resolution.

Interrupt Upon Conversion Complete Mode - May be programmed to interrupt upon completion of conversion for each individual channel, or upon completion of conversion of the group of all scanned channels.

User Programmable Interval Timer - Controls the delay between each channel converted when Uniform-Continuous or Single Scan modes are selected. If Burst-Continuous is selected, the Interval Timer controls the period of the group of channels. The interval timer's range is a minimum period of 8μsec and a maximum period of 2.09 seconds.

Uniform Continuous Scanning Mode - All channels selected for scanning are continually digitized in a round robin fashion with the interval between conversions controlled by the programmed interval timer. The results of each conversion are stored in the sample FIFO. Scanning is stopped by software control.

Burst Continuous Scanning Mode – Each channel in the scan list is digitized in the order they were added to the scan list. All channels in the list are sequentially digitized at a 66,773.5 Hz conversion rate (14.967μ second conversion time). At the end of a programmed interval time a new conversion of all channels is re-initiated. The conversion results are stored in the sample buffer. This mode can be used as a pseudo-simultaneous sampling mode for low to medium speed applications requiring simultaneous channel acquisition. For example, if four channels are selected then they could be pseudo-simultaneously converted every 60μ seconds (each of the channels actually takes 14.967μ seconds). This is repeated in bursts determined by the programmed interval time. The scan is initiated by a software or external trigger. Scanning is stopped by software control.

Uniform Single Cycle Scan Mode - All channels in the scan list are digitized once with the idle time between each channel conversion controlled by the programmed interval timer. The scan is initiated by a software or external trigger.

Burst Single Cycle Scan Mode - All channels in the scan list are digitized once at a 66,773.5 Hz conversion rate (14.967μsec/Channel). The scan is initiated by a software or external trigger.

External Trigger Scan Mode - A single channel is digitized with each external trigger. Successive channels are digitized in sequential order with each new external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.

External Trigger Output - The external trigger is assigned to a field I/O line. This external trigger may be configured as an output signal to provide a means to synchronize other AP323 modules or devices to a single AP323's on board timer reference.

Precision On Board Calibration Voltages - Calibration auto-zero and auto-span precision voltages are available to permit host computer correction of conversion errors. Calibration voltages include: 0V (local analog common), 9.88V, 4.94V, 2.47V, and 1.235V.

Hardware DIP Switch for Selection of A/D Ranges - Both bipolar (±5V, ±10V) and unipolar (0 to 5V and 0 to 10V) ranges are available. Selected range applies to all channels and cannot be individually selected on a per channel basis.

User Programmable Data Output Format - Software control provides selection of straight binary or binary two's complement data output format.

Fault Protected Input Channels - Analog input overvoltage protection from -35 V to +55 V is provided in the event of power loss or power off.

AcroPack Module INTERFACE FEATURES

Field Connections – All analog input, trigger, and power connections are made through a single 100-pin board stacking connector. An AcroPack carrier board will provide the connection between the AcroPack module and the field cabling.

PCIe Bus – This AP module includes a PCI Express Generation 1 interface operating at a speed of 2.5 Gbps with one lane in each direction.

Compatibility –– PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

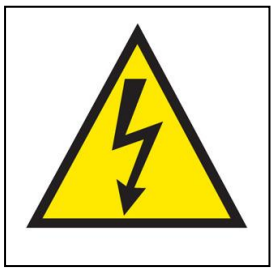
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original

manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

Installation Considerations

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed PMC modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the AcroPack module to the carrier/CPU board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the PCIe bus and AcroPack module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible DIP switch and jumper settings will be discussed in the following sections. The DIP switch and jumper locations are shown in Figure 2.

Remove power from the carrier board when configuring hardware jumpers, installing AcroPack modules, cables, termination panels, and field wiring. Refer to the APPENDIX and the following paragraphs for configuration and assembly instructions.

Default Configuration

When the board is shipped from the factory, it is configured as follows:

Analog input range is configured for a bipolar input with a 10 Volt span (i.e. an ADC input range of -5 to +5 Volts).

The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired mode, and channel configuration before starting ADC analog input acquisition.

Analog Input Range Configuration

The ADC input range is selected via switches. The switches control the input voltage span and the selection of unipolar or bipolar input ranges. The configuration of the switches for the different ranges is shown in Table 1. The switch location is shown in Figure 2.

Table 1 Analog Input Range Selections/DIP Switch Settings

ADC Input Range (VDC)	Input Span (Volts)	Input Type	Switch Settings ON	Switch Settings OFF
-5 to +5	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 to +10	20	Bipolar	2,5,6,9	1,3,4,7,8
0 to +5	5	Unipolar	1,3,5,8	2,4,6,7,9
0 to +10	10	Unipolar	1,3,4,7	2,5,6,8,9

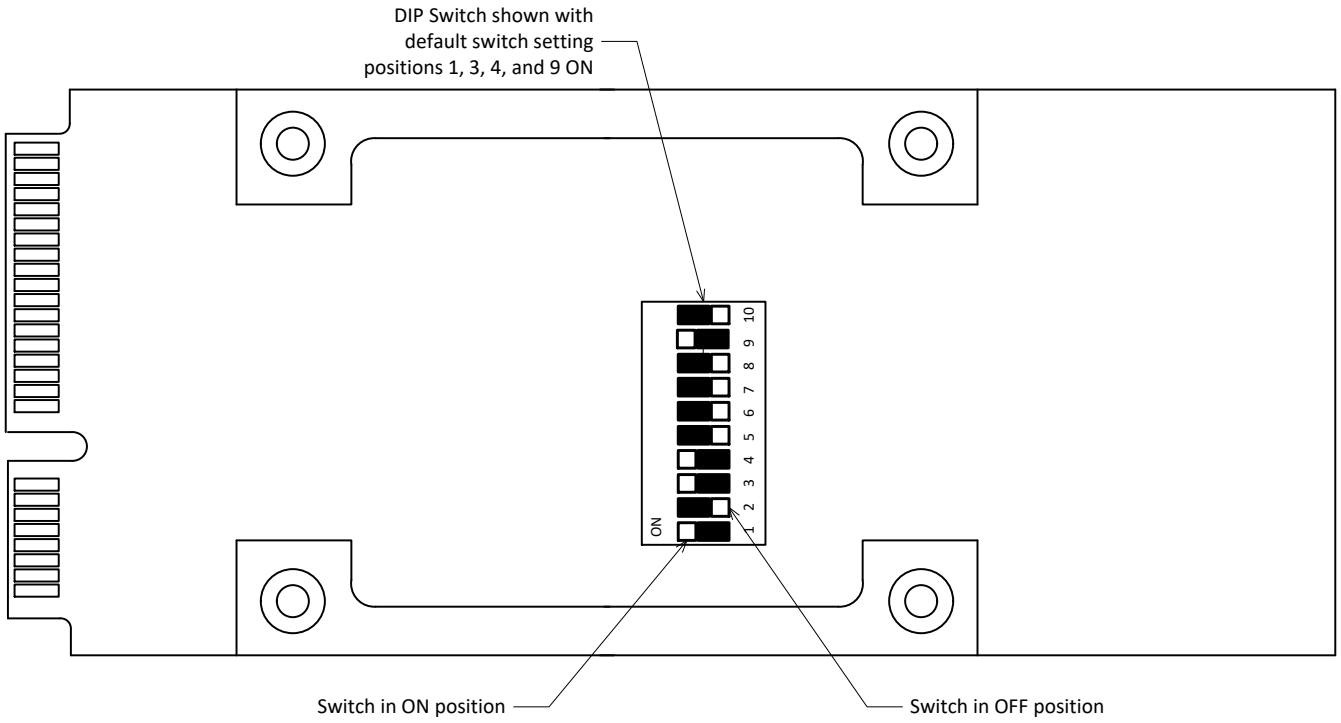


Figure 2 Range Select Switch

Software Configuration

Software configurable control registers are provided for control of external trigger mode, data output format, acquisition mode, timer control, interrupt mode, and convert channel(s) selection. These control registers must also be configured as needed for the application before starting ADC analog input acquisition. Refer to section 3 for details.

Wiring Recommendations

Differential Voltage input connections are recommended over single ended to achieve the greatest accuracy and lowest noise.

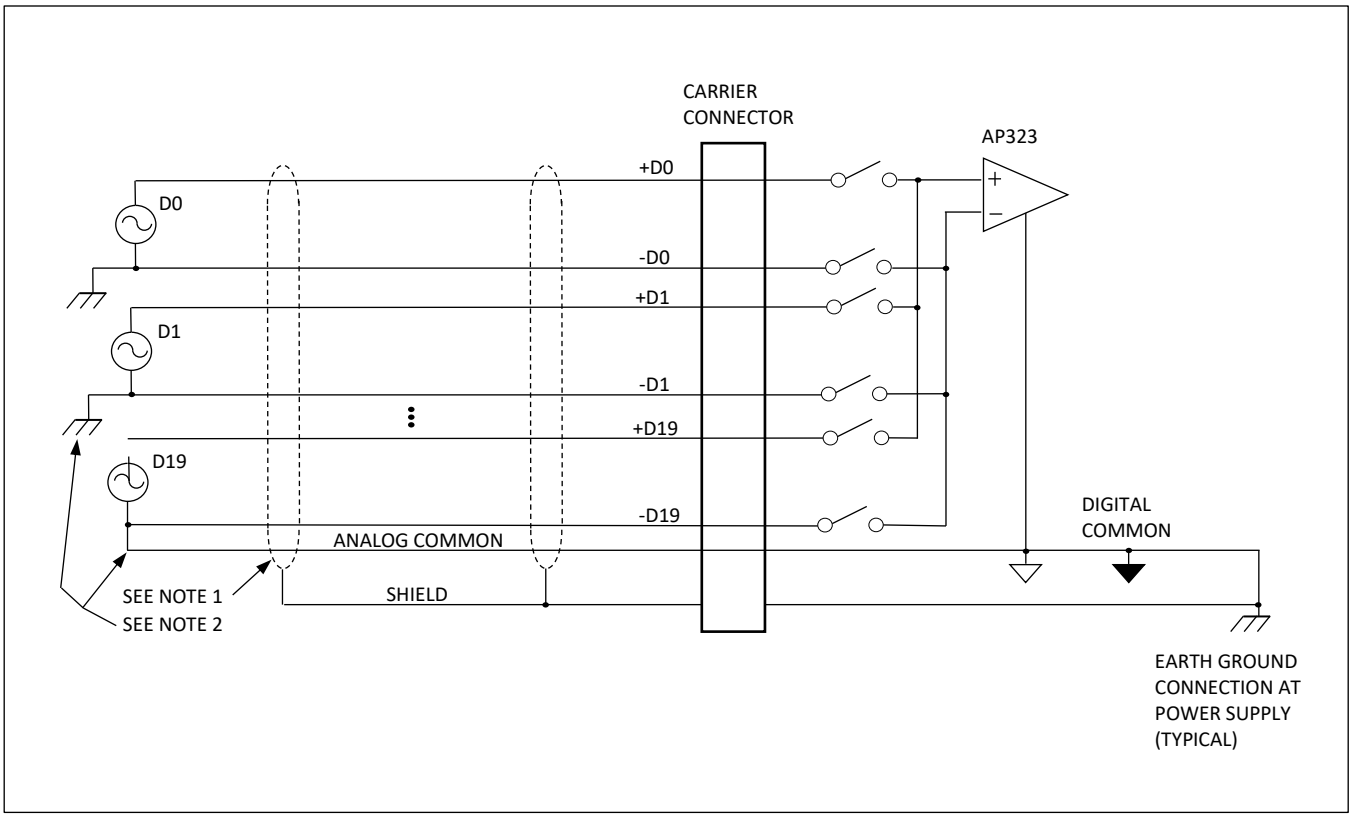


Figure 3 Differential Voltage Input Connection Diagram

1. Shielded cable is recommended for lowest noise. Shield is connected to ground reference at one end only to provide shielding without ground loops.
2. Reference channels to analog common if they would otherwise be floating. Channels already having a ground reference must not be connected to analog common to avoid ground loops.

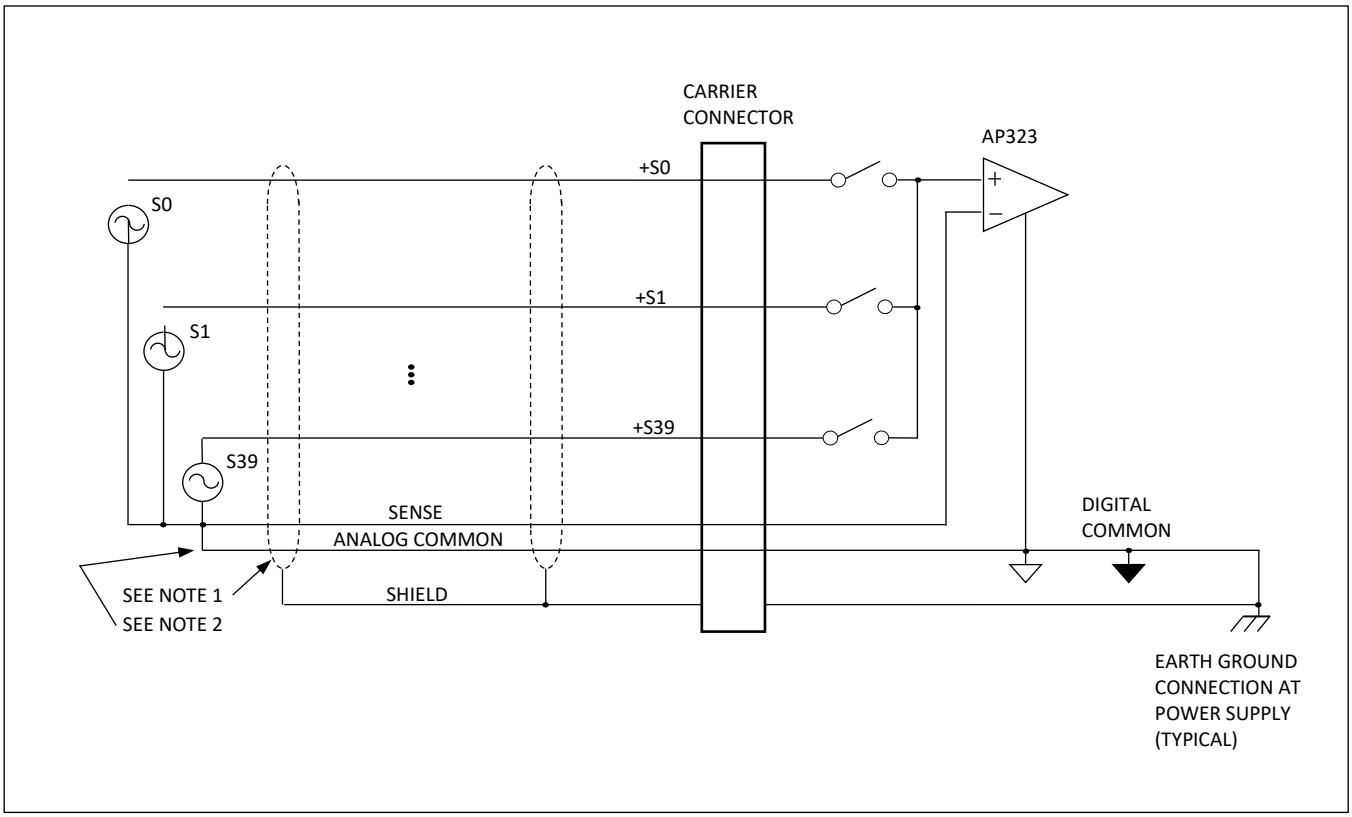


Figure 4 Single Ended Voltage Input Connection Diagram

1. Shielded cable is recommended for lowest noise. Shield is connected to ground reference at one end only to provide shielding without ground loops.
2. Reference channels to analog common if they would otherwise be floating. Channels already having a ground reference must not be connected to analog common to avoid ground loops.

CONNECTORS

Field I/O Connector P2

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Pin assignments are unique to each AP model. Table 2 lists signal pin assignments for the module field I/O connector. Pins are left unconnected in order to meet the minimum creepage distance required for 60 Volt isolation. Front panel connector P2 pin assignments are shown in Table 2. When reading Table 2 note that channel designations are abbreviated to save space. For example, single ended channel 0 is abbreviated as “S00”; the +input for differential channel 0 is abbreviated as “D00+”. Both of these labels are attached to pin 1, but only one is active for a particular installation (i.e. if your

inputs are applied differentially, which is recommended for the lowest noise and best accuracy, follow the differential channel labeling for each channel's + and - input leads).

IMPORTANT: All unused analog input pins should be tied to analog ground. Floating unused inputs can drift outside the input range causing temporary saturation of the input analog circuits. Recovery from saturation is slow and affects the reading of the desired channels.

Table 2 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	S00, D00+
35	26	2	1	S20, D00-
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	S01, D01+
36	27	4	5	S21, D01-
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	S02, D02+
37	28	6	9	S22, D02-
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	S03, D03+
38	29	8	13	S23, D03-
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	S04, D04+
39	30	10	17	S24, D04-
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	S05, D05+
40	31	12	21	S25, D05-
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	S06, D06+
41	32	14	25	S26, D06-
			28	Reserved/isolation

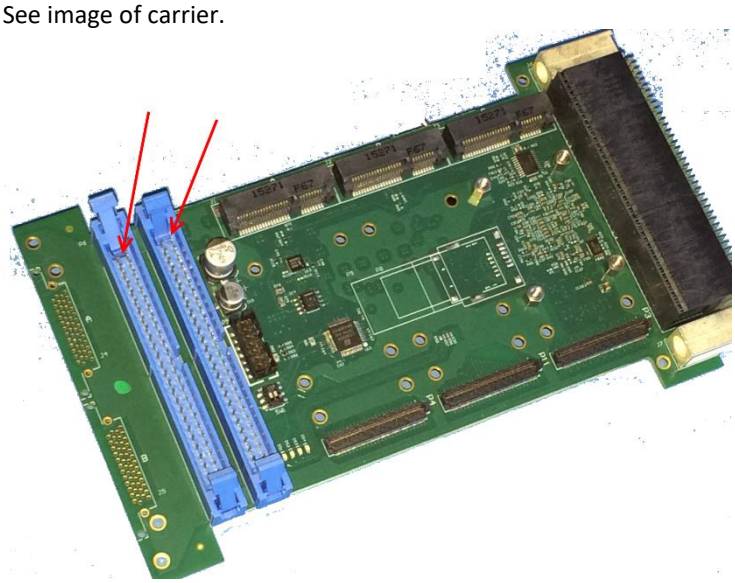
68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			27	Reserved/isolation
8	8	15	30	S07, D07+
42	33	16	29	S27, D07-
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	S08, D08+
43	34	18	33	S28, D08-
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	S09, D09+
44	35	20	37	S29, D09-
			40	Reserved/isolation
			39	Reserved/isolation
11	11	21	42	S10, D10+
45	36	22	41	S30, D10-
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	S11, D11+
46	37	24	45	S31, D11-
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	S12, D12+
47	38	26	49	S32, D12-
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	S13, D13+
48	39	28	53	S33, D13-
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	S14, D14+
49	40	30	57	S34, D14-
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	S15, D15+
50	41	32	61	S35, D15-
			64	Reserved/isolation

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			63	Reserved/isolation
17	17	33	66	S16, D16+
51	42	34	65	S36, D16-
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	S17, D17+
52	43	36	69	S37, D17-
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	S18, D18+
53	44	38	73	S38, D18-
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	S19, D19+
54	45	40	77	S39, D19-
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	SENSE
55	46	42	81	SENSE
			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	COMMON
56	47	44	85	COMMON
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	NC
57	48	46	89	NC
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	NC
58	49	48	93	*Ext Trigger[3]
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	NC
59	50	50	97	Chassis GND
			100	Reserved/isolation

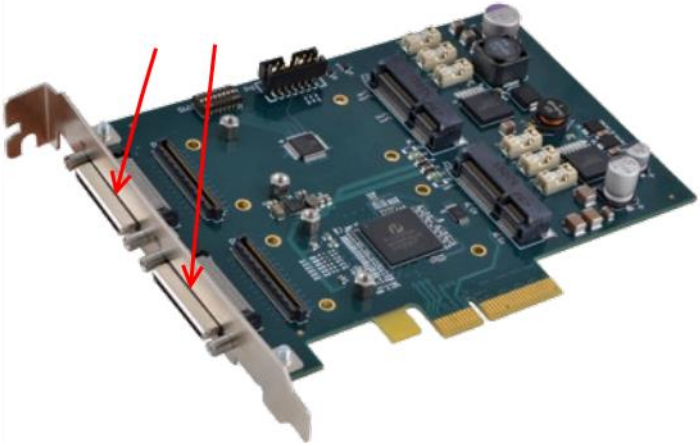
68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			99	Reserved/isolation

Note:

1. VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector. See image of carrier.



2. APCe7020E-LF is an example of a carrier that uses the Champ connector. See image of carrier.



3. * Indicates that the signal is active low.
4. Some AcroPack carriers utilize a double-stack 68-pin Champ connector. On these carriers, pins 26 thru 34 and 60 thru 68 are not connected.

Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all

AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 3 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The 'Present' signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 3 Logic Interface Connections

Pin #	Name	Pin #	Name
51	+5V[2]	52	+3.3V[3]
49	+12V[2]	50	GND
47	-12V[2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	N.C. (+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#[1]	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: Signals are not applicable for the AP323 implementation. Pins are either "no connects" on the module or are repurposed for JTAG.

Note 2: +5V, +12V, and -12V power supplies have been assigned to pins that are reserved in the mini-PCIe specification.

Note 3: All +3.3Vaux power pins are changed to +3.3V power.

Note 4: The 'Present' signal is tied to circuit common on the AP module.

Note 5: The SM Bus signals SMB_CLK and SMB_DATA are used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the AcroPack module and be within the allowable voltage range of the input circuitry.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Figure 3 and Figure 4 for analog input connections for differential and single-ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

Single-ended inputs only require a single lead (+) per channel, with a shared "sense" (reference) lead for all channels, and can be used when a large number of input channels come from the same location (e.g. printed circuit board). The channel density doubles when using single-ended inputs, and is a powerful incentive for their use. However, caution must be exercised since the single "sense" lead references all channels to the same common which will induce noise and offset to the degree they are different.

The AP323 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier/CPU board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AP323 input module.

External Trigger Input/Output

The external trigger signal can be programmed as disabled, or to input a TTL compatible external trigger signal, or output AP323 hardware generated triggers to allow synchronization of multiple AP323s.

As an input, the external trigger must be a 3.3 Volt logic, TTL-compatible, debounced signal referenced to analog common. The external trigger signal is an active low edge sensitive signal. That is, the external trigger signal will trigger the AP323 hardware on the falling edge. Once the external trigger

signal has been driven low, it should remain low for a minimum of 500n seconds.

As an output an active-low TTL signal can be driven to additional AP323s, thus providing a means to synchronize the conversions of multiple AP323s. The additional AP323s must program their external trigger for signal input and convert on external trigger only mode. See section 3 for programming details to make use of this signal.

3. PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP323 module.

This Acromag AP323 is a PCI Express Base Specification, Revision 2.1compliant AcroPack module. The carrier/CPU connects a PCIe bus to the AcroPack module.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AP323 module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access an AcroPack's configuration registers.

PCIe Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the module requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the module.

Since this module is relocatable and not fixed in address space, this module's device driver must use the mapping information stored in the module's Configuration Space registers to determine where the module is mapped in memory space and which interrupt line will be used.

Configuration Registers

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This module provides 512 bytes of configuration registers for this purpose. The AP323 contains the configuration registers, shown in Table 4, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the AP323 and the interrupt request line that goes active on an AP323 interrupt request.

Table 4 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=7017		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for AP323 4K-Byte Block (BAR0)			
5 : 10	Not Used			
11	Subsystem ID=7017		Subsystem Vendor ID=16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCIe bus memory space to control the acquisition of analog inputs from the field. As such, three types of information are stored in the memory space: control, status, and data.

The memory space address map for the AP323 is shown in Table 5. Note that the base address for the AP323 in memory space must be added to the addresses shown to properly access the AP323 registers.

Table 5 AP323 Memory Map

Description	Base Addr+
Interrupt Register	00
Location Register	04
Control Register	08
Timer Prescaler	0C
Conversion Timer	10
Scan List FIFO	14
Scan List FIFO Count	18
Status	1C
Sample FIFO	20
Sample FIFO count	24
Trigger / FIFO clear	28
XADC Status/Control	60
XADC Address	64
Firmware Revision Register	200
Flash Data	204
Flash Chip Select	208

Interrupt Register, (Read/Write) - (Base + 00H)

1. This read/write register is used to enable board interrupt, determine the pending status of interrupts, and release an interrupt.

The function of each of the interrupt register bits are described in Table 6. A power-up or system reset sets all interrupt register bits to 0.

Table 6 Interrupt Register

BIT	FUNCTION
0	Board Interrupt Enable Bit. This bit must be set to logic “1” to enable generation of interrupts from the AP323. Setting this bit to logic “0” will disable board interrupts. (Read/Write Bit)
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the AP323. When this bit is logic “1” an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is a logic “0” an interrupt is not being requested.
14 to 2	Not Used[1]
15	Interrupt Release Bit. This bit must be set to a logic “1” to release an interrupt request. This bit is typically set in the interrupt service routine to remove the interrupt request. Once an interrupt request is generated on the AP323, it will continue to assert the interrupt request until this Interrupt Release bit is set to logic “1” or interrupts are disabled via bit 0 of this register.

Notes (Table 6):

1. All bits labeled “Not Used” will return logic “0” when read.

Location Register, (Read Only) – (Base + 04H)

This read only register is used identify the module's plugin location in a system.

Table 7 Location Register

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or a carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

Control Register, (Read/Write) - (Base + 08H)

This read/write register is used to select the output data format, select the external trigger signal as an input or output, select acquisition input mode, select scan mode, enable/disable the timer, and select the interrupt mode.

The function of each of the control register bits are described in Table 8. A power-up or system reset sets all control register bits to 0.

Table 8 Control Register

BIT	FUNCTION
0	Output Data Format 0 = Binary Two's Complement 1 = Straight Binary See Table 10 for a description of these two data formats.

2,1	External Trigger 00, 11 = Disabled 01 = Input 10 = Output It is possible to synchronize the data acquisition of multiple AP323 modules. A single master AP323 module must be selected to output the external trigger signal while all other AP323 modules are selected to input the external trigger signal. The external trigger must also be wired together for all synchronized modules. The External Trigger input could be sensitive to external EMI noise, which can cause erroneous external triggers. If External Trigger input or output is not required, the External Trigger should be configured as Disabled.
5,4,3	Acquisition Input Mode 000 = All Channels Differential Input 001 = All Channels Single Ended Input 010 = Not Used 011 = 9.8800v Calibration Voltage Input 100 = 4.9400v Calibration Voltage Input 101 = 2.4700v Calibration Voltage Input 110 = 1.2350v Calibration Voltage Input 111 = Auto Zero Calibration Voltage Input
7,6	Not Used[1]
BIT	**FUNCTION**
10,9,8	Scan Mode 000 = Disable 001 = Uniform Continuous 010 = Uniform Single 011 = Burst Continuous 100 = Burst Single 101 = Convert on External Trigger Only 110 = Not Used 111 = Not Used See the Modes of Operation section for a description of each of these scan modes.
11	Timer Enable 0 = Disable 1 = Enable
13,12	Interrupt Control 00 = Disable Interrupts 01 = Interrupt After Convert of Each Channel 10 = Interrupt After Conversion of all selected channels is completed. A group of channels includes all channels from the Start Channel up to and including the End Channel value. 11 = Disable Interrupts
15,14	Not Used[1]

Notes (Table 8):

1. All bits labeled “Not Used” will return logic “0” when read.

Analog Input Ranges and Corresponding Digital Output Codes

Selection of an analog input range is implemented via the DIP switch settings given in Table 1. The ideal input voltage corresponding to each of the

supported input ranges is given in Table 9. In Table 10 the digital output code corresponding to each of the given ideal analog input values is given in both binary two's complement and straight binary formats.

Table 9 Supported Full-Scale Ranges and Ideal Analog Input

DESCRIPTION	ANALOG INPUT			
Input Range	±10V	0 to 10V	±5V	0 to 5V
LSB (Least Significant Bit) Weight	305µV	153µV	153µV	76µV
+ Full Scale Minus One LSB	9.999695V	9.999847V	4.999847V	4.999924V
Midscale	0V	5V	0V	2.5V
One LSB Below Midscale	-305µV	4.999847V	-153µV	2.499924V
- Full Scale	-10V	0V	-5V	0V

The digital output format is controlled by bit-0 of the Control register. The two formats supported are Binary Two's Complement and Straight Binary. The hex codes corresponding to these two data formats are depicted in Table 10.

Table 10 Digital Output Codes and Input Voltages

	DIGITAL OUTPUT	
	Binary 2's Comp	Straight Binary
DESCRIPTION	(Hex Code)	(Hex Code)
+ Full Scale - 1 LSB	7FFF	FFFF
	DIGITAL OUTPUT	
	Binary 2's Comp	Straight Binary
DESCRIPTION	(Hex Code)	(Hex Code)
Midscale	0000	8000
1 LSB Below Midscale	FFFF	7FFF
- Full Scale	8000	0000

Timer Prescaler Register (Read/Write, Base + 0CH)

The Timer Prescaler register can be written with an 8-bit value to control the interval time between conversions.

Table 11 Timer Prescaler Register

Timer Prescaler Register							
MSB							LSB
07	06	05	04	03	02	01	00

This 8-bit number divides a 7.8125 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 40 hex or 64 decimal.

A Timer Prescaler value of less than 64 (decimal) will result in no data entry in the sample FIFO. This minimum value corresponds to a conversion interval of 8.192 μ seconds which translates to the maximum conversion rate of 122 KHz. Although the board will operate at the 122 KHz conversion rate, conversion accuracy will be sacrificed.

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows.

The Timer Prescaler register contents are cleared upon reset.

Conversion Timer Register (Read/Write, Base + 10H)

The Conversion Timer Register can be written to control the interval time between conversions. This register's contents are cleared upon reset.

Table 12 Conversion Timer Register

Conversion Timer Register															
MSB								LSB							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

This 16-bit number is the second divisor of a 7.8125 MHz clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by a 7.8125 MHz clock signal. The output of this clock is input to the second counter, the Conversion Timer, and this output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{7.8125} = \text{T in } \mu\text{seconds}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 64 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 7.8125 = 2.139 seconds. The minimum time interval which can be programmed to occur is
(64 * 1) ÷ 7.8125 = 8.192μ seconds. This minimum of 8.192μ seconds is defined by the minimum conversion time of the hardware but does sacrifice conversion accuracy. To achieve specified conversion accuracy a minimum conversion time of 14.976μ seconds is recommended (see the specification chapter for details regarding accuracy).

Scan List FIFO (Write, Base + 14H)

A list of the channels to be scanned must be written to the Scan List FIFO prior to the start of data acquisition. The channels can be scanned in any order. A channel can appear multiple times in the list to facilitate sampling some channels at a higher frequency than others. For example, the list 1,2,3,1,4,5,1,2,6,1,4,7 scans channel 1 at 4x the group frequency, channels 2 and 4 at 2x the group frequency and channels 3,5,6 and 7 at the group frequency. The Scan List FIFO can hold 1026 entries. The Scan FIFO full/empty status can be read from the status register. The Scan FIFO count register reports the current number of entries in the scan list.

The Scan List FIFO can be written with 8-bit data transfers. The Scan List FIFO contents are cleared upon reset or by writing bit 1 of the Trigger / FIFO Clear Register. Entries in the Scan List FIFO are not consumed during scanning. In continuous mode, after digitizing the last channel in the scan list, the scans continue with the first channel in the scan list.

Table 13 Scan List FIFO

Scan List FIFO Channel entry							
Unused		Channel					
07	06	05	04	03	02	01	00

When conversions are re-started after being halted, conversions continue with the next channel in the scan list following the last acquired channel.

Scan List FIFO Count (Read Only, Base + 18H)

The Scan List FIFO Count Register contains the count of entries in the Scan List FIFO. The counter is 11-bits

Table 14 Scan List FIFO Count Register

Scan List FIFO Count Register											
Unused					Count						
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Status (Read Only, Base + 1CH)

The status register reports the status of both the Scan List FIFO and the Sample FIFO.

Table 15 Status Register

BIT	FUNCTION
0	Scan List FIFO empty
1	Scan List FIFO full
2	Sample FIFO empty
3	Sample FIFO full
4	Sample FIFO overflow
8 – 5	Unused

Sample FIFO (Read Only, Base + 20H)

The Sample FIFO is read-only, and contains the 16-bit digitized input channel values. Each of the FIFO entries is tagged with the 6-bit channel number to form a 22-bit result. The FIFO entries are read as a 32-bit number with the most significant 10 bits set to zero. The Sample FIFO has 16,384 storage locations. The Sample FIFO must be read using a 32-bit read operation.

Table 16 Sample FIFO

Sample FIFO entry								
Unused			Channel			A/D Conversion Result		
31	. . .	22	21	. . .	16	15	. . .	0

Sample FIFO Count (Read Only, Base + 24H)

The Sample FIFO Count register is read-only, and contains the 15-bit count of the number of samples in the Sample FIFO. The Sample FIFO Count register must be read using a 32-bit read operation.

Table 17 Sample FIFO Count

Sample FIFO Count					
Unused			Count		
31	. . .	15	14	. . .	0

Trigger / FIFO Clear Register (Write Only, Base + 28H)

The Trigger / FIFO Clear register is a write-only register and is used to trigger conversions or clear FIFOs.

Table 18 Trigger / FIFO Clear Register

BIT	FUNCTION
0	Start Convert
1	Clear Scan List FIFO
2	Clear Sample FIFO
3	Clear Sample FIFO overflow flag
8 – 3	Unused

Conversions are started by setting data bit-0 of this register to a logic one. The Scan List FIFO, Sample FIFO and Sample FIFO overflow flag can be cleared by setting their respective bits to one.

Prior to the start of data acquisition, the mode must first be configured by setting the following registers: Control, Scan List FIFO, Timer Prescaler, and Conversion Timer.

This register can be written with either a 32-bit, 16-bit or 8-bit data value. Data bit-0 must be a logic one to start data conversions.

For the External Trigger Only mode the Software Start Convert bit is not used to start data acquisition. However, the Start Convert bit should be set prior to the first external trigger. In this mode the Start Convert bit serves as a means

for the hardware to identify the occurrence of the first External Trigger. On the first external trigger (given the Software Start Convert bit is set) converted data from the A/D Converter is not written to the Sample FIFO since it is old convert data. See the Convert on External Trigger Only-Mode (in the Modes of Operation section) for additional details.

At least 5µ seconds of data acquire time should be provided after programming the Control register and Scan List FIFO before a Software Start Convert command is issued. These configuration registers control the AP323 on board multiplexers which select the desired channel for input to the converter.

XADC Status/Control Register (Read/Write) - (Base + 60H)

This read/write register will access the XADC register at the address set in the XADC Address Register allowing the module's key supply voltages and FPGA junction temperature to be monitored.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at Base plus 0x64H. Next, this register at Base plus 60H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only) - (Base + 64H)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x60H.

Table 19 System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 20 FPGA Voltage and Temperature Range

	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Recommended Operating Temperature Range	-40°C	50-60°C	100°C[1]

Notes:

1. Absolute maximum junction temperature 125°C

Firmware Revision Register (Read Only) - (Base + 200H)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

Flash Data Register (Read/Write) - (Base + 0204H)

A byte write to this address triggers a write/read serial transfer to/from the serial FLASH device. A byte read from this address returns the data read from a previous write/read serial transfer.

WARNING: Factory calibration data is stored in FLASH. Writing to FLASH could result in loss of factory calibration data. See Table 23 Flash Memory Map.

Note that the Flash chip select must be set prior to the start of any instruction. Flash chip select must also be driven high after the instruction is issued.

Table 21 Flash Data Register

BIT	Function
31 - 8	Unused
7 - 0	Flash Data

Note that any registers/bits not used will remain at the default value logic low.

Flash Chip Select Register (Write Only) - (Base + 0208H)

Writing "0" to bit-0 activates the Flash chip select signal. The default state of this bit is logic "1" which is the inactive state of the Flash chip select signal.

Note that the Flash chip select must be set prior to the start of Flash memory instruction. Flash chip select must also be driven high after the instruction is issued.

Table 22 Flash Chip Select Register

BIT	Function
31 - 1	Unused
0	Flash Chip Select

Flash Memory Map

Calibration coefficients for ADC reference voltage values and a model identification string are stored in flash memory.

Reference voltage values are provided so that software can adjust and improve the accuracy of the analog input voltage over the uncalibrated state. The reference voltages are precisely measured at the factory and then stored to this location at the addresses given in Table 23. See the "Use of Calibration Reference Signals" section for analog input calibration correction details.

Reference voltages are stored in memory as a null terminated ASCII character string. For example, if the value 9.88335 were stored to memory the corresponding ASCII characters would be 39, 2E, 38, 38, 33, 33, 35, 00 as shown in Table 23. Note, the ASCII equivalent of a decimal point is 2E and the null character is 00. For this example, the memory should be read starting at address 0x3F E000H until the null ASCII character is read.

Table 23 Flash Memory Map

Flash Address	Description
0x3F E000	Most significant digit of 9.88 Cal Voltage

⋮	⋮
0x3F E006	Least significant digit of 9.88 Cal Voltage
0x3F E007	Null character
0x3F E008	Most significant digit of 4.94 Cal Voltage
⋮	⋮
0x3F E00E	Least significant digit of 4.94 Cal Voltage
0x3F E00F	Null character
0x3F E010	Most significant digit of 2.47 Cal Voltage
⋮	⋮
0x3F E016	Least significant digit of 2.47 Cal Voltage
0x3F E017	Null character
0x3F E018	Most significant digit of 1.23 Cal Voltage
⋮	⋮
0x3F E01E	Least significant digit of 1.23 Cal Voltage
0x3F E01F	Null character
0X3F E020	Reserved
⋮	⋮
0X3F EFEF	Reserved
0X3F EFF0	Model Id byte 0 “A = 0x41”
0X3F EFF1	Model Id byte 1 “P= 0x50”
0X3F EFF2	Model Id byte 2 “3= 0x33”
0X3F EFF3	Model Id byte 3 “2= 0x32”
0X3F EFF4	Model Id byte 4 “3= 0x33”
0X3F EFF5	“Null = 0x00”
0X3F EFF6	Reserved
⋮	⋮
0X3F EFFF	Reserved

MODES OF OPERATION

The AP323 provides five different modes of analog input acquisition to give the user maximum flexibility for each application. These modes of operation include: uniform continuous, uniform single, burst continuous, burst single, and convert on external trigger only. In all modes a single channel or a sequence of channels may be converted. The following sections describe the features of each and how to best use them.

Uniform Continuous-Mode

In uniform continuous mode of operation, conversions are performed continuously (in sequential order) for all channels in the scan list. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set “01” to accept the external trigger as an input signal.

Stopping the execution of uniform continuous conversions is possible by writing 000 to the Scan Mode bits (10-8) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

Interrupts can be enabled to activate after conversion of each channel or the group of channels in the scan list. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8μ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 8μ seconds after the interval time of the last selected channel has expired.

If interrupts are selected to go active after conversion of each channel be sure to program a large enough interval between conversions to allow adequate time for execution of an interrupt service routine. It may also be necessary to allow time for your computer to perform other housekeeping operations between servicing interrupts.

Uniform Single-Mode

In uniform single mode of operation, conversions are performed once (in sequential order) for all channels in the scan list. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set ”01” to accept the external trigger as an input signal.

Interrupts can be enabled to activate after conversion of each channel or the group of channels in the scan list. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8µ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 8µ seconds after the interval time of the last selected channel has expired.

Burst Continuous-Mode

In burst continuous mode of operation, conversions are continuously performed in sequential order from the channel defined by the scan list. Within a group of channels, the interval between conversions is fixed at 14.976µ seconds. The group conversion interval is controlled by the interval timer (Timer Prescaler and Conversion Timer).

Burst modes can be used to provide pseudo-simultaneous sampling for many low to medium speed applications requiring simultaneous channel acquisition. The 14.976µ seconds between conversions of each channel can essentially be considered simultaneous sampling for low to medium frequency applications.

After software selection of the burst continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

Stopping the execution of burst continuous conversions is accomplished by writing 000 to the Scan Mode bits (10-8) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

Interrupts can be enabled to activate after conversion of a group of channels as defined by the entries in the Scan List FIFO. If interrupts are configured to go active after the completion of a group of channels, the interrupt will be issued 23µ seconds after conversion of the last channel in the group has started.

Burst Single-Mode

In burst single mode of operation conversions are performed once for all channels in the scan list. The interval between conversions of each channel is

fixed at 14.976µ seconds. The interval timer has no functionality in this mode of operation.

After software selection of the burst single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

Interrupts can be enabled to activate after the group of channels as defined by the Scan List has been digitized. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 23µ seconds after conversion of the last channel has started.

When burst single operations are run back to back with less than 7µ seconds between the previous burst and the start of a new burst signal operation, software must issue a scan disable command before issuing burst single mode and a start convert. This will prevent erroneous operation of the next burst signal operation.

Convert On External Trigger Only-Mode

In convert on External Trigger Only Mode of operation each conversion is initiated by an external trigger (falling edge of a logic low pulse) input to the AP323 on the EXT TRIGGER* signal of the front panel field I/O connector. Conversions are performed for each channel in the scan list. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation.

The external trigger signal must be configured as an input for this mode of operation. The external trigger can be configured as an input by setting bits 2 and 1 of the Control register to “01”.

At least 5µ seconds of data acquire time should be provided after programming the Control register or writing the first entry in the scan list before the first external trigger is issued. These configuration registers control the AP323 on board multiplexers to select the channel that is input to the converter.

In the external trigger only mode, it is important to understand the sequence in which converted data is transferred from the ADC to the sample FIFO. Upon an external trigger the selected analog signal is converted but remains at the ADC while the previous digitized value is output from the ADC to the sample FIFO. Thus, with this sequence the FIFO is consistently updated with the previous cycle’s converted data. In other words, new data in the FIFO is one cycle behind the ADC. With this sequence, at the end of data conversions, one additional external trigger is required to move the data from the ADC to the FIFO. At the start of data conversion, with the first external trigger signal

(given the Start Convert Bit is set), data is not input to the FIFO since the data in the ADC buffer is old convert data.

The AP323 requires the setting of the Start Convert bit to logic one prior to receiving the first active external trigger pulse. This will prevent erroneous data from being written into the FIFO corresponding to the first channel converted. This is the only mode of operation in which the Start Convert bit does not cause data conversions.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the scan list. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued 8µ seconds after a valid external trigger pulse is detected. The only exception to this is upon the very first external trigger pulse, no interrupt will be issued since data is not written to the FIFO. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 8µ seconds after detection of the first external trigger following conversion of all channels in the selected group. Again, one extra external trigger is needed to complete update of the FIFO for the selected group of channels.

External Trigger Only mode of operation can be used to synchronize multiple AP323 modules to a single AP323 running in uniform continuous, uniform single, burst continuous, or burst single mode. The external trigger, of the AP323 running uniform or burst mode, must be programmed as an output. The external trigger signal of that AP323 must be connected to the external trigger signals of all other AP323s (programmed for external trigger input) that are to be synchronized. These other AP323s must be programmed for External Trigger Only Mode. Data conversion can then be started by writing high to the Start Convert bit of the AP323 configured for Uniform or Burst mode.

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The AP323 provides different methods of analog input acquisition to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided for use to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Software calibration uses some fairly complex equations. Acromag recommends purchase of our Windows, Linux, or VxWorks software to make communication with the board and calibration easy. It relieves you from

having to turn the equations in the following sections into debugged software calibration code.

Uncalibrated Performance

The uncalibrated performance is affected by one primary error source, the Analog to Digital Converter (ADC). The untrimmed ADC has significant offset and gain errors (see specifications in SPECIFICATIONS) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the AP323 can be accomplished by using calibration voltages present on the board. The four voltages and the analog common reference are used to determine two points of a straight line which defines the analog input characteristic. The exact value of the four reference voltages is stored in on board memory to provide the most accurate calibration. See Table 23 and the Flash Data and Chip Select registers for details regarding reading calibration coefficients.

The calibration voltages are used with the auto zero signal to find two points that determine the straight line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in Table 24.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected\_Count} = \left[\frac{65536 * m}{\text{Ideal\_Volt\_Span}}\right] * \left[Count\_Actual + \frac{Volt_{CALLO} - Ideal\_Zero}{m} - Count_{CALLO}\right] \quad (1)$$

where, "**m**" represents the actual slope of the transfer characteristic as defined in equation 2:

$$m = \left[\frac{Volt_{CALHI} - Volt_{CALLO}}{Count_{CALHI} - Count_{CALLO}}\right] \quad (2)$$

$Volt_{CALHI}$	=	High Calibration Voltage (See Table 24)
$Volt_{CALLO}$	=	Low Calibration Voltage (See Table 24)
$Count_{CALHI}$	=	Actual ADC Data Read with High Calibration Voltage Applied
$Count_{CALLO}$	=	Actual ADC Data Read with Low Calibration Voltage Applied

Ideal_Volt_Span	=	Ideal ADC Voltage Span (See Table 25)
Count_Actual	=	Actual Uncorrected ADC Data for Input Being Measured
Ideal_Zero	=	Ideal ADC Input for "Zero" (See Table 25)

Table 24 Recommended Calib. Voltages for Input Ranges

Input Range (Volts)	Rec. Low Calib. Voltage "$Volt_{CALLO}$" (Volts)	Rec. High Calib. Voltage "$Volt_{CALHI}$" (Volts)
-5 to +5	0.0000 (Auto Zero)	4.94
-10 to +10	0.0000 (Auto Zero)	9.88
0 to+5	1.235	4.94
0 to +10	1.235	9.88

Table 25 Ideal Voltage Span and Zero for Input Ranges

Input Range (Volts)	"Ideal_Volt_Span" (Volts)	"Ideal_Zero" (Volts)
-5 to +5	10.0000	-5.0000
-10 to +10	20.0000	-10.0000
0 to +5	5.0000	0.0000
0 to +10	10.0000	0.0000

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) for each active input range should not be determined immediately after startup but after the module has reached a stable temperature and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 64) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

Calibration Programming Example 1

Assume that the desired input range is -10 to +10 volts (select desired input range via hardware switch on module). Channels 0 to 3 are connected differentially, and corrected input channel data is desired. From Table 24 & Table 25 several calibration parameters can be determined:

$Volt_{CALHI}$ = 9.88 volts (From Table 24)
$Volt_{CALLO}$= 0.0000 volts (Auto Zero; From Table 24)
Ideal_Volt_Span = 20.0000 volts (From Table 25)
Ideal_Zero = -10.0000 volts (From Table 25)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Write 0439H to Control Register at Base Address + 08H.
    a. Select Straight Binary
    b. External Trigger Disabled
    c. Auto Zero Calibration Voltage
    d. Burst Single Scan Mode
    e. Timer Disabled
    f. Interrupts Disabled
2. Write 0006H to the Trigger / FIFO Clear Register at Base Address + 28H to clear the Scan List FIFO and the Sample FIFO.
3. Write 0000H to Scan List FIFO at Base Address + 14H thirty-two times. This will permit thirty-two conversions of the Auto Zero value to be stored in the Sample FIFO.
4. Wait at least 5µ seconds before the Start Convert bit is set to allow the input signal to settle.
5. Write 0001H to the Trigger / FIFO Clear register at Base Address + 28H. This starts the burst single mode of conversions. Thirty-two conversions of the Auto Zero are stored in the Sample FIFO.
6. Read the thirty-two values from the Sample FIFO at Base Address + 20H.
7. Take the average of the thirty-two ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

1. Write 0419H to Control Register at Base Address + 08H.
    a. Select Straight Binary
    b. External Trigger Disabled
    c. Select 9.88 Calibration Voltage
    d. Burst Single Scan Mode
    e. Timer Disabled
    f. Interrupts Disabled
2. Writing the Scan List FIFO is not necessary if it has not been changed from that programmed in steps 2 and 3 above.
3. Wait at least 5µ seconds before the Start Convert bit is set to allow the input signal to settle.

4. Write 0001H to the Trigger / FIFO Clear register at Base Address + 28H. This starts the burst single mode of conversions. Thirty-two conversions of the 9.88 Volt calibration voltage are stored in the Sample FIFO.

5. Read the 32 values from the Sample FIFO at Base Address + 20H.

6. Take the average of the 32 ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual_slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range (i.e. -10 to +10 volts). Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 0 to 3 Differentially and Correct

1. Write 0401H to the Control Register at Base Address + 08H.
    a. Select Straight Binary
    b. External Trigger Disabled
    c. All Channels Differential Input
    d. Burst Single Scan Mode
    e. Timer Disabled
    f. Interrupts Disabled
2. Write 0006H to the Trigger / FIFO Clear Register at Base Address + 28H to clear the Scan List FIFO and the Sample FIFO.

3. Write 0000H, 0001H, 0002H, 0003H to the Scan List FIFO at Base Address + 14H. This will permit conversions of channels 0 to 3.

4. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

5. Write 0001H to the Trigger / FIFO Clear Register at Base Address + 28H. This starts the burst single mode of conversions. Conversions of channels 0 to 3 are stored in the Sample FIFO at Base Address + 20H.

6. Read the four samples from the Sample FIFO at Base Address +20H. The data represents the uncorrected “Count_Actual” term in equation 1. Since all parameters on the right hand side of equation 1 are known, calculate the calibrated value “Corrected_Count”. This is the desired, corrected value. Repeat this procedure for each of the channels.

7. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

Calibration Programming Example 2

Assume that the desired input range is 0 to +5 Volts (selection of the desired input range is implemented via hardware switch on module). Channels 3 to 13 are connected single ended, and corrected input channel data is desired. The calibration voltages are converted using burst single mode (for quick conversion of the calibration voltages) while the actual data will be converted using uniform single mode. From Table 24 and Table 25, several calibration parameters can be determined:

Preselect 0 to 5V ADC Range via switches.
$Volt_{CALHI}$ = 4.94 Volts (From Table 24)
$Volt_{CALLO}$ = 1.235 Volts (From Table 24)
Ideal_Volt_Span = 5.0000 volts (From Table 25)
Ideal_Zero = 0.0000 volts (From Table 25)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Write 0431H to the Control Register at Base Address + 08H.
    a. Select Straight Binary
    b. External Trigger Disabled
    c. Select 1.2350v Calibration Voltage
    d. Burst Single Scan Mode
    e. Timer Disabled
    f. Interrupts Disabled
2. Write 0006H to the Trigger / FIFO Clear Register at Base Address + 28H to clear the Scan List FIFO and the Sample FIFO.
3. Write 0000H to Scan List FIFO at Base Address + 14H thirty-two times. This will permit thirty-two conversions of the Auto Zero value to be stored in the Sample FIFO.
4. Wait at least 5µ seconds before the Start Convert bit is set to allow the input signal to settle.
5. Write 0001H to the Trigger / FIFO Clear Register at Base Address + 28H to start burst single mode conversions. Thirty-two conversions of the calibration voltage are stored in the Sample FIFO.
6. Read the thirty-two values from the Sample FIFO at Base Address + 20H.
7. Take the average of the thirty-two ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

8. Write 0421H to the Control Register at Base Address + 08H.
    g. Select Straight Binary
    h. External Trigger Disabled
    i. Select 4.9400 Calibration Voltage
    j. Burst Single Scan Mode
    k. Timer Disabled
    l. Interrupts Disabled
9. Writing the Scan List FIFO is not necessary if it has not been changed from that programmed in steps 2 and 3 above.
10. Wait at least 5µ seconds before the Start Convert bit is set to allow the input signal to settle.
11. Write 0001H to the Trigger / FIFO Clear Register at Base Address + 28H. This starts a burst single mode of conversions. Thirty-two conversions of the 1.235 calibration voltage are stored in the Sample FIFO.
12. Read the thirty-two values from the Sample FIFO at Base Address + 20H.
13. Take the average of the thirty-two ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range. Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 3 to 13 Single Ended and Correct Using Uniform Single Mode

1. Write 0A09H to the Control Register at Base Address + 08H.
    a. Select Straight Binary
    b. External Trigger Disabled
    c. Select Single Ended Input
    d. Uniform Single Scan Mode
    e. Timer Enabled
    f. Interrupts Disabled
2. Write 0006H to the Trigger / FIFO Clear Register at Base Address + 28H to clear the Scan List FIFO and the Sample FIFO
3. Write the eleven channel numbers 3 thru 13 to the Scan List FIFO at Base Address + 14H. This will permit conversions of channels 3 to 13.
4. Write 0050H to the Timer Prescaler at Base Address + 0CH. This sets the Timer Prescaler to 80 decimal.

5. Write 0008H to the Conversion Timer at Base Address + 10H. This Conversion Timer value in conjunction with the Timer Prescaler sets the interval time between conversions to (80 ∗ 8) * 0.128 μS = 81.92 μS.

6. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

7. Write 0001H to the Trigger / FIFO Clear Register at Base Address + 28H. This starts the uniform single mode of conversions. Conversions of channels 3 to 13 are stored in the Sample FIFO.

8. Read the 11 values from the Sample FIFO at Base Address + 20H. The data represents the uncorrected "Count Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. The calibrated value "Corrected Count" can be calculated for each of the channels.

9. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

Error checking should be performed on the "Corrected Count" value to make sure that calculated values below 0 or above 65,535 are restricted to those end points. Note that the software calibration cannot recover signals near the end points of each range which are clipped off due to the uncalibrated hardware (e.g. ADC) or power supply limitations.

See the specifications in Section 6 for details regarding the maximum corrected (i.e. calibrated) error.

Programming Interrupts

Interrupts can be enabled for generation after conversion of individual channels or after a group of channels have been converted. Interrupts generated by the AP323 use interrupt request line INTA#. The interrupt release mechanism is release on register access. That is, the AP323 will release the INTA# signal when bit-15 of the Interrupt Register at Base Address + 00H is set to logic "1".

Interrupt Programming Example

1. Enable AP323 board interrupt by writing a "1" to bit 0 of the Interrupt register at Base Address + 00H.

2. Enable the AP323 for interrupt after each channel or after conversion of a group of channels by setting bits 12 or 13 of the Control register (at Base Address + 08H) as required.

3. Interrupts can now be generated after start of a scan mode of operation (burst, continuous, or external trigger only).

General Sequence of Events for Processing an Interrupt

1. The AP323 asserts the Interrupt Request Line (INTA#) in response to an interrupt condition.
2. Determine the IRQ line assigned to the AP323 during system configuration (read configuration register number 15).
3. Set up the system interrupt vector for the appropriate interrupt.
4. Unmask the IRQ in the system interrupt controller.
5. The interrupt service routine pointed to by the vector set up in step 3 starts.
6. Interrupt service routine determines if the AP323 has a pending interrupt request by reading the Interrupt pending bit-1 of the Interrupt register.
7. Example of Generic Interrupt Handler Actions:
    a. Disable the interrupting AP323 by writing “0” to bit-0 of the Interrupt Register to disable interrupts on the AP323.
    b. Service the interrupt by reading converted data resident in the sample FIFO of the AP323. Use the Sample FIFO Count register to determine the number samples to read.
    c. Clear the interrupt request by writing a “1” to bit-15 of the Interrupt register.
    d. Enable the AP323 for interrupts by writing “1” to bit-0 of the Interrupt register.
8. Write “End-Of-Interrupt” command to the system’s interrupt controller.
9. If the AP323’s interrupt stimulus has been removed, the interrupt cycle is completed and the board holds the INTA# inactive.

4. THEORY OF OPERATION

This section contains information regarding the hardware of the AP323. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Figure 1 as you review this material.

FIELD ANALOG INPUTS

The field I/O interface to the AP323 is routed through the AcroPack carrier. **Field I/O signals are NON-ISOLATED.** This means that the field return and

logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operational errors, and with extreme abuse, possible circuit damage. Refer to Figure 3 and Figure 4 for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. AP323 control logic automatically programs the multiplexers for selection of the required analog input channel. The required control is based upon selection of single ended or differential analog input and the channels in the scan list FIFO.

Single ended and differential channels cannot be mixed (i.e. they must all be single ended or differentially wired). Up to 40 single ended inputs can be monitored, where each channel's + input is individually selected along with a single sense lead for all channels. Up to 20 differential inputs can be monitored, where each channel's + and - inputs are individually selected.

The output of the multiplexer is buffered by an instrumentation amplifier with a gain of one. The instrumentation amplifier drives the ADC (Analog to Digital Converter). The ADC is a 16-bit, successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then it returns to sample mode to acquire the next channel. Once a conversion has been started, control logic on the AP323 automatically updates the multiplexer for the next channel to be converted as required. This allows the input to settle for the next channel while the previous channel is converting. This pipelined mode of operation facilitates maximum system throughput.

A miniature DIP switch on the board controls the range selection for the ADC (-5 to +5, -10 to +10, 0 to 5, and 0 to 10 Volts) as detailed in Table 1. DIP switch selection should be made prior to powering the unit. Thus, all channels will use the same ADC range.

The board contains four precision voltage references and a common (auto zero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for the desired ADC range.

CARRIER INTERFACE

The interface to the carrier board is made by a 52-pin Mini-PCIe connector (see Table 3) and a 100 pin Samtec board stacking connector (see Table 2). These connectors also provide +5V and ±12V power to the module. Note that the signals in bold italic are not used.

A Field Programmable Gate-Array (FPGA) on the AcroPack Module provides an interface to the carrier board per PCIe. The interface to the carrier board allows complete control of all AP323 functions.

PCIe INTERFACE LOGIC

The PCIe interface is imbedded within the FPGA. This interface includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCIe endpoint uses a single 4K base address register. The AP323 logic also implements interrupt requests via interrupt line INTA#.

AP323 CONTROL LOGIC

All logic to control data acquisition is imbedded in the FPGA. The control logic of the AP323 is responsible for controlling the operation of a user specified sequence of data acquisitions. Once the AP323 has been configured, the control logic performs the following:

- Controls the channel multiplexers based upon the scan list FIFO values, and single ended or differential analog input mode.
- Controls data conversion at the ADC based on one of five different scan modes of operation.
- Controls data transfer from the ADC to the FPGA's 16-bit serial shift register.
- Controls and updates the Sample FIFO, Sample FIFO count, and Sample FIFO status registers.
- Stops data acquisition for Single Cycle Scan modes.
- Provides external or internal trigger control.
- Controls the interval between data conversions.
- Issues interrupt requests to the host.

SCAN LIST FIFO

A FIFO in the FPGA is used to store a list of channels to sample during a scan. Analog multiplexers route the analog signal for the current channel to the instrumentation amplifier and the ADC. The list of channels is digitized in the order they were written to the FIFO.

In the continuous modes of operation the FIFO will continuously cycle, in order, from the first entry to the last, and then sequence repeats. When the continuous mode of operation is halted by disabling the scan mode via the control register, the internal hardware counter remains at the count value reached when halted. Upon start of a new scan, the conversion will resume with the next channel in the list.

A 16-bit serial shift register is implemented in the FPGA. This serial shift register interfaces to the ADC. A clock signal provided by the converter is used to serially shift the new data from the converter to the FPGA's 16-bit serial

shift register. Use of the converter's clock signal (instead of an external clock) minimizes the danger of digital noise feeding through and corrupting the results of a conversion in process.

The converted data serially shifted from the ADC to the FPGA, represents the analog signal digitized in the previous convert cycle. That is, the ADC transfers digitized analog input data to the FPGA one convert cycle after it has been digitized. Serially shifting the 16-bits of digitized data to the FPGA and then writing to the Sample FIFO is completed 8μ seconds after start of the convert cycle.

Upon initiation of an ADC convert cycle, the analog input data is digitized and stored into an internal ADC buffer. Also during this cycle, the last converted data value is moved from the ADC buffer to the FPGA's sample FIFO. Understanding this sequence of events is important when using the External Trigger Only scan mode. The first digitized value received from the ADC in External Trigger Only mode will not be written to the sample FIFO if the Start Convert bit is set prior to issuance of the first external trigger signal. This first value received from the ADC is digitized data that has remained in the ADC's buffer from a previous data acquisition session. Likewise, to update the sample FIFO with the last desired digitized data value one additional convert cycle is required.

For all other scan modes, the FPGA control logic will automatically discard the first digitized data value received from the ADC. It is not written to the sample FIFO. In addition, the FPGA logic also automatically generates the required "flush" convert signals to obtain the last converted data value from ADC.

EXTERNAL TRIGGER

For the Burst and Continuous scan modes the falling edge of the external trigger will start data acquisition which will then be controlled by the FPGA. For External Trigger Only mode, each falling edge of the external trigger causes a conversion at the ADC. Once the external trigger signal has been driven low, it should remain low for a minimum of 500n seconds.

TIMED PERIODIC TRIGGER CIRCUIT

Timed Periodic Triggering is provided by two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by the 7.8125 MHz clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 8.192 μ seconds to 2.139 seconds. The output of the second counter is used to trigger the start of new ADC conversions for the Uniform Scan modes of operation. For the Burst Continuous mode, the interval between conversions of each channel is fixed at 14.976μ seconds. However, the interval of the start

of a burst (one pass through the scan list) can be controlled by the Interval Timer.

INTERRUPT CONTROL LOGIC

The AP323 can be configured to generate an interrupt after completion of conversion of a single channel or after conversion of the last channel in the list is completed. AP323 interrupt signal INTA# is driven active to the carrier/CPU to request an interrupt. Bit-1 of the Interrupt register (at Base Address + 0H) can be read to identify a pending interrupt. The interrupt release mechanism employed is release on register access. The AP323 will release the interrupt request when bit-15 of the Interrupt register (at Base Address + 0H) is set to a logic "1".

5. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

The AP323 is shipped pre-calibrated by Acromag and may be returned at the discretion of the customer to measure the accuracy of the calibration at some defined period. Recalibration, if required, can be performed by the customer if the proper equipment is available to them and is otherwise offered through the Service Department at Acromag for a fee.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes/White Papers
- I/O Questions Answered

Acromag's application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the "I/O Questions Answered" or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6. SPECIFICATIONS

PHYSICAL

Height.....4.6 mm (0.179 in).
Length .....70.0 mm (2.874in).
Width .....30.0 mm (1.181 in).
Board Thickness .....1.0 mm (0.039 in).
Field I/O Connector.....100-pin, ST5-50-1.50-L-D-P-TR Samtec connector.
Power.....

Power Supply	Typical	Max
+3.3V	400 mA	500 mA
+5V	20 mA	30 mA
+12V	0.7 mA	1.4 mA
-12V	0.7 mA	1.4 mA

ENVIRONMENTAL

Operating Temperature.....-40 to +85°C (with 400 LFM airflow)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +100°C
Non-Isolated .....Logic and field commons have a direct electrical connection.

EMC Compliance

The AcroPack complies with EMC Directive 2004/108/EC.
Immunity.....per EN 61000-6-2
Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
Radiated Field Immunity (RFI), per IEC 61000-4-3
Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
Surge Immunity, per IEC 61000-4-5
Conducted RF Immunity (CRFI), per IEC 61000-4-6

Emissions .....per EN61000-6-4
Enclosure Port, per CISPR 16
Low Voltage AC Mains Port, per CISPR 16
Note: This is a Class A product

Note:
Reference Test Conditions: Differential inputs, all channels, Temperature 25°C, using a 2 meter shielded cable length connection to the field analog input signals.

Vibration and Shock Standard

The AcroPack is designed to comply with the following Vibration and Shock standards.
Vibration, Sinusoidal Operating ...Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating .....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating.....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

Reliability Prediction

AP323E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,965,741	224.4	508.7
40°C	1,046,028	119.4	956.0

[1] FIT is Failures in 10^9 hours.

ANALOG INPUTS

Input Channels (Field Access) .....40 Single-ended or 20 Differential via 50-pin front panel connector
Analog Input Data Buffer.....32 16-bit Registers
Input Signal Type .....Voltage (Non-isolated).
Input Ranges (DIP switch selectable):
Bipolar -5 to +5 Volts
Bipolar -10 to +10 Volts
Unipolar 0 to +5 Volts
Unipolar 0 to +10 Volts
Input Resistance.....1 MΩ, Typical.
Input Bias Current.....1nA, Typical
Input Overvoltage Protection .....- 32 V to + 52 V with Power ON
-35 V to +55 Volts Power OFF
Common Mode Voltage Range.....± (I Vs I – 2.5) Volts, Typical
Common Mode Rejection Ratio (60Hz)
96 dB Typical

Channel to Channel Rejection Ratio (60Hz)
96 dB Typical
ADC .....TI ADS8509IBDB
A/D Resolution.....16-bits.
Data Format .....Binary 2's Complement and Straight Binary
No Missing Codes.....No Missing Codes 15 bits ADC
A/D Integral Linearity Error.....±1 LSB Typical
±3 LSB Maximum
Unipolar Zero Error .....±10mV Maximum for 0-10V Range
±10mV Maximum for 0-5V Range
Bipolar Offset Error.....±10mV Maximum, for ±10V Range
±10mV Maximum for ±5V Range.
Full Scale Error .....±0.5% Maximum

Note:

Software calibration minimizes these error components.

Settling Time (20V step).....3.5 µS to 0.01%, Typical
A/D Conversion Time .....8.192 µS Maximum
Conversion Rate.....122 KHz Maximum
Recommended Conversion Rate ...67 KHz
Recommended Source Impedance
Maximum 75 Ohms for rated accuracy at maximum sample rate
A/D Triggers .....External and Software
Input Noise.....1.8 LSB rms, Typical. ±5V input range
Temperature Coefficient.....See spec. of calibration voltages

Programmable Calibration Voltages

Calibration Signal	Ideal Value (Volts)	Maximum Tolerance @25°C (Volts)	Maximum Temperature Drift[1] (ppm/°C)
Auto Zero	0.0000	±0.000150	0
CAL0	9.8800	±0.000228	±6
CAL1	4.9400	±0.000228	±11
CAL2	2.4700	±0.000228	±11
CAL3	1.2350	±0.000228	±11

Note:

1. Worst case temperature drift is the sum of the ±6 ppm/°C * drift of the calibration voltage reference plus the ±5 ppm/°C drift of the resistors in the voltage divider.

Maximum Overall Calibrated Error @ 25°C

The maximum corrected (i.e. calibrated) error is the worst case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C.

Input Range (Volts)	ADC Range (Volts)	Max Err[1,2,3,4] ±LSB (% Span)	Typ. Err[1,2,3,4] ±LSB (% Span)
-5 to +5	-5 to +5	±8.6 LSB (0.013%)	±4 LSB (0.006%)
-10 to+10	±10	±9.4 LSB (0.014%)	±3 LSB (0.005%)

Note:

1. A total of 64 input samples, autozero values, and calibration voltages were averaged with a throughput Rate of 67 kHz conversions/second. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. For critical applications multiple input samples should be averaged to improve performance. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.
2. Reference Test Conditions: Differential inputs, all channels, Temperature 25°C, 61 K conversions/second, with a 2 meter shielded cable length connection to the field analog input signals.
3. A total of 2048 input samples were taken statistically, assuming a normal distribution, to determine the RMS value.
4. Accuracy may be further improved by increasing the time between conversions (e.g. from 15µ seconds to 30µ seconds).

External Trigger Input/Output

As an Input:.....Must be an active low 3.3 Volt logic TTL compatible, debounced signal referenced to analog common. Conversions are triggered on the falling edge of this trigger signal. Minimum pulse width 500n seconds.

As an Output:.....Active low 3.3 Volt logic TTL compatible output is generated. The trigger pulse is low for a maximum of 500n seconds.

PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\,Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

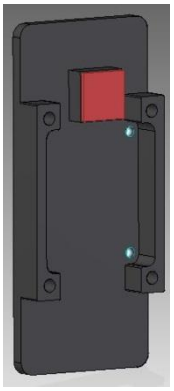
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

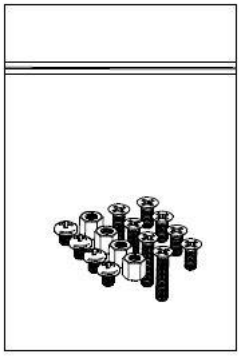
7. APPENDIX

AP-CC-01 Heatsink Kit Installation



Bottom view

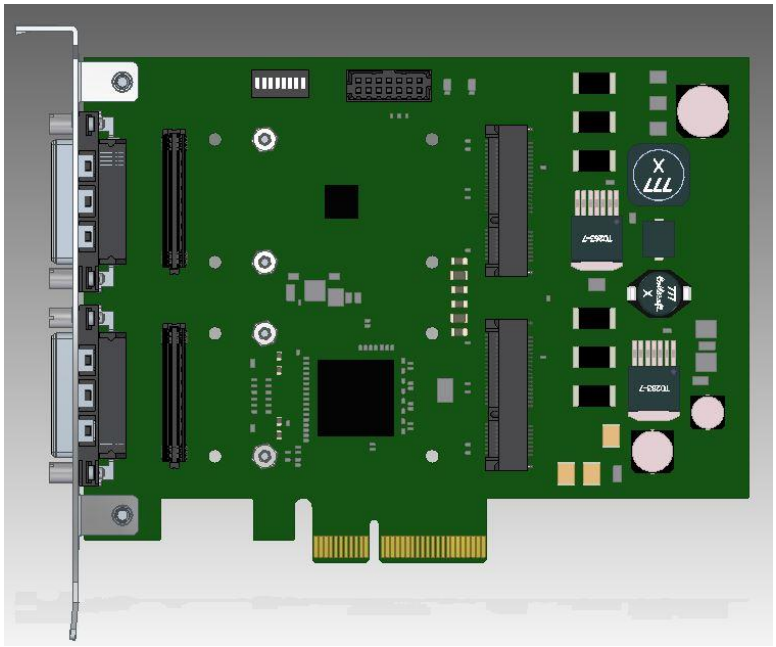
Top view



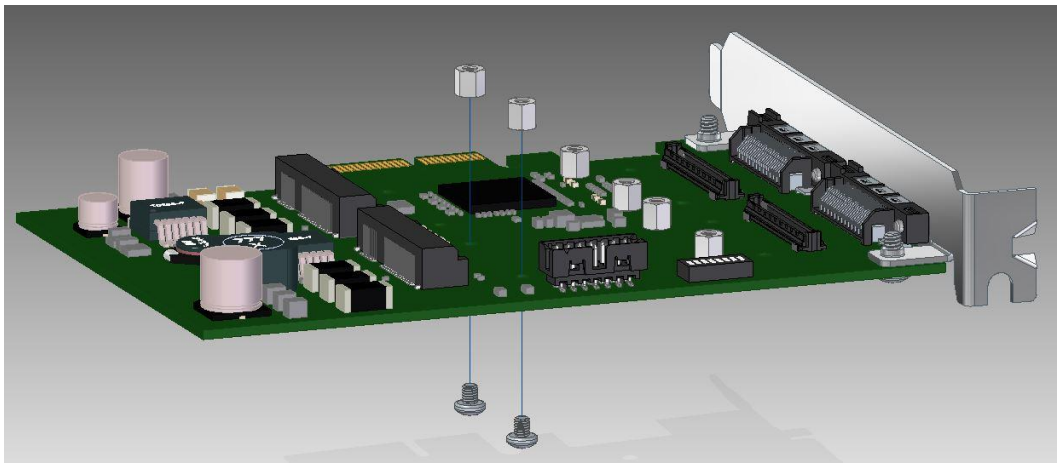
Hardware

AP-CC-01 Heat Sink Kit

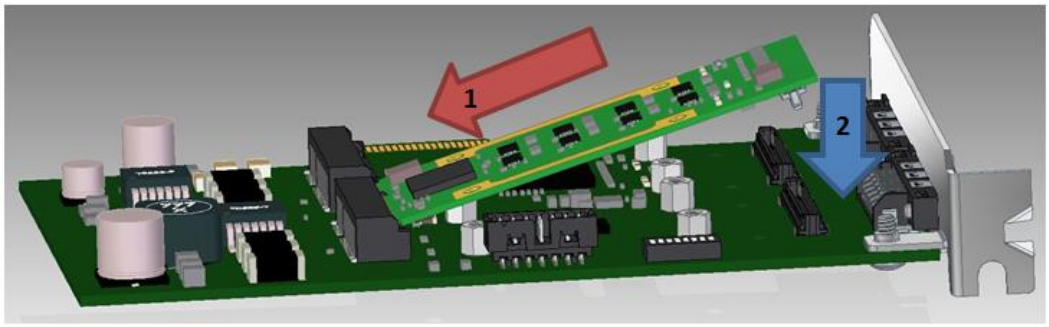
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



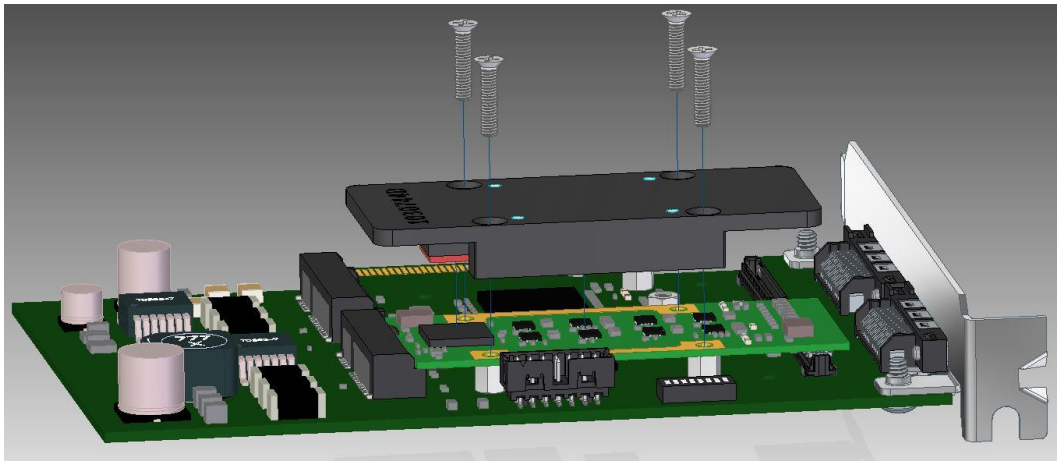
1. Install two standoffs and secure with two screws.



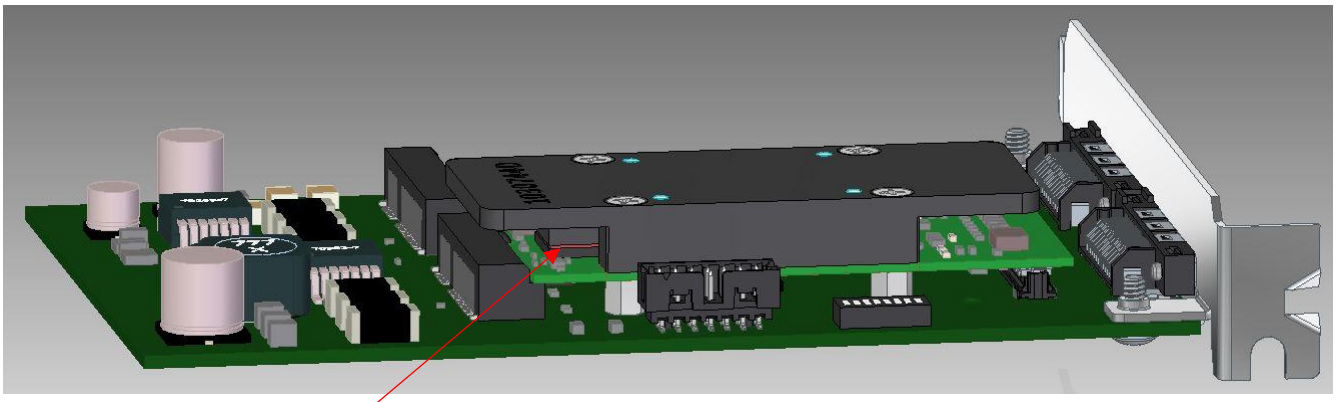
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

8. Certificate of Volatility

Acromag Model AP323E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks	Size: 16,640 Logic Cells	User Modifiable ■ Yes □ No	Function: FPGA logic blocks	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.) FPGA based RAM	Size: 25 x 36-Kbit	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Power Down
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type (EEPROM, Flash, etc.) Flash	Size: 32 Meg x 1bit	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Erase using JTAG
Type (EEPROM, Flash, etc.) Security Registers in Flash device	Size: 1 K bytes	User Modifiable □ Yes ■ No	Function: Writing to the security registers has been disabled by writing the OTP lock registers with zeroes	Process to Sanitize: Not applicable
Acromag Representative				
Name:	Title: Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

9. Revision History

The revision history for this document is summarized in the table below.

Release Date	Version	EGR/DOC	Description of Revision
21 NOV 2016	A	JCL/MJO	Initial Release
11 JAN 2018	B	LMP/MJO	Added PCIe Bus Data Rates Table, Section 6.
27 JAN 2018	C	LMP/MJO	Added Reliability Prediction MTBF Table
20 NOV 2019	D	LMP/ARP	Corrected error on page 17.
19 JUL 2021	E	LMP/AMM	Correct Burst conversion time from 15us to 14.976us