DETAILED SYLLABI OF ALL SUBJECTS (3rd Semester onwards)

DEPARTMENT: COMPUTER SCIENCE AND ENGINEERING
COURSE CODE: CSPC-201
COURSE TITLE: DIGITAL CIRCUITS AND LOGIC DESIGN
COURSE DESIGNATION: REQUIRED
PRE-REQUISITES: NONE
CONTACT HOURS/CREDIT SCHEME: (L-T-P-C: 3-0-0-3)
COURSE ASSESSMENT METHODS: Two sessional exams and one end-semester exam, along with assignments, presentations and class tests which may be conducted by the course coordinator ~~in lieu of internal~~ assessment.

COURSE OUTCOMES
After completion of the course, students will be able to:

1. Demonstrate knowledge of binary number, boolean algebra and binary codes.
2. Design, simulate, built and debug complex combinational and sequential circuits based on an abstract functional specification.
3. Analyze combinational systems using standard gates and minimization methods such as karnaugh maps.

Course Outcomes	Program outcomes											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CSPC-201												
CO 1.	H	M	L									
CO 2.	M	M	H	L								
CO 3.	M	H	M	L								

TOPICS COVERED

Basics of Number Systems, Boolean Algebra and Logic Gates

Gate – Level Minimization: The map method, Four-variable map, Five-Variable map, product of sums simplification Don't-care conditions, NAND and NOR implementation other Two-level implementations, Exclusive – Or function, Hardware Description language (HDL).

Combinational Logic: Combinational Circuits, Analysis procedure Design procedure, Binary Adder-Subtractor Decimal Adder, Binary multiplier, magnitude comparator, Decoders, Encoders, Multiplexers, HDL for combinational circuits.

Synchronous Sequential Logic: Sequential circuits, latches, Flip-Flops Analysis of clocked sequential circuits, HDL for sequential circuits, State Reduction and Assignment, Design Procedure**.**

Registers and Counters: Registers, shift Registers, Ripple counters synchronous counters, other counters, HDL for Registers and counters.

Memory, CPLDs, and FPGAs: Introduction, Random-Access Memory, Memory Decoding, Error Detection and correction Read-only memory, Programmable logic Array programmable Array logic, Sequential Programmable Devices.

Asynchronous Sequential Logic: Introduction, Analysis Procedure, Circuits with Latches, Design Procedure, Reduction of state and Flow Tables, Race-Free state Assignment Hazards, Design Example.

TEXT BOOKS, AND/OR REFERENCE MATERIAL

1. DIGITAL DESIGN – Third Edition, M.Morris Mano, Pearson Education/PHI.
2. Digital Principles and Design – Donald D.Givone, Tata McGraw Hill, Edition.
3. John F Wakerly, "Digital Design Principles and Practices 3/e", Pearson Education 2001.
4. J P. Hayes, "Introduction to Digital Logic Design", Addison-Wesley Publishing Co
5. Charles H. Roth, Jr. Fundamentals of logic design, Cengage Learning, New Delhi