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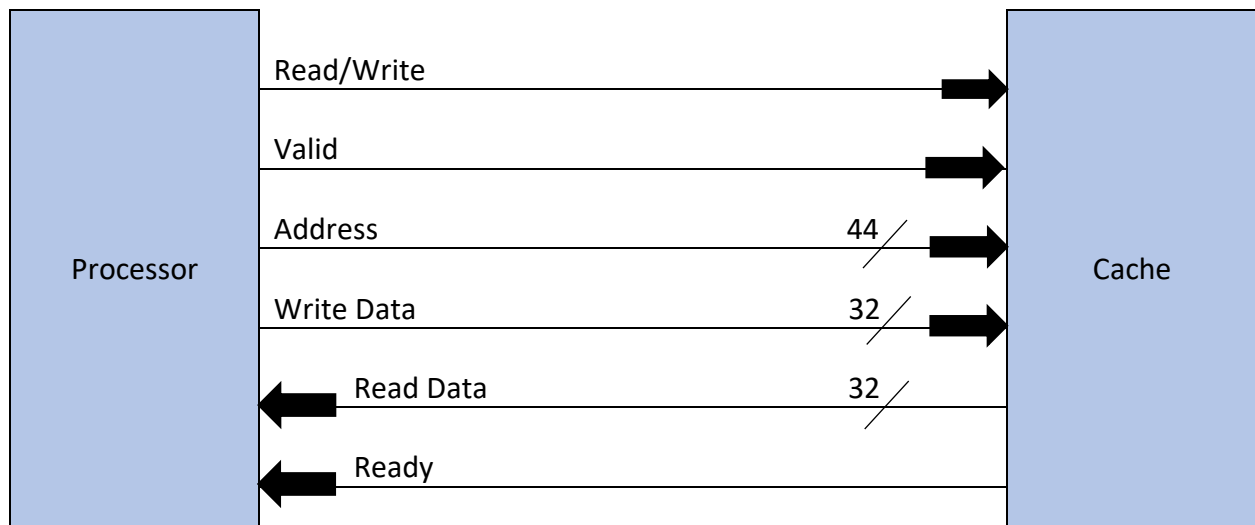
CSCI-B 443

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Project 3

Note: Lowercase b will mean bits and uppercase B will mean bytes.

Part 1: Interface between the processor and cache



Read/Write: Bit to distinguish whether read or write is occurring.

Valid: Bit to signify whether the data in the memory is valid or not.

Address: 44-bit address which goes from the processor to the memory in order to access a specific piece of data (for read or write operations) located at the address specified.

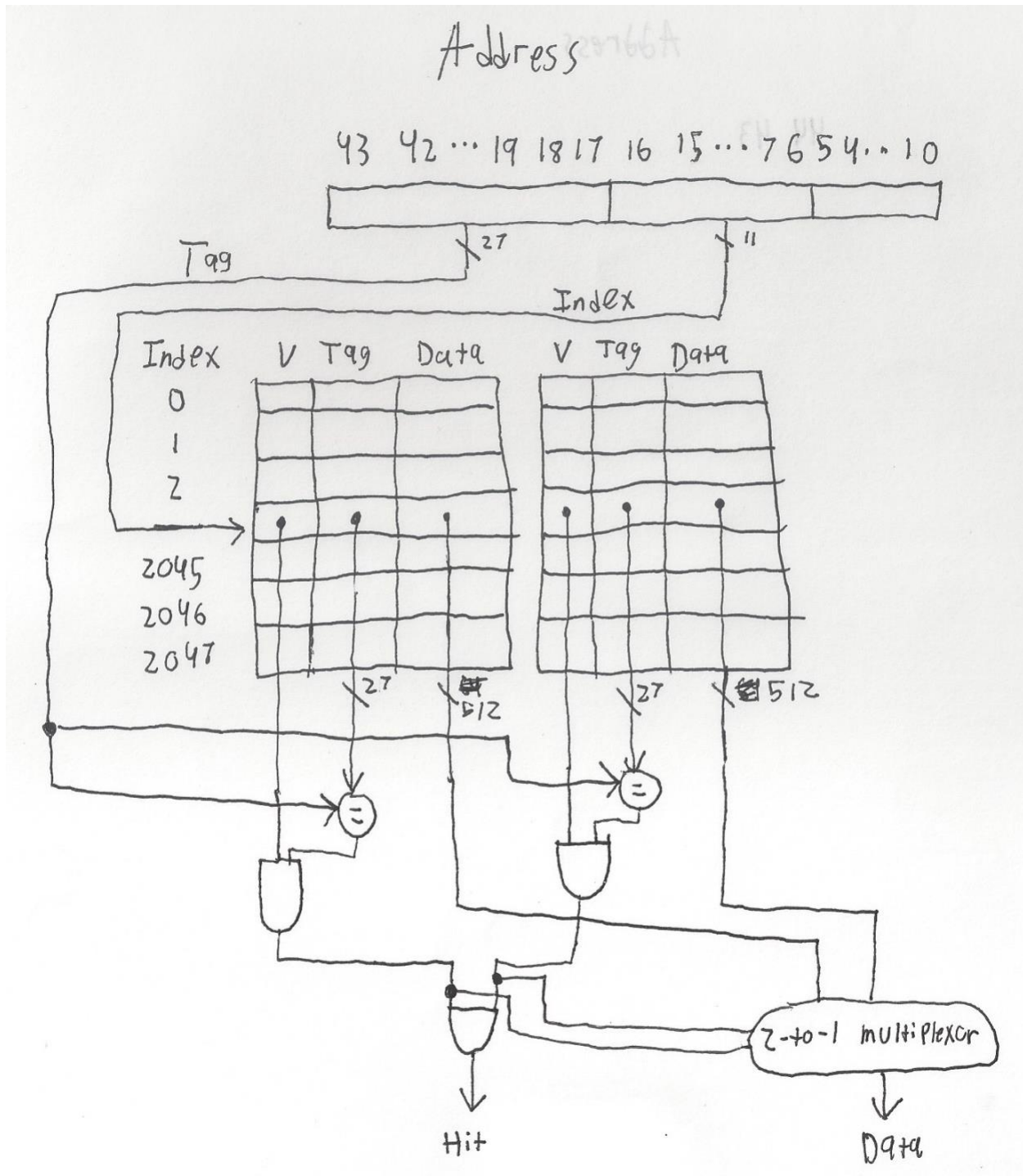
Write Data: The data to write to the memory at the address specified.

Read Data: The data read from the memory at the address specified.

Ready: Bit to distinguish whether or not the data has been fully read or written from the memory. This is necessary to ensure the processor doesn't continue onwards without the memory being fully transferred or written.

Part 2: Design of 2-way set associative cache

Design a 2-way associative cache with the parameters given on the previous page. Present your design in a form of block diagram, like the the one given on the first page.



Total number of bits in the physical memory address:

The total number of bits in the physical memory address is 44 bits.

Number of bits in tag, index and offset fields of the physical memory address:

The number of tag bits is 27 bits.

The number of index bits is 11 bits.

The number of offset bits is 6 bits.

Number of sets in cache:

The number of sets in the cache is $\frac{\text{cache size}}{(2 \cdot \text{block size})} = \frac{256 \text{ kB}}{(2 \cdot 64 \text{ B})} = \frac{2^8 \cdot 2^{11} \text{ B}}{2 \cdot 2^6 \text{ B}} = \frac{2^{18}}{2^7} = 2^{11} \text{ sets}$

Number of tag and data bits per set in cache:

The number of tag and data bits per set in the cache is as follows:

$$\begin{aligned} \# \text{ of data bits per set} &= \frac{\text{total number of data bits in the cache}}{\text{total number of sets}} = \frac{256 \text{ kB}}{2^{11} \text{ sets}} \\ &= \frac{\left((2^8 \cdot 2^{10}) \text{ Byte} \cdot \frac{8 \text{ bits}}{\text{Byte}} \right)}{2^{11} \text{ sets}} = \frac{\left(2^{18} \text{ Byte} \cdot \frac{2^3 \text{ bits}}{\text{Byte}} \right)}{2^{11} \text{ sets}} = \frac{2^{21}}{2^{11}} = 2^{10} \text{ bits} \end{aligned}$$

$$\# \text{ of tag bits per set} = 2 \cdot \# \text{ of bits for tag} = 2 \cdot 27 = 54 \text{ bits}$$

$$\begin{aligned} \# \text{ of tag \& data bits per set} &= \# \text{ of data bits per set} + \# \text{ of tag bits per set} \\ &= 2^{10} + 54 = 54 \text{ kilo bits} \end{aligned}$$

Part 3: Cache size

Total number of data bits in the cache:

The total number of data bits in the cache is given to be 256 kB or $(2^8 \cdot 2^{10}) \text{ Byte} \cdot \frac{8 \text{ bits}}{\text{Byte}} = 2^{18} \text{ Byte} \cdot \frac{2^3 \text{ bits}}{\text{Byte}} = 2^{21} \text{ bits}$ **or 2 mega bits**

Total number of tag bits in cache:

The total number of tag bits in the cache is $(\# \text{ of sets} \cdot 2) \cdot \# \text{ of bits for tag} = 2^{11} \cdot 2 \cdot 27 = 2^2 \cdot 27 \cdot 2^{10} = 108 \cdot 2^{10} = 108 \text{ kilo bits}$

Total number of control bits in cache:

The total number of control bits in the cache is $(2 \text{ bits per set}) \cdot \# \text{ of sets} = 2^{11} \cdot 2 = 2^2 \cdot 2^{10} = 4 \text{ kilo bits}$

Part 4: Cache parameters

Number of blocks in main memory address space:

The number of blocks in the main memory address space is $\frac{2^{\# \text{ of physical address bits}}}{\text{block size}} = \frac{2^{44}}{64} = \frac{2^{44}}{2^6} = 2^{34}$ blocks or $2^4 \cdot 2^{30} = 16$ giga blocks

Number of cache blocks per set:

The number of cache blocks per set is $\frac{256 \text{ kB}}{\text{block size}} = \frac{2^8 \cdot 2^{10}}{2^6} = 2^{12} = 2^2 \cdot 2^{10} = 4$ kilo blocks.

Number of main memory blocks per cache set:

The number of main memory blocks per cache set is $\frac{\# \text{ of blocks}}{\# \text{ of sets}} = \frac{2^{34}}{2^{11}} = 2^{23}$ blocks or $2^3 \cdot 2^{20} = 8$ mega blocks.