B443 Computer Architecture, Spring 2018

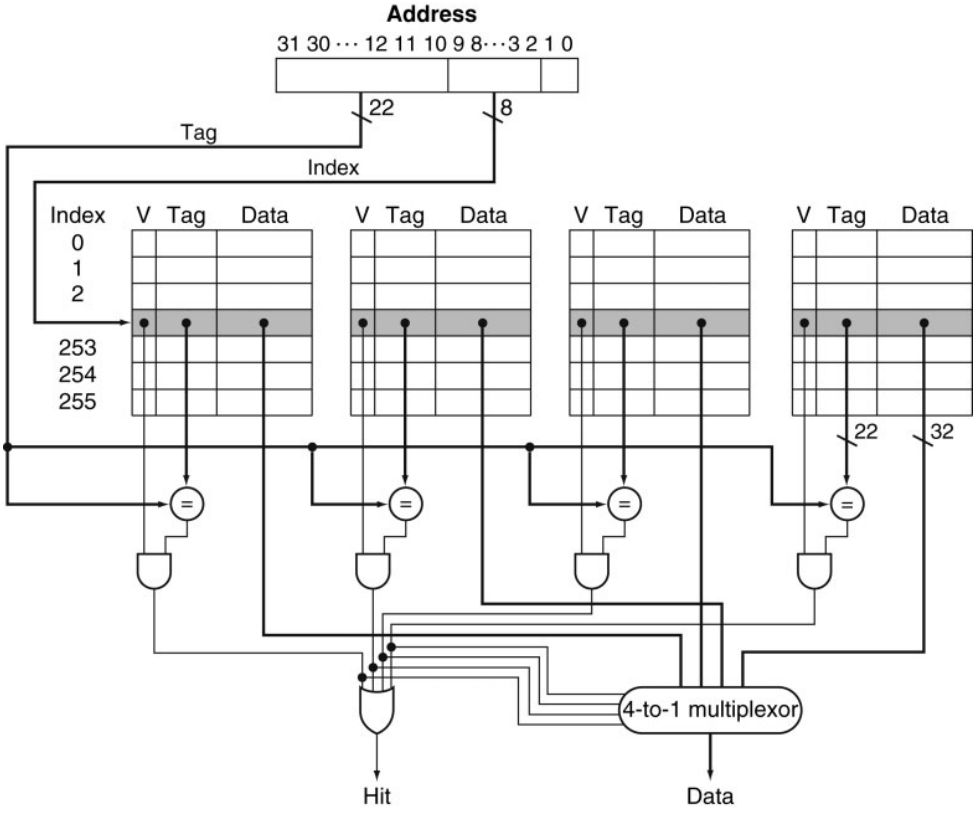
Project #3: Cache Memory Design

Released: Saturday, March 24

Due: Saturday, March 31

Cache Memory

In this project you will design a 2-way associative cache memory for a microprocessor with 44 bit physical memory address. A block diagram of a similar, 4-way cache memory, for a 32-bit microprocessor is given below.



Assume the following parameters relevant for the cache design:

Physical address	44 bits $2^4 \cdot 2^{40} = 16\text{ TB}$
Word size:	32-bit words, byte addressable
Cache size:	256 kB (this is the size of data bits in cache) + tag bits + control bits
Block size:	64 bytes
Control bits:	Valid bit (1)
Size of word:	4 bytes

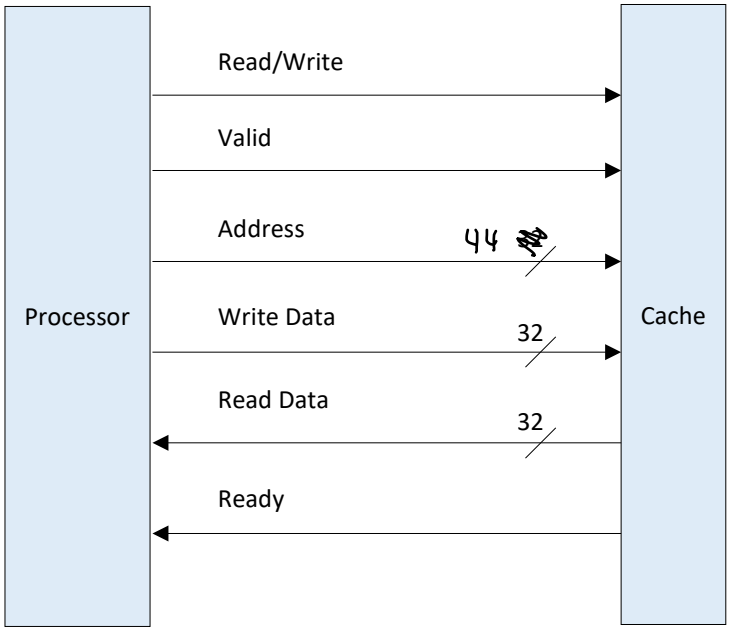
Part 1: Interface between the processor and cache (20 points)

Signals between the processor and cache can be either indvidual (single bit) or multiple signals with the same functionality (called bus, such as address bus), which carry several bits in parallel.

List the signals between the processor to the cache. Describe each signal (individual signals and buses), and give the number of bits.

Draw a block diagram of the processor and cache and indicate the names and direction of the signals. For each signal and each bus indicate the number of bits.

Your diagram should look like the example given in the class, see diagram below, but of course, the number of bits will be different.



Part 2: Design of 2-way set associative cache (40 points)

Design a 2-way associative cache with the parameters given on the previous page. Present your design in a form of block diagram, similar to the one given on the first page.

Calculate and indicate the number of:

Total number of bits in the physical memory address 44 total

Number of bits in tag, index and offset fields of the physical memory address
tag = 27 bits index = 11 bits offset = 6 bits

Numbers of sets in cache
$2^{11} = 2^1 \cdot 2^{10} = 2$ kb

Number of tag and data bits per set in cache
2(tag) = 54 + 2(data)

Show the calculation of the above values.

16 words / block
$2^8 \cdot 2^{10} / 2 = 2^{16}$
$2^{18} / 2^7 = 2^{11}$
4 bits / word

Part 3: Cache size (20 points)

What is the total number of data bits in the cache?
256 kb

What is the total number of tag bits in cache?
$(2^{11} \cdot 2) \cdot 27 = 108$ kb

What is the total number of control bits in cache?
$(2 / \text{block}) \cdot 2^{11} = 2^1 \cdot 2^{11} = 2^2 \cdot 2^{10} = 4$ kb
(↑ blocks)

Part 4: Cache parameters (20 points)

What is the number of blocks in main memory address space?
$2^{44} / 2^{10} = 2^{34}$ ($2^{\text{physical address}} / \text{block size}$)

What is the number of cache blocks per set?
$2^8 / 2^6 = 2^2$ (256 / block size)

What is the number of main memory blocks per cache set?
(# of blocks / # of sets)
$2^{34} / 2^{11} = 2^{23}$