CS107 x86-64 Reference Sheet

Common instructions mov src, dst dst = src movsbl src, dst byte to int, sign-extend		pushsrcadd to top of stack Mem[%rsp] = srcpopdstremove top from stack	
<pre>movzbl src, dst cmov src, reg</pre>	byte to int, zero-fill reg = src when condition holds, using same condition suffixes as jmp	dst = Mem[%rsp++] call fn push %rip, jmp to fn ret pop %rip	
lea addr, dst	dst = addr	Condition codes/flags	
<pre>add src, dst sub src, dst imul src, dst neg dst</pre>	dst += src dst -= src dst *= src dst = -dst (arith inverse)	Zero flagSero flagCero flagCero	
<pre>imulq S mulq S</pre>	<pre>signed full multiply R[%rdx]:R[%rax] <- S * R[%rax] unsigned full multiply</pre>	Addressing modes Example source operands to mov	
marq 3	same effect as imulq	Immediate	
idivq S	signed divide R[%rdx] <- R[%rdx]:R[%rax] mod S	mov <u>\$0x5</u> , dst \$val source is constant value	
divq S unsig	<pre>R[%rax] <- R[%rdx]:R[%rax] / S gned divide - same effect as idivq</pre>	Register	
	dx]:R[%rax] <- SignExtend(R[%rax])	mov <u>%rax</u> , dst %R	
<pre>sal count, dst sar count, dst</pre>	dst <<= count dst >>= count (arith shift)	R is register source in %R register	
shr count, dst	dst >>= count (logical shift)	Direct	
and src, dst	dst &= src	mov <u>0x4033d0</u> , dst	
<pre>or src, dst xor src, dst</pre>	dst = src dst ^= src	0xaddr	
xor src, dst not dst	dst = ~dst (bitwise inverse)	source read from Mem[0xaddr]	
cmp a, b	b-a, set flags	Indirect	
test a, b	a&b, set flags	mov <u>(%rax)</u> , dst	
set dst	sets byte at dst to 1 when condition holds, 0 otherwise, using same condition suffixes as jmp	(%R) R is register source read from Mem[%R]	
	condition caminos as jimp	Indirect displacement	
<pre>jmp label je label jne label js label jns label jg label</pre>	jump to label (unconditional) jump equal ZF=1 jump not equal ZF=0 jump negative SF=1 jump not negative SF=0 jump > (signed) ZF=0 and SF=OF	mov 8(%rax), dst D(%R) R is register D is displacement source read from Mem[%R + D]	
jg label jge label	jump >= (signed) SF=0F	Indirect scaled-index	
jge label jl label	jump < (signed) SF=OF	mov <u>8(%rsp, %rcx, 4)</u> , dst	
jle label	jump <= (signed) ZF=1 or SF!=OF	D(%RB,%RI,S)	
ja label	jump > (unsigned) CF=0 and ZF=0	RB is register for base	
jae label	jump >= (unsigned) CF=0	RI is register for index (0 if empty)	
<pre>jb label jbe label</pre>	jump < (unsigned) CF=1 jump <= (unsigned) CF=1 or ZF=1	D is displacement (0 if empty) S is scale 1, 2, 4 or 8 (1 if empty) source read from: Mem[%RB + D + S*%RI]	

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Registers

%rip Instruction pointer %rsp Stack pointer Return value %rax 1st argument %rdi %rsi 2nd argument %rdx 3rd argument %rcx 4th argument %r8 5th argument %r9 6th argument %r10,%r11 Callee-owned %rbx,%rbp,

%r12-%15 Caller-owned

Instruction suffixes

byte b

word (2 bytes) W

1 long /doubleword (4 bytes)

quadword (8 bytes)

Suffix is elided when can be inferred from operands. e.g. operand %rax implies q,

%eax implies 1, and so on

Register Names

64-bit register	32-bit sub-register	16-bit sub-register	8-bit sub-register
%rax	%eax	%ax	%al
%rbx	%ebx	%bx	%b1
%rcx	%ecx	%cx	%cl
%rdx	%edx	%dx	%dl
%rsi	%esi	%si	%sil
%rdi	%edi	%di	%dil
%rbp	%ebp	%bp	%bpl
%rsp	%esp	%sp	%spl
%r8	%r8d	%r8w	%r8b
%r9	%r9d	%r9w	%r9b
%r10	%r10d	%r10w	%r10b
%r11	%r11d	%r11w	%r11b
%r12	%r12d	%r12w	%r12b
%r13	%r13d	%r13w	%r13b
%r14	%r14d	%r14w	%r14b
%r15	%r15d	%r15w	%r15b