INDIAN INSTITUTE OF INFORMATION TECHNOLOGY UNA
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AY 2023-24
School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test – II
09, Oct.'23
Time: 02:00-03:00PM

Degree	B.Tech.	**Branch**	ECE
Semester	VII		
Subject Code & Name	ECPE52: Application-Specific Integrated Circuit (ASIC)		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	Explain the role of simulation and verification in the IC design flow.	1
1.b	Explain the interconnect architecture used in Altera MAX 5000, 9000, and Xilinx EPLD.	2
1.c	What is meant by iterative system portioning? Explain KL algorithm for system partitioning in detail.	2
2.a	Distinguish between the floor-planning and placement of IC deisgn.	1
2.b	Explain the process for floor-planning using simulated Annealing Algorithm in detail.	2
2.c	List the different types of algorithm used in placement of IC Design. Derive the expression for X and Y components for the zero force target location of forced directed algorithm.	2
3.a	Write the objectives and goals of system partitioning.	1
3.b	Explain the Breuer's algorithm for the placement of IC design with the help of suitable example.	2
3.c	What is global routing? Explain the different type of approaches for this routing.	2
4.a	Explain the difference between top-down and bottom-up approaches in placement of IC design.	1
4.b	How many algorithms are used to perform the grid routing? Explain the Hadlock's Algorithm to optimize the result for grid routing.	2
4.c	How is detailed routing different from global routing? How does the design rule checks (DRC) influence the detailed routing process?	2

**** GOOD LUCK *****