

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY UNA HIMACHAL PRADESH

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Saloh, Una - 177 209

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School of Electronics

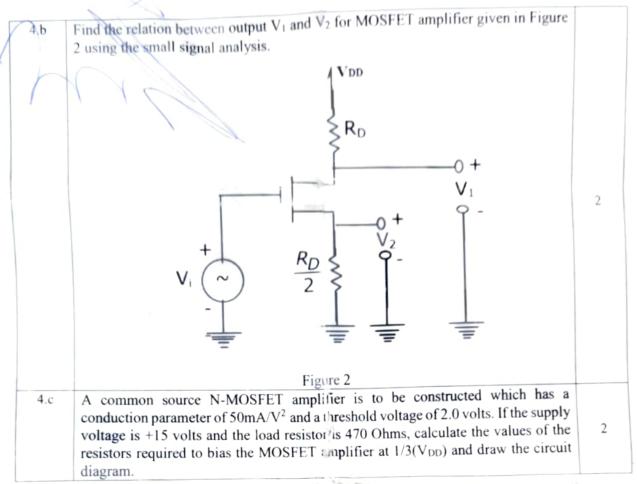
CURRICULUM: IIITUGECE22

Cycle Test - II 09, Oct.'23

Time: 09:00-10:00AM

Degree	B.Tech.	Branch	ECE
Semester	VII	Dianen	LCC.
Subject Code & Name	ECPE42: VI	SI Design	
Time: 60 Minutes		All Questions	Maximum: 20 Marks

Sl. No.	Question	Marks	
l.a	What is the difference between Ratioed and Ratioless logic.		
1.b	Explain why Pseudo NMOS might be preferred in certain applications despite its drawbacks as compared to the CMOS logic? Draw the circuit of 3-input NOR and AND gate with the pseudo NMOS.		
1.c	How is NORA CMOS logic used for pipelined systems? Design the 8-bit input OR gate using the Zipper NORA CMOS logic.		
2.ā	Explain the basic principle of Transmission Gate (TG).		
2.b	Explain the advantage of Domino CMOS over static CMOS. Implement the Boolean function Y=AB'+(C+ D')(E+F)+(G'+H) using Domino CMOS.		
2.c	Enlist the difference between pass transistor and Transmission Gate (TG). Implement the EX-OR and 4×1 Mux function using the TG.		
3.a 3.b	Explain the methods to overcome the charge sharing problem in dynamic CMOS logic.	1	
	Determine values for R_D and R_G for the circuit shown in Figure 1, such that the drain current is 8 mA, V_{DD} =20V, V_{GS} (th)=2.5V, and I_D (on)=5mA at V_{GS} (on)=4V. + V_{DD} R_G Figure 1	2	
3.c	Define the term Logical effort and electrical effort. Determine the W/L ratio of each PMOS and NMOS transistor of 3-input NAND and NOR gate using the Logical effort method.	2	
4.a	Compare and contrast the characteristics of MOSFET amplifier with BJT amplifier.	1	



**** GOOD LUCK *****