



INDIAN INSTITUTE OF INFORMATION TECHNOLOGY

UNA (HP)

An Institute of National Importance under MoE

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AY 2022-23

School of Electronics

End Semester Examination

06, December, '22

2022

Degree	B. Tech.	Branch	ECE
Semester	V		
Subject Code & Name	ECPE22: Modelling and Testing of Digital Systems (VHDL)		
Time: 180 Minutes	Answer All Questions		Maximum: 100 Marks

Q. No.		Questions	Marks
1.	a)	Implement the full adder circuit using minimum number of NAND gates and write down VHDL code using structural modeling.	[5]
	b)	Describe in detail about various design units of VHDL language.	[5]
	c)	Implement 2 to 4 decoder using 1x4 demultiplexer and write down VHDL code using structural modeling.	[5]
	d)	Write down truth table and VHDL code to implement 3-bit asynchronous up counter.	[5]
2.	a)	Draw the circuit and truth table for 8x1 multiplexer and write down VHDL code using case statement.	[5]
	b)	Draw the circuit and write down VHDL code to perform serial in serial out (SISO) operation in universal shift register.	[5]
	c)	Draw the circuit and truth table for 8 to 3 encoder and write down VHDL code using dataflow modeling.	[5]
	d)	Write down truth table and VHDL code to implement BCD down counter.	[5]
3.	a)	Write down VHDL code to implement a 4-bit adder using structural modeling.	[5]
	b)	Describe the various data types used in VHDL language.	[5]
	c)	Draw the circuit and truth table for gray to binary code converter and write down VHDL code using behavioral modeling.	[5]
	d)	Write down VHDL code to implement 1x16 demultiplexer using dataflow modeling.	[5]
4.	a)	Write down truth table and VHDL code to implement a 2-bit comparator using behavioral modeling.	[5]

	b)	Draw the circuit and write down VHDL code for master slave JK flip flop.	[5]
	e)	Describe the various data operators used in VHDL language.	[5]
	d)	Draw the circuit and truth table for full subtractor and write down VHDL code using dataflow modeling.	[5]
5.	a)	Write a VHDL code to implement Decimal-to-BCD Encoder.	[5]
	b)	Describe the different modeling styles in VHDL. What is process statement? How many sequential statements are there inside process statement?	[5]
	c)	Draw the circuit and truth table for D flip flop and write down VHDL code using structural modeling.	[5]
	d)	Describe about subprogram and overloading? What is the difference between Generics and Configuration?	[5]

*****GOOD LUCK*****