INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
UNA [HP]
An Institute of National Importance under MoE
Saloh, Una (HP) – 177 209
Website: www.iiitu.ac.in

AY 2022-23
School of Electronics
Cycle Test – II
14, November.'22

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE22: Modelling and Testing of Digital Systems (VHDL)		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Q. No.		Questions	Marks
1.	a)	What is the basic unit of structural modeling?	[1]
	b)	Write down the VHDL Code for the 3 to 8 decoder using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the D Flip-Flop using structural modeling.	[2]
2.	a)	What is inertial delay?	[1]
	b)	Write down the VHDL Code for the 1X8 multiplexer using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 2 to 4 decoder using structural modeling.	[2]
3.	a)	What is dataflow modeling?	[1]
	b)	Write down the VHDL Code for the full subtractor using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 1X4 multiplexer using structural modeling.	[2]
4.	a)	List the objects of VHDL.	[1]
	b)	Write down the VHDL Code for the binary to gray code converter using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 1-bit comparator using structural modeling.	[2]

*****GOOD LUCK*****