INDIAN INSTITUTE OF INFORMATION TECHNOLOGY UNA
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AY 2023-24

School of Electronics

CURRICULUM: IIITUGECE22

END SEMESTER EXAMINATION

05, Dec'23

Time: 09:00-12:00 hrs.

Degree	B. Tech.	**Branch**	ECE
Semester	VII		
Subject Code & Name	ECPE52: Application-Specific Integrated Circuit (ASIC)		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

Sl. No.	Question	Marks
1.a	What is an ASIC, and how does it differ from other types of integrated circuits? Also, explain the primary categories of ASICs based on their customization levels.	5
1.b	What is a Programmable Logic Devices (PLDs), and how does it differ from other digital devices like microcontrollers and microprocessors? Moreover, describe any four types of PLDs in detail.	5
1.c	Implementing the following Combinational Circuit Using a PLA; I. $F1(A,B,C) = \Sigma m(1,2,3,7)$ II. $F2(A,B,C) = \Sigma m(7,8,9,10,11,12,13,14,15)$	5
1.d	Implementing the following Combinational Circuit Using a PAL; I. $X(A,B,C,D) = \Sigma m(3,5,6,7)$ II. $Y(A,B,C,D) = \Sigma m(0,2,3,4,5,6,7,8,10,11,15)$	5
2.a	What is the purpose of using Hardware Description Languages (HDLs) in digital design? Design the master slave flip flop using the behavioral modeling.	5
2.b	Differentiate between FPGAs and Application-Specific Integrated Circuits (ASICs) in terms of flexibility and development time.	5
2.c	How many inputs and outputs are available in an XC3000 CLB, and how can they be configured to perform different logical functions?	5
2.d	What is the difference between Look Up Table (LUT) and multiplexer (MUX)? Also design the LUT for half subtractor and full adder.	5
3.a	Describe the key steps involved in the ASIC physical design process, from RTL (Register Transfer Level) to the final layout with flow diagram.	5
3.b	List down the four difference between floor-planning and placement of IC deisgn. How can the value of each node be assigned using the hierarchical clustering method of partitioning.	5
3.c	What are the typical considerations and factors that influence the pin assignment of an ASIC? Moreover, explain the nine zero algorithm of pin assignment.	5

3.d	List down the design rule of floor planning. Also, derive the wire length, cost function and dead space of a chip for the floor planning.	5
4.a	Write the objectives and goals of routing. Also, derive the possible objective function to minimize the cost for integer linear programming approach of global routing.	5
4.b	What is grid routing? Discuss the line search algorithm of grid routing with suitable example.	5
4.c	A chip is having four components with their locations on a grid as follows: Component A at (0, 0) Component B at (2, 0) Component C at (4, 0) Component D at (6, 0) A force-directed placement algorithm is applied to minimize the wire length. Calculate the final placement of the components after one iteration, considering only horizontal movement. Assume that there are no initial forces acting on the components.	5
4.d	What is a System-on-Chip (SoC), and how does it differ from traditional microcontrollers or microprocessors? Also, explain the different categories of intellectual property of SoC.	5
5.a	Explain the different types of power dissipation in CMOS logic. Derive the expression of switching power dissipation of CMOS Inverter.	5
5.b	What is low power design? How can the Parallelism and pipeline be used to reduce the power dissipation with a suitable example?	5
5.c	What are some of the key metrics and reports that PowerTheater Analyst can generate to evaluate power consumption in a design?	5
5.d	Explain the different low power techniques to reduce the power dissipation at different abstraction.	5

****** GOOD LUCK *******