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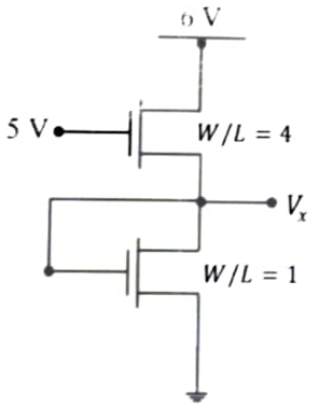
AY 2023-24
School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test – I
14, Aug.'23
Time: 09:00-10:00AM

Degree	B.Tech	**Branch**	ECE
Semester	VII		
Subject Code & Name	ECPE42: VLSI Design		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	A particular junction has C_{J0} = 0.6pF, V_O=0.75V and m=1/3. Find the value of C_J at reverse-bias voltages of 1 V and 10 V.	(1)
1.b	Draw the flow chart of VLSI Design and explain the operation of each step in detail.	(2)
1.c	Explain the working principle of FET. The MOS transistors shown in Figure 1 are having $\mu_n \times C_{ox}$ is 100 $\mu A/V^2$ and the threshold voltage V_{th} is 1 V. Calculate the voltage V_x at the source of the upper transistor.  Figure 1	(2)
2.a	The data sheet for an E-MOSFET shows I_D(on) = 500 mA at V_{GS} = 10V and V_{Th} = 1V. Determine the drain current for V_{GS} = 5V.	(1)
2.b	Explain the different capacitances associated with MOS transistors, including gate-to-source capacitance, gate-to-drain capacitance, and drain-to-source capacitance. How do these capacitances impact the operation of MOSFETs?	(2)
2.c	What is the effect of channel length modulation in a MOSFET? Derive the expression of drain current for the MOSFET after considering the effect of channel length modulation.	(2)
3.a	Define the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) for Voltage Transfer Curve (VTC). How is the noise margin of Inverter calculated?	(1)
3.b	Consider a resistive-load inverter circuit V_{DD} =5V, V_{T0}= 0.8V, V_{Tp}= -0.7V, k_n= = 20 $\mu A/V^2$, R_L=200kΩ and W/L=2. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC.	(2)

3.c	Consider a CMOS inverter circuit with the following parameters: V_{DD} =3.3V, V_{Tn}= 0.6V, V_{Tp}= -0.7V, k_n= = 200 $\mu A/V^2$, and k_p = 80 $\mu A/V^2$. Calculate the noise margins of the circuit for k_R = 2.5.	(2)
4.a	Define the rise time, fall time, and propagation delay for inverter.	(1)
4.b	What is transient analysis of CMOS inverter? Also, derive the τ_{PHL} for the CMOS inverter.	(2)
4.c	Discuss about the effects of scaling down the dimensions of MOS circuits and systems. Also, derive the expression of drain current, area and power density for the different type of scaling in MOS circuits.	(2)

**** GOOD LUCK *****