Progress Report:

CP0, CP1, CP2 work. CP3 is implementation of advanced features.

Functionality	Testing Strategy	Who worked on this component?
Tournament Branch Prediction	Shadow memory with test code. The initial state of the predictors was varied and programs were tested for completeness.	Andrew
Multiplier	Shadow memory with test code. Testbench made to ensure completeness of the multiplier and divider on its own.	Matthew
L2 Cache + Parameterized Set Associative Cache	Shadow memory with test code, using given cache to visualize performance, benchmark, and find correctness of the L2 Cache.	Tim, Andrew

Roadmap:

For Checkpoint 4, we are mostly focused on improving the performance of the advanced features we have implemented in checkpoint 3. With regard to the L2 Cache, we will run benchmarks with the parameterization feature that we implemented and figure out the most optimal way and set for the L2 Cache that will result in the improvement of performance. Adding on to that, with the instruction cache and data cache, we may possibly convert them into parameterized caches and see how performance would be affected as a result of the change. We plan on looking at the clock cycles, timing analysis, as well as total time in order to determine the best parameters and types of caches for all three caches in order to maximize the potential of the processor.

Timing needs to be considered. This means a change to the multiplier is necessary to meet timing. The multiplier will need to be broken up into stages and stall the pipeline.
We will all be working on improving performance by running timing analysis and looking to optimize the multiplier as well as seeing if we can improve the performance of the branch predictor if necessary.