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Paulaner

Hardware Functional Specification

Documents the Hardware features and functions of Paulaner 2RU Chassis

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| 1.0 | 3/28/2022 | Jianqun Fu | Initial version |
| 2.0 | 7/26/2022 | Jianqun Fu | Change PMOD1 & PMOD2 VRM smbus address |
| 3.0 | 9/19/2022 | Jianqun Fu | Change TPS53915 to SIC453 from P2A, update PMUBS address in section 4.4.3.2 |
| 4.0 | 2/24/2023 | Haojie Tian | Modify the description for Paulaner-VE version   * **Remove Main board 12V hotswap circuit** * **Combine original 2 Altera MIFPGAs into one Xilinx FPGA** * Change first 12x CDR5 to MT3722RBQ * Remove 1588/SyncE |

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# Overview

Paulaner is a 2RU TOR (top of the Rack) L2/L3 switch with 64 x QSFP28 & 2 x SFP+ ports on front panel. QSFP28 is used for 100G operation. It can also be used for 40G operation. The main switching ASIC used is Ararat 6.4T Single-Die w/o HBM. The first 48 x QSFP28 ports are driven by retimer mode PHY and the last 16 x QSFP28 ports are driven by MACsec capable PHY. The PHY used is MT3722 from MediaTek. Paulaner uses 1.4KW PSU’s and with limited space on front panel, the management SFP & RJ45 ports, and USB ports have been located on the rear panel. CPU used is Hewitt Lake (using Red Dog). Paulaner will have 32GB of DRAM.

Paulaner supports the following ports & capabilities:

* 64x 100GE QSFP28 Ports
* Single Ararat 6.4T ASIC with ACI Spine and Leaf enablement.
* Secure boot support
* 48 ports retimer + 16 ports MACsec support

Paulaner supports field replacement of SSD and DDR4 modules through access on top cover.

## Risks

|  |  |
| --- | --- |
| Thermal | Implement compact VC heatsink for Ararat cooling in limited height space, has some risk for optics behind Ararat for back to front airflow direction. |
| SI | In order to save cost, SI design paulaner PCB with only 4 HSD layers and w/o 5C rotation, the HSD cross talk also a litter worse under QSFP cage after reducing HSD layer to 4 layers. SI do much simulation/test to demonstrate the risk is low. Will verify after getting the boards back in lab. |
| New Silicons | Ararat – new ASIC |

## Design Considerations

Paulaner needs new chassis design to address more power. It will utilize 1.4KW PSUs and VC based directly attached heatsink for Ararat ASIC and 4x80mm smart fans.

Major key design requirements are listed here:

* 2RU with 64 ports of 100G QSFP28 and 2 ports of 10G SFP+ ports
* Dual 1400W PSU.
* 4x 80mm high speed smart fans
* 16 out of 64 Ports support MACSec

The chassis and building blocks include three newly designed PCBs. There are CPU board, MGMT board and main data board. Red Dog as a CPU board, Red Stripe as MGMT board, for MGMT board, it populates console, USB,management SFP & RJ45 ports. and Paulaner board as a main data board.

Major features of Paulaner main board:

* Single Ararat 6.4T ASIC
* 64x 100GE QSFP28 Ports
* 2x 10G SFP+ Ports

Major features of Red Stripe MGMT board:

* MGMT PHY, MGMT RJ45/SFP/USB port and Console port

## Related Documents

|  |  |
| --- | --- |
| **Doc No** | **Title** |
| **EDCS-23881782** | **Paulaner MIFPGA Specification** |
| **EDCS-23303847** | **Paulaner  PRD** |
| **EDCS-23881806** | **Paulaner Diag Spec** |
| **EDCS-23269899** | **Red Dog CPU board HWFS** |
| **EDCS-23050746** | **Red Dog IOFPGA Specification** |

# High-Level Description

Paulaner is a 2RU TOR (top of the Rack) L2/L3 switch with 64 x QSFP28 & 2 x SFP+ ports on front panel. QSFP28 is used for 100G operation. It can also be used for 40G operation. The main switching ASIC used is Ararat 6.4T Single-Die w/o HBM. The first 48 x QSFP28 ports are driven by retimer mode PHY and the last 16 x QSFP28 ports are driven by MACSec capable PHY. SFP+ ports are directly driven by Ararat. The PHY used is MT3722 from MediaTek. CPU used is Hewitt Lake (using Red Dog). MGMT ports (management SFP & RJ45, Console and USB3.0) are located on the rear side panel. The system uses two (1+1 redundant) 1.4KW AC/DC PSU’s and 4x 80mm high speed smart fans. Both port intake (RED) and port exhaust (BLUE) airflow direction are supported.

Paulaner system is a 2RU chassis that comprises of three separate PCBs:

* Paulaner Main board (also called Base board)
* Red Dog: CPU board
* Red Stripe: MGMT board

The following section provides major components on these three main PCBs:

* CPU complex is based on Intel Hewitt Lake NS SoC. Refer to EDCS-23269899 for CPU board specifications.

1. Hewitt Lake NS D-1624N, 4C, 2.4/2.7GHz, 35W
2. 1 x 32GB of 2400MHz DDR4 DIMM for a total memory of 32GB (64GB support is possible by using 2x 32GB DDR4 DIMMs).
3. 128GB M.2 SATA SSD Flash Drive
4. 16MB each of primary and golden boot flash (With Secure boot support)
5. Microsemi M2S060TS\_FG676 for IOFPGA (Secure Boot and Secure JTAG support)
6. 8GB of eMMC that can be used as OBFL
7. Default 2MB NVRAM, support up to 8MB of NVRAM memory

* Paulaner main board which implements the following key components:

1. Single Ararat 6.4T ASIC
2. One Xilinx Artix7 – MIFPGA (MB Power Sequence and Ararat, CDR5 control, 64x QSFP I2C and management control)
3. Two Lattice LCMXO3LF\_1300 – Base CPLD (MB front port optics management and LEDs driver)
4. Front Ports: 32x QSFP28 2x1 stacked cage and 1x ZSFP+ 2x1 stacked cage

* MGMT board which implements the following key components:
  + Red Stripe:
* MGMT PHY, MGMT RJ45/SFP/USB ports and console port

Each Paulaner also has following FRUs:

1. 1400W PSUs that supports 1 + 1 redundancy, dual air flow
2. 4x 80mm high speed stacked smart fan assemblies supporting port side intake and port side exhaust

Diagram, engineering drawing

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Figure 1: Paulaner Chassis ISO View (Front)

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Figure 2: Paulaner Chassis Port-Side View

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Figure 3: Paulaner Chassis FAN-Side View

## Configurations

Paulaner configurations supported:

* N9K PID
  + Hewitt Lake SKU: D-1624N
    - 4C, 2.4 GHz, 35W (15-107496-01)
  + 32 GB of RAM (2400MT/sec)
  + 2 MB of NVRAM (1 x NVRAM chip)
  + 128GB SSD (boot flash) in M.2 form factor
  + 1 Mgmt port (either copper/RJ45 or fiber/SFP)
  + 2 SFP+ 10G Ports connected to Ararat
  + 1 USB 3.0
  + 1 Console

### Paulaner Numbers

| Paulaner Base |  |
| --- | --- |
| N9K-C9364C-H1 | PID |
| 800-110832-XX | ASY,ELMECH,CHASSIS,Paulaner,TOR |
| 73-103039-XX | |  |  | | --- | --- | |  | PCA,MBRD,Paulaner Ararat 6.4T,64 port 100G,MB,INSBU | |
| 28-102834-XX | PCBFAB,22 L,EM888SA,OSP,120 mil,Paulaner,INSBU |
| 60-105315-XX | PCADWG,Paulaner Ararat 6.4T,MB,INSBU |
| 61-106357-XX | PCAMAP,Paulaner Ararat 6.4T,MB,INSBU |
| 92-105378-XX | SCH,Paulaner Ararat 6.4T,MB,INSBU |

| Red Dog | CPU daughter card |
| --- | --- |
| 73-103040-XX | PCA,MBRD,Red Dog,CPU board,INSBU |
| 28-102835-XX | PCBFAB,12 L,TU-862HF,OSP,93.0 mil,Red Dog,INSBU |
| 60-105316-XX | PCADWG,Red Dog,CPU board,INSBU |
| 61-106358-XX | PCAMAP,Red Dog,CPU board,INSBU |
| 92-105379-XX | SCH,Red Dog,CPU board,INSBU |

| Red Stripe | MGMT card |
| --- | --- |
| 73-103041-XX | PCA,MBRD,Red Stripe,MGMT board,NXOS version,INSBU |
| 28-102836-XX | PCBFAB,10 L,TU-862HF,OSP,62 mil,Red Stripe,INSBU |
| 60-105317-XX | PCBDWG,Red Stripe, MGMT board NXOS version,INSBU |
| 61-106359-XX | PCAMAP,Red Stripe, MGMT board NXOS version,INSBU |
| 92-105380-XX | SCH,Red Stripe, MGMT board NXOS version,INSBU |

### Paulaner CPU Complex Configuration

Paulaner runs on a 4 Core, 2.4/2.7GHz, Hewitt Lake NS CPU (D-1624N). For details of CPU complex and Secure Boot functionality refer to Red Dog CPU Hardware Functional Specification EDCS-23269899.

|  |  |
| --- | --- |
| Device | Configuration |
| CPU | 4 Core, 2.4/2.7GHz, 35W, Hewitt Lake NS SOC SKU:D-1624N |
| Memory | 1x32GB DDR4 DIMMs |
| M.2 SATA Drive | 128 GB SSD Flash Drive |
| Boot Flash | 16MB Primary and 16MB Golden |
| USB | 1 x USB3.0 |
| Consoles | UART0 |
| MGMT | MGMT copper/fiber using NIC I210/88E1112 |
| OBFL | 8GB eMMC |
| NVRAM | 2MB, 55ns access time |

Table 1: Red Dog CPU Complex Configuration

### Paulaner FRUs

#### PSU information

| PSU Type | N9K new PID | Comments |
| --- | --- | --- |
| 1400W-AC | NXA-PAC-1400W-PI  341-1823-01 | AC PSU, Port Intake (Red) Airflow |
| 1400W-AC | NXA-PAC-1400W-PE  341-1824-01 | AC PSU, Port Exhaust (Blue) Airflow |
| 2000W-DC | NXA-PDC-2KW-PI  341-0753-01 | DC PSU, Port Intake (Red) Airflow |
| 2000W-DC | NXA-PDC-2KW-PE  341-0754-01 | DC PSU, Port Exhaust (Blue) Airflow |
| 2000W-HVDC | NXA-PHV-2KW-PI  341-1806-01 | HV DC PSU, Port Intake (Red) Airflow |

#### FAN information

Paulaner uses four fan assemblies per system

|  |  |  |
| --- | --- | --- |
| PID | CPN | Description |
| NXASFAN-160CFM2PI | 800-50343-01 | ASY-MECH,FAN,160CFM,PORT SIDE INTAKE,RED,SMART,NXK |
| NXASFAN-160CFM2PE | 800-50341-01 | ASY-MECH,FAN,160CFM,PORT SIDE EXHAUST,BLUE,SMART,NXK |

## Performance

Provide a description of expected performance/features and justification for claims of performance. Once performance tests have been completed, document the results and indicate how they were obtained.

**<<ISO requirement>>**

Paulaner performance is based on Ararat ASIC performance

## Functional Blocks

Diagram

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Figure 4: Paulaner block diagram

## Theory of Operation

Paulaner 2RU TOR switch provides 100G/40G Ethernet switching on its data ports, The first 48 x QSFP28 ports are driven by retimer mode PHY and the last 16x QSFP28 ports are driven by MACsec capable PHY. In addition, it can support switching at speeds of 40G/4x25G/4x10G by provided appropriate optics/cables and splitter cables are used. There are some restrictions on use of splitter cables and configurations supported. On Paulaner, each Ararat 8-lane macro fans out 4 front panel ports in one column through RGB, each macro can be broken out to x2 or x4 only, thus Ararat does not support a macro to be broken out into 8 separate ports. Take one column front panel ports in Paulaner as an example, the supported front ports (in one column) configuration is shown in below table.

**One column ports as example, please note: breakout can happen in any one of the four ports.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Front Port** | **Front port configuration** | | | |
| **4x 100G QSFP** | **4x 40G QSFP** | **Breakout case #1** | **Breakout case #2** |
| 1 | 100G | 40G | 4x25G | 4x10G |
| 2 | 100G | 40G | Disable | Disable |
| 3 | 100G | 40G | Disable | Disable |
| 4 | 100G | 40G | Disable | Disable |

For more complete list of optics, cables and modes supported refer Cisco TMG website. There is a single Ararat 6.4T ASIC used as the switching chip on Paulaner. When ASIC cannot route packets, they are sent to CPU through control path (PCIe). Management path allows CPU/Switch to be managed through external Ethernet/RS232 ports. Mechanically, Paulaner is a 2RU switch that internally has 3 PCBs inside. System SW and Diagnostic software can treat all the PCBs as single system.

## Initiative, Legal, & Regulatory

Paulaner complies with the same legal and regulatory requirements as all N3K and N9K switching TOR products.

# Detailed Description

## System Block Diagram

System level block diagram of Panlaner is shown in figure-4 above.

The Paulaner 2RU TOR is internally made up of 3 PCBs

1. Paulaner mother board: Single Ararat ASIC is in the center of the main board. One Xilinx Artix7 MIFPGA and two lattice CPLDs are used to manage MB power control, optics control/status interface and Ararat control/status interface.
2. Red Dog: new CPU board, inherited most of the features of Flying Dog CPU board used on Paulaner. Details are in Red Dog HWFS (EDCS-23269899).
3. MGMT board:
   * Red Stripe: Management board, with traditional management ports (MGMT PHY, MGMT RJ45/SFP/USB ports and Console).

64x QSFP28 ports are placed on mother board by using 2x1 stacked belly to belly cages.

### CPU Board (Red Dog)

CPU board Red Dog is redesigned based on existing Flying Dog CPU board. Red Dog handles all the control plane data for the ToR switch. PCIe is the main communication channel to all the IOFPGA, MIFPAGs, switching ASICs, and NICs. Details refer to Red Dog HWFS (EDCS-23269899).

### Power Supply Unit (PSU)

* The Paulaner system will be powered with two 1400W Power Supply Units (PSU) in 1+1 mode
* Each PSU can operate on AC or DC mode.
* Each PSU outputs (a) 12V-Main power and (b) 12V-Standby power. The 12V-Main and 12V-Standby from both PSUs are interconnected by BUSBAR then power the whole chassis.
* **Paulaner removed 12V hotswap circuit on Main Board from P3, 12V from 2 PSUs will directly power on the Main board/CPU board.**
* Both PSUs share current using active current share feature on 12V-Main by tying the Ishare pins of both PSUs together and 12V-Standby current is shared using droop mode.

### Fan modules and control

Fan modules are directly plugged into Red Dog board. Red Dog has 4 fan connectors. These 4 fan assemblies are controlled and monitored by single fan controller. Detail register map is available in Red Dog HWFS section 4.4.3.

For the Fan modules, reuse the 80mm Fans used on RedHorse

|  |  |  |
| --- | --- | --- |
| PID | CPN | Description |
| NXASFAN-160CFM2PI | 800-50343-01 | ASY-MECH,FAN,160CFM,PORT SIDE INTAKE,RED,SMART,NXK |
| NXASFAN-160CFM2PE | 800-50341-01 | ASY-MECH,FAN,160CFM,PORT SIDE EXHAUST,BLUE,SMART,NXK |

### Console, Management Ethernet, USB interface

The management ports of Paulaner system are located on Red Stripe which connect to CPU board through PCIe\_98P gen-3 connector. The CPU board directly drives a UART RS232 device for the console and USB port. The CPU root port also has a Gen1 x1 PCIe link to the i210 controller which provides a management ethernet port. This ethernet port supports dual media, SFP and RJ45 copper interface, exclusively.

### Front and Rear panel

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Figure 5 Front and rear panel

## Ararat

Paulaner uses Ararat 6.4T (single-die w/o HBM) ASIC. Refer to Ararat specifications listed in references section for detailed description and functionality of this ASIC. Below list the major features of 12.8T Ararat, Ararat 6.4T is single-die version w/o HBM.

* Up to 12.8Tbps aggregate switching bandwidth, supporting the following break-out modes:[[1]](#footnote-1)
  + 32x400G (8x 50G PAM4)
  + 64x200G (4x 50G PAM4)
  + 32x(1x 200G + 2x 100G/50G/40G/25G/10G)
  + 128x100G (2x25G PAM4) or 64x100G (QSFP 25G)
  + 128x50G/40G/25G/10G (50G PAM4)
  + 64x40G/10G (QSFP 10G/2.5G)
* Single stage output buffer divided into 4 slices:
  + 80MB of total on chip buffer;
  + ~40MB of buffer per pair of output slices, for 6.4Tbps of port bandwidth;
  + Full 12.8Tbps of enqueue bandwidth per slice for non-blocking internal switching;
  + Non-blocking packet replication (multicast) with overspeed;
* 36MB input buffer:
  + 288KB per 100Gbps bandwidth;
  + 4 non-blocking queues, 2 for no-drop and provides PFC overhead storage;
  + 2 queues for drop classes and provides forwarding oversubscription absorption;
* 8GB useable off-die, DRAM based deep buffer;
  + Output buffer, extending on-die {oport, oclass} queues;
  + Only for user class unicast queues;
  + Supports no-drop classes;
  + 8KB page size, may include multiple packets per page;
  + Flat space shared by all input/output ports, i.e., no traffic pattern restrictions;
  + Per queue enable, e.g. only allow for certain links/direction
    - ToR uplink ports, north-bound for OSB
    - ToR host interfaces, south-bound for incast absorption
    - Spine LC ingress direction
    - Inter-DC WAN ports, no-drop classes
* Jumbo frame (up to 10KB);
* 802.1Qbb PFC
  + Up to 7 no-drop classes (mapped down to two queues);
  + Up to 2 non-overlapping no-drop queues;
* 100% line rate for all packet sizes > 257B @1.45Ghz clock rate in 12.8Tbps mode;
  + 30% line rate for 64B packets;
* 10 CoS levels
  + 8 user classes (extendable to DB) + 2 ASIC internal classes;
  + Total 20 queues per port between unicast/multicast;
* Per {output port, CoS} queuing;
  + SP or DWRR on all classes;
  + Min/max rate limiting on all classes;
  + Individually flushable queue;
  + Local CPU/Embedded CPU and (low speed) management ports;
  + Internal recirculation ports for SPAN-on-Drop;
* Buffer allocation by ‘logical switch’
  + Statically divide buffer between two independent, ‘logical’ switches;
  + An output port belongs to one of the logical switches;
  + Input accounting is scoped by the logical switch;
  + No restriction of UC/MC class count per logical switch;
* Limited internal recirculation
  + Per output slice can loop back to the input slice connected to the same set of MACs;
  + 2x200Gbps recirculation bandwidth;
    - Can be configured for 200Gbps recirculation per logical switch;
  + Recirculation can be MET destination;
  + Supports egress-forwarding SPAN on drop;
* Two management ports up to 10GE speed

|  |  |  |  |
| --- | --- | --- | --- |
| **MAC Mode** | **Link Speed** | **Serdes Speed** | **Link Width** |
| 400GE R8 | 400G | 56Gbps PAM4 | 8 |
| 200GE R8 | 200G | 25Gbps NRZ | 8 |
| 200GE R4 | 200G | 56Gbps PAM4 | 4 |
| 100GE R4 | 100G | 25Gbps NRZ | 4 |
| 100GE R2 | 100G | 56Gbps PAM4 | 2 |
| 50GE R2 | 50G | 25Gbps NRZ | 2 |
| 40GE R4 | 40G | 10Gbps NRZ | 4 |

**Table 2 Ararat Supported MAC modes**

****

Figure 6 Ararat Power On/Off Sequence

## CDR5

Paulaner uses 16 retimer chips and will drive all 64 ports up to 100G. There are two dedicated MDIO interface from FPGA to each retimer. Each retimer chip works as reverse gearbox mode to fan out 4x100G ports. Paulaner can support MACSec for the last 16 QSFP28 ports.

The CDR5 retimer used in design is: MT3722RBQ(Retimer mode only) from MTK, its CPN is 15-107637-02, and MT3722MBQ(MACSec mode capable) from MTK , its CPN is 15-107175-02.

CDR5 can be configured or monitored using either MDIO or I2C interface. And the reference clock of the CDR5 is 156.25MHz.

Below table list all type of port operation modes supported in retimer mode.

Table 3 Port mode of CDR5 supported in Retimer mode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Device | Port operation mode | Port number | lanes x speed per port | signal type |
| MTK | 400G | 2 | 8x 53.12G P | PAM4 |
| 200G | 4 | 4x 53.12G | PAM4 |
| 100G | 8 | 2x 53.12G PAM4 | PAM4 |
| 100G | 4 | 4x 25.78125G NRZ | NRZ |
| 50G | 16 | 1x 53.12G PAM4 | PAM4 |
| 50G | 8 | 2x 25.78125G NRZ | NRZ |
| 40G | 4 | 4x 10G NRZ | NRZ |
| 25G | 16 | 1x 25.78125G NRZ | NRZ |
| 10G | 16 | 1x 10G NRZ | NRZ |
| 1G | 16 | 1x 1G NRZ | NRZ |
| mixed | TBD | combinationm of above mode within the limt of availabe ports | TBD |

CDR5 supports two MDIO slaves and can handle different commands from the two MDIO master in parallel. It could meet higher throughput requirement, for example, in MACsec application, one MDIO could be dedicated to handle MDIO access for MACsec. There are two MDIO interfaces from FPGA to each CDR5.

Table 4 HW address pins of CDR5

|  |  |  |  |
| --- | --- | --- | --- |
| Device | ADDR[3:0] pins definition | HW default settings | Notes |
| MTK | ADDR[3:2] : phy address setting[1:0] for slave ID  PHY[1:0]: phy address selection[1:0] as chip selection for MDIO master | ADDR[3:0] are Pull down to GND | Two MDIO master connected to MTK CDR5,  The slave ID are set 00 and chip selection MDIO master is set “00” |

MTK MT3722MBQ main feature:

Serdes

* 16-lanes of SerDes at Host side and 16-lanes of SerDes at Line side.
* Supports Ethernet bit rate of 56Gbps (PAM4), 28/20/10Gbps (NRZ) and 1G SGMII.
* Per lane independent clock and data rate selection
* Retimer function with TX clock locked to RX recovered clock
* upports Forward GearBox from low bit rate to high bit rate, such as from 28G to 56G and from 10G to 20G
* Supports pure Retimer mode, in which Host side SerDes interconnects with Line side SerDes directly.
* Supports lane swap per 8-lane slice.
* Supports AC-coupled or DC-coupled operation on both Host side and Line side.

PCS and FEC

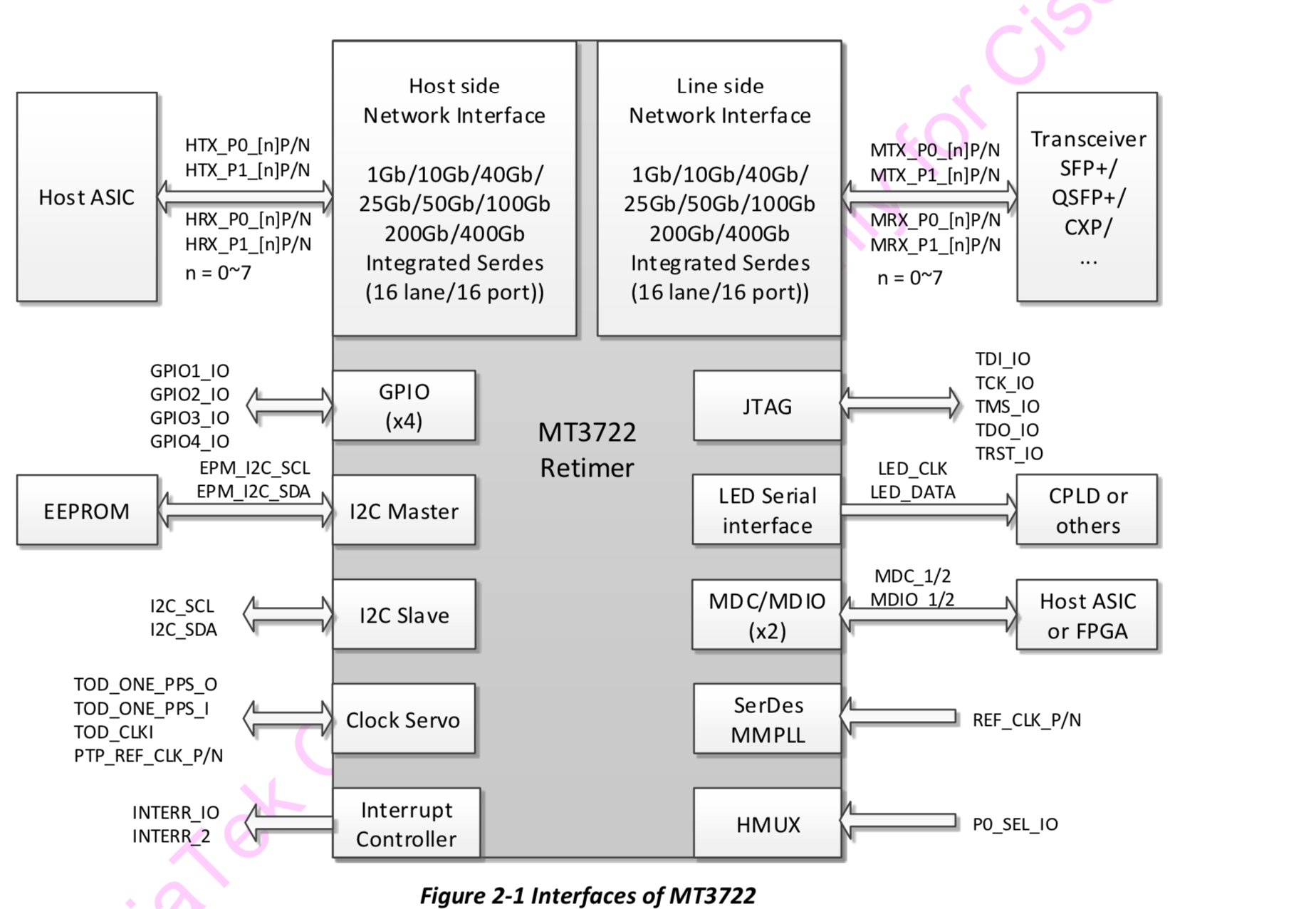
* The embedded Physical Coding Sublayer (PCS) supports Ethernet 400G-R16/R8, 200G-R8/R4, 100G-R4/R2, 50G-R2/R1, 40G-R4/R2, 25G, 10G, 1G.
* Supporting Forward Error Correction (FEC) format translation, for example, from RS-FEC-528 to RS-FEC-544

MAC and MACsec

* Per 400G slice supports up to 1x400G, 2x200G, 4x100G/40G, 8x50G/25G/10G/1G MAC ports.
* MACsec supports 1024 SecY and 2048 SA per 400G slice.
* MACsec supports CISCO proprietary CloudSec-2.5 and ClearTag-3.5.
* MACsec supports tremendous 64-bit statistic counters for debugging and monitoring.
* Supports up to 2x MDC / MDIO as host interface.

Host Control interface

* Supports up to 2x MDC / MDIO as host interface
* Supports IEEE 802.3 CL45 commands for standard feature control.
* Supports special access command to improve host access throughput. It can read/write data up to 512 bits per access command.
* Supports I2C Slave as another host interface for debugging.
* Max Tj is 110C



## FPGA

There are total two FPGAs on Paulaner system:

1. CPU-Microsemi FPGA

The CPU-MicrosemiFPGA is located on the CPU board. For register and bit descriptions, refer to: Red Dog IOFPGA Specification, EDCS-23050746.

1. Base-MIFPGA

The Base-MIFPGA is located on the Main board. MIFPGA functions as MB power sequencer, Ararat, CDR5 controller, 64x QSFP I2C and optics management controller. For register and bit descriptions, refer to EDCS-23881782.

MIFPGA is of Xilinx Artix7 family and use 256Mb SPI Flash for storing the FPGA image. IOFPGA uses Microsemi M2S060TS\_FG676

Both FPGAs can be upgraded in the field. This allows new features and bug fixes that could be rolled out after FCS. The system would need to be followed by full power cycle for the new image to take effect.

The FPGA supports the field upgrade through its internal PCIe to FPGA SPI interface. The software bundled the FPGA image and downloaded it into the FPGA internal block ram through the PCIe interface. FPGA will automatically write the new image into its own SPI flash. The FPGA also maintains the golden image that is pre-programed at the factory for fail-recovery in case the new image is corrupted during the download process.

## IO Expander CPLDs

Paulaner uses two Lattice LCMXO3LF\_1300 CPLDs for “io expander” functionality. (primarily port LEDs and low speed QSFP28 signals). They are connected to MIFPGA using proprietary serial interface running at 2MHz. Field upgrade of CPLD image is also supported.

## PCIe architecture

PCIe port connections from CPU are shown in the drawing below. There are four ports of PCIe is used on Paulaner.

* IOFPGA is connected to PE1[0] of Hewitt Lake NS CPU, single lane, Gen1 speed.
* Ararat is connected to PE2[0-3] of Hewitt Lake NS CPU, four lanes, Gen3 speed.
* MIFPGA on Paulaner main board is connected to PE[1] of PCH, single lane, Gen1 speed.
* I210 NIC on Red Dog is connected to PE[6] of PCH, single lane, Gen1 speed

## ID EEPROM/ACT2 Chip

Paulaner has one ID ACT2 chip 15-14497-02 connected to MIFPGA on main board through SMBUS. CPU board use Aikido FPGA internal ACT2. Software should use MB ACT2 for security check

* Provides EEPROM and security functionality
* I2C up to 400KHz
* UART 9600 baud
* 50KB EEPROM space available to host system

Refer to <http://172.21.158.41:8080/logicaldoc/download?docId=342> for more info

## Clock Distribution

Timeline

Description automatically generated with medium confidence

Figure 7: Paulaner Clock Diagram

The figure above shows the clocking scheme used on Paulaner. The 156.25 MHz, fiber channel 212.5 MHz reference clocks needed for ASIC, 156.25 MHz needed for retimers, ASIC 100 MHz for HBM and INFO reference clock are generated by crystal oscillators with fan out buffers placed in between. PCIe clock outputs from CPU are used as reference PCIe clocks for ASIC, MIFPGA, i210. MIFPGA 50MHz reference clock can come from a dedicated on-board oscillator.

## Temperature sensors

There are 2 ambient temperature sensors in the system, one in Red Dog is embedded in fan controller (ADT7462) placed closed to the fans. The other one in Paulaner base board (MAX1617, CPN: 15-12160-01) is wired to the front. Depend on system air flow direction, these two temperature sensors can be used to monitor intake and exhaust air temperature.

## Power distribution

The system uses 2x1400W PSUs. (1 + 1 redundant). One power supply connector on Paulaner main board and another one on CPU board.

**The interconnection of 12V power from 2 PSUs is through BUSBAR. Paulaner removed 12V hotswap circuit on Main Board from P3, 12V from 2 PSUs will directly power on the Main board/CPU board.**

DC-DC point-of-load converters convert 12V into final voltages.

System level power distribution is shown in the diagram below.

Diagram, schematic

Description automatically generated

Figure 8: Paulaner Power Diagram

### Power Supply Unit (PSU)

* The Paulaner system will be powered with two 1.4KW Power Supply Units (PSU) in 1+1 mode
* Each PSU can operate on AC, HVDC or LVDC mode
* Each PSU outputs (a) 12V-Main power and (b) 12V-Standby power.
* Both PSUs share current using active current share feature on 12V-Main by tying the Ishare pins of both PSUs together and 12VStandby current is shared using droop mode.

| PSU Type | N9K new PID | Comments |
| --- | --- | --- |
| 1400W-AC | NXA-PAC-1400W-PI  341-1823-01 | AC PSU, Port Intake (Red) Airflow |
| 1400W-AC | NXA-PAC-1400W-PE  341-1824-01 | AC PSU, Port Exhaust (Blue) Airflow |
| 2000W-DC | NXA-PDC-2KW-PI  341-0753-01 | DC PSU, Port Intake (Red) Airflow |
| 2000W-DC | NXA-PDC-2KW-PE  341-0754-01 | DC PSU, Port Exhaust (Blue) Airflow |
| 2000W-HVDC | NXA-PHV-2KW-PI  341-1806-01 | HV DC PSU, Port Intake (Red) Airflow |

**The PSUs Paulaner supported are in this table**

### Paulaner Power Domains

Paulaner power plane can be split into these two domains:

* Always power domain voltage rails are driven directly from Main 12V, they are for IOFPGA on CPU board, MGMT NIC ports and MIFPGA on Main board. The A domain power will always on once Main 12V is on and good, it is not controlled by any FPGA.
* Main power domain is derived from Main 12V on Paulaner CPU/Main board. IOFPGA controls Main power domain’s power on/off sequence on CPU board, MIFPGA controls Main power domain’s power on/off sequence on Main board.

### Power-Up Sequence

* When one or more PSU is installed in the system and the PSU input power is ON, Standby domain power will be turned on. At the same time, PSUs will be turned on automatically.
* A domain power will be turned on automatically to configure IOFPGA on CPU board and MIFPGA on MB.
* IOFPGA will start turning on other voltage rails on CPU, and Main board. In the process, IOFPGA and MIFPGA will use handshake signals to control system level power sequence.
* System level power sequence of each board please refer:
  + Red Dog power on sequence – EDCS-23269339
  + Paulaner MB power on sequence – EDCS-xxxxx

## System Cooling

System cooling is accomplished by 4 x 80mm dual stacked fans in 3+1 configuration. These fans are individually hot swappable. The system monitors ambient and critical component temperature and adjusts fan speed accordingly. Paulaner can support both airflow direction.

Power supplies have their own fans. Red Dog is responsible for control/status of the system fans.

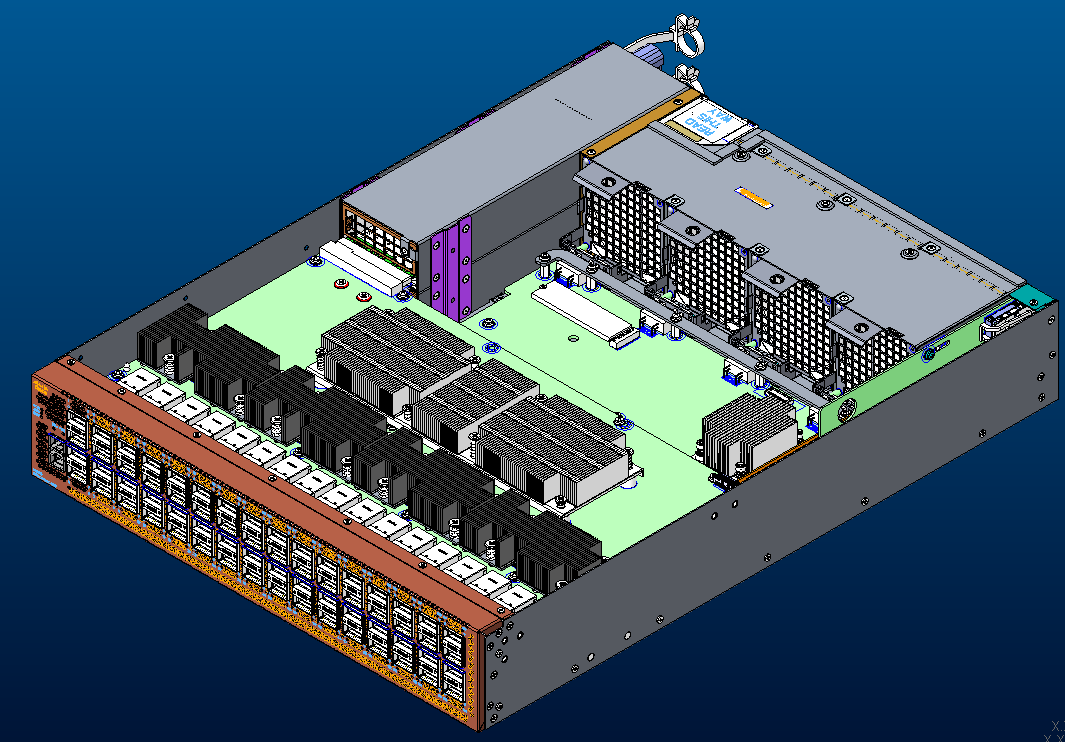


Figure 9：System FAN and PSU Placement

### Components for thermal analysis

Table 5: Thermal Thresholds and power consumption

| Component | Max T | Power Consumption | Comments |
| --- | --- | --- | --- |
| CPU | 90°C | 35W |  |
| QSFP28 module | Depends on module | 4.5W each |  |
| Ararat 6.4T | 115°C | 250W |  |
| CDR5 MACSec | 110°C | 19W |  |
| CDR5 Retimer | 110°C | 16W |  |
| ASIC VRD FETs | 115°C | N/A |  |
| Intake temp sensor | 55 | N/A |  |

# Software Considerations

## Memory Maps

Refer to Red Dog IOFPGA and Paulaner MIFPGA specs for memory map definitions. The document EDCS numbers are listed in the References section of this document.

## Register Definitions

Refer to Red Dog IOFPGA and Paulaner MIFPGA specs for register definitions. The document EDCS numbers are listed in the References section of this document

## Programming Requirements / Mapping

### Programmable Devices

Following table shows the programmable devices on the system and their preprogrammed part numbers.

| Device | Board | Reference Designator | CPN | Raw part number | description |
| --- | --- | --- | --- | --- | --- |
| MIFPGA | Paulaner | U35 | 17- | 16-4194-04 | Paulaner MIFPGA image |
| CPLD0 | Paulaner | U12 | 17- | 16-100991-01 | Paulaner CPLD0 image |
| CPLD1 | Paulaner | U4 | 17- | 16-100991-01 | Paulaner CPLD1 image |
| 10GE SPROM | Red Dog | U11\_CP | 17-101581-01 | 16-100239-xx | CPU 10GE port configuration |
| I210 FLASH FW | Red Dog | U2\_MGMT1 | 17-14437-04 | 16-4194-04 | I210 NIC FW |
| BIOS FLASH | Red Dog | U41\_CP, U42\_CP | 17- | 16-4194-04 | Golden and Primary BIOS |
| IOFPGA image | Red Dog | U59 | 17- | 16-100925-01 | CPU Board IOFPGA image |

### Temperature Monitoring

Suggested temperature sensors are listed in the table below for ambient temperature monitoring.

|  |  |
| --- | --- |
|  | Port Side Intake airflow |
| Intake | Use a front sensor on Base board  (remote sensor of MAX1617@0x18(7bit) on TSENSE through Base MIFPGA0) |
| Exhaust | Use a rear sensor  (local sensor on Fan controller ADT7462) |
|  |  |

## Other Software Considerations

### Magic Cookie EPROM

Paulaner will support the ACT2 ID PROM on both CPU and MB for tracking purpose.

Refer to latest PCAMAP in Agile for IDPROM HW Changes bit definition

### PCIe Configuration

On Paulaner, the Hewitt Lake NS CPU PCIe ports are bifurcated and mapped as follow table.

PCIe will be enumerated by BIOS when the system CPU is booting up. The software will leverage the bus numbers and the memory space from BIOS

|  |  |  |
| --- | --- | --- |
| **Broadwell PCIe Port** | **Speed** | **Device Connectivity** |
| CPU.PE1[0] | Gen 1 (2.5 GT/s) x1 | CPU IOFPGA |
| CPU.PE2[0-3] | Gen 3 (8 GT/s) x4 | Ararat |
| PCH.PE[1] | Gen 1 (2.5 GT/s) x1 | MIFPGA in MB |
| PCH.PE[6] | Gen 1 (2.5 GT/s) x1 | I210 NIC |

Table 6: Hewitt Lake CPU PCIe Root Port Bifurcation and Mapping

### PMB/SMB/I2C and MDIO BUS

The I2C bus is separated into several groups to minimize the stubs and reflections on the bus. The following tables show the I2C bus details for base-iofpga.

#### CPU IOFPGA SMBUS/I2C Address Map

Please refer to Red Dog HWFS EDCS-23269899.

#### Mother board MIFPGA Address Map

| **Bus Master** | **Bus Name** | **Device** | **Address**  **(7-bit)** | **Description** | **Note** |
| --- | --- | --- | --- | --- | --- |
| MIFPGA | I2C\_IDPROM | ACT2 | 0x70 | Paulaner MB ACT2 |  |
| I2C\_TSENSE | MAX1617 | 0x18 | Ambient Temperature sensor | Use remote |
| PMBUS0 | XDPE132G5 | 0x40 | AR\_VDDK, 0.8V | Ararat VDDK 10phase VRM |
| PMBUS1 | IR35215(1+1) | 0x74 | AR\_AVDD1V0, 1.0V  AR\_AVDD0V8, 0.8V | Insieme use base 0x10/0x40 |
| IR35215(2+0) | 0x71 | P3V3\_QSFP\_A |  |
| IR35215(2+0) | 0x70 | P3V3\_QSFP\_B |  |
| PMBUS2 | IR35215(2+2) | 0x74 | MS\_VDDK\_A1, 0.8V  MS\_VDDK\_A2, 0.8V | Macsec Group A |
| IR35215(2+1) | 0x72 | MS\_AVDD12\_A, 1.15V  MS\_AVDD09\_A, 0.85V |  |
| IR35215(2+3) | 0x76 | MS\_VDDK\_B1, 0.8V  MS\_VDDK\_B2, 0.8V | Macsec Group B |
| IR35215(2+1) | 0x78 | MS\_AVDD12\_B, 1.15V  MS\_AVDD09\_B, 0.85V |  |
| PMBUS3 | TPS53915(P1A)  SIC453(P2A~) | 0x10  0x10 | AR\_P1V8 | Change to SIC453 from P2A |
| TPS53915(P1A)  SIC453(P2A~) | 0x1F  0x11 | MS\_P1V8 | Change to SIC453 from P2A |
| ~~I2C\_SI5341~~ | ~~SI5341~~ | ~~0x74~~ | ~~Clock generator~~ |  |
| I2C\_LTC2497 | LTC2497 | 0x28 | Voltage monitor, LTC2497 |  |
| AR\_HOST | Ararat |  | Ararat host i2c interface | See MIFPGA spec |
| AR\_i2C\_0 | Ararat |  | Ararat i2c interface | See MIFPGA spec |

#### MDIO Buses

There are 32 separate MDIO (IEEE 802.3ae Clause 45) buses on Paulaner, two for each retimer device. Each bus is point to point with MIFPGA as master.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Front Panel Port #** | **ASIC ETHL #** | **Retimer Instance # / (Ref Des)** | **Retimer Port/Channel # (Lane #)** | **MDIO Bus Name** | **PHY Address [4:0]** |
| 1 | 56G\_00 | 0 | 0 (Lanes 0 - 3) | MS0\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 2 | 0 (Lanes 4 – 7) |
| 3 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 4 | 1 (Lanes 4 – 7) |
| 5 | 56G\_01 | 1 | 0 (Lanes 0 - 3) | MS1\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 6 | 0 (Lanes 4 – 7) |
| 7 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 8 | 1 (Lanes 4 – 7) |
| 9 | 56G\_02 | 2 | 0 (Lanes 0 - 3) | MS2\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 10 | 0 (Lanes 4 – 7) |
| 11 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 12 | 1 (Lanes 4 – 7) |
| 13 | 56G\_03 | 3 | 0 (Lanes 0 - 3) | MS3\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 14 | 0 (Lanes 4 – 7) |
| 15 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 16 | 1 (Lanes 4 – 7) |
| 17 | 56G\_04 | 4 | 0 (Lanes 0 - 3) | MS4\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 18 | 0 (Lanes 4 – 7) |
| 19 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 20 | 1 (Lanes 4 – 7) |
| 21 | 56G\_05 | 5 | 0 (Lanes 0 - 3) | MS5\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 22 | 0 (Lanes 4 – 7) |
| 23 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 24 | 1 (Lanes 4 – 7) |
| 25 | 56G\_06 | 6 | 0 (Lanes 0 - 3) | MS6\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 26 | 0 (Lanes 4 – 7) |
| 27 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 28 | 1 (Lanes 4 – 7) |
| 29 | 56G\_07 | 7 | 0 (Lanes 0 - 3) | MS7\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 30 | 0 (Lanes 4 – 7) |
| 31 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 32 | 1 (Lanes 4 – 7) |
| 33 | 56G\_08 | 8 | 0 (Lanes 0 - 3) | MS8\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 34 | 0 (Lanes 4 – 7) |
| 35 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 36 | 1 (Lanes 4 – 7) |
| 37 | 56G\_09 | 9 | 0 (Lanes 0 - 3) | MS9\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 38 | 0 (Lanes 4 – 7) |
| 39 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 40 | 1 (Lanes 4 – 7) |
| 41 | 56G\_10 | 10 | 0 (Lanes 0 - 3) | MS10\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 42 | 0 (Lanes 4 – 7) |
| 43 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 44 | 1 (Lanes 4 – 7) |
| 45 | 56G\_11 | 11 | 0 (Lanes 0 - 3) | MS11\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 46 | 0 (Lanes 4 – 7) |
| 47 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 48 | 1 (Lanes 4 – 7) |
| 49 | 56G\_12 | 12 | 0 (Lanes 0 - 3) | MS12\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 50 | 0 (Lanes 4 – 7) |
| 51 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 52 | 1 (Lanes 4 – 7) |
| 53 | 56G\_13 | 13 | 0 (Lanes 0 - 3) | MS13\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 54 | 0 (Lanes 4 – 7) |
| 55 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 56 | 1 (Lanes 4 – 7) |
| 57 | 56G\_14 | 14 | 0 (Lanes 0 - 3) | MS14\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 58 | 0 (Lanes 4 – 7) |
| 59 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 60 | 1 (Lanes 4 – 7) |
| 61 | 56G\_15 | 15 | 0 (Lanes 0 - 3) | MS15\_MDIO[0/1] | 0x8-0xF (Host Side)  0x18-0x1F (Line Side) |
| 62 | 0 (Lanes 4 – 7) |
| 63 | 1 (Lanes 0 – 3) | 0x0-0x7 (Host Side)  0x10-0x17 (Line Side) |
| 64 | 1 (Lanes 4 – 7) |

Table 7 Paulaner Port Mapping and Retimer MDIO Bus assignment

*Note: Front panel port # is one based.*

Below table shows the 5 bit PHY Address field of the MDIO transaction needed to address the 32 serdes of each Retimer instance. Note that there are 16 serdes on Host side and 16 on Line side.

|  |  |  |  |
| --- | --- | --- | --- |
| **Retimer Port/Channel #** | **Retimer Serdes #** | **MDIO PHY Address (5 bits)**  **Host Side** | **MDIO PHY Address (5 bits)**  **Line Side** |
| 0 | 0 | 5’b00000 | 5’b10000 |
| 1 | 5’b00001 | 5’b10001 |
| 2 | 5’b00010 | 5’b10010 |
| 3 | 5’b00011 | 5’b10011 |
| 4 | 5’b00100 | 5’b10100 |
| 5 | 5’b00101 | 5’b10101 |
| 6 | 5’b00110 | 5’b10110 |
| 7 | 5’b00111 | 5’b10111 |
| 1 | 8 | 5’b01000 | 5’b11000 |
| 9 | 5’b01001 | 5’b11001 |
| 10 | 5’b01010 | 5’b11010 |
| 11 | 5’b01011 | 5’b11011 |
| 12 | 5’b01100 | 5’b11100 |
| 13 | 5’b01101 | 5’b11101 |
| 14 | 5’b01110 | 5’b11110 |
| 15 | 5’b01111 | 5’b11111 |

Table 8 Retimer MDIO Phy Address

Table

Description automatically generated

### Data Path Port Mapping

Regarding Paulaner Data Path port mapping, referring table 15 above.

### Port/Retimer interrupts

Two Interrupt lines per retimer device is connected to MIFPGA. Each QSFP28 module has one interrupt signal connected to FPGA to indicate module fault or critical status.

Referring Paulaner MIFPGA specifications for details information about interrupt register of CDR5M and QSFP module.

### Firmware/Configuration download

Firmware needs to be downloaded on each CDR5 via SW and because there is no onboard flash memory for FW, the image needs to be bundled in the SW image.

# User Interface Considerations/ User Experience

Paulaner contains the beacon (blue),status (green/amber) and ENV (green/amber) LED. Each front panel port has its own dedicated port LED (green/yellow).

| LED | Color | Location |
| --- | --- | --- |
| Ports | Green/Amber | SFP+ or QSFP28 cage |
| Beacon | Blue | Front and rear of chassis |
| Status | Green/Red | Front and rear of chassis |
| Env | Green/Red | Front and rear of chassis |
| Power supply | Green Amber | See PSU spec for definition |
| Fan modules | Green/Amber | Rear of chassis integrated in fan |

Table 9 System LEDs

## Paulaner Front and Rear Panel LEDs

The BCM, STATUS, ENV and BMC LEDs are located on Front panel. Following table describes the possible states for each of these LEDs.

|  |  |  |
| --- | --- | --- |
| **LED** | **Color** | **Status** |
| BCN(Beacon) | Flashing blue | The operator has activated this LED to identify this switch in the chassis. |
|  | Off | This module is not being identified. |
| STS(Status) | Green | The module is operational and has no active major or critical alarms. |
| Amber | Temperature exceeds minor alarm threshold. |
| Red | Power-up failure which prevents the CPU from booting (set by hardware), or  Temperature exceeds major alarm threshold. |
| Flashing Amber | The module is booting up. |
| Off | The module is powered-off. (set by hardware) |
| Env | Green | Fans and power supply modules are operational. |
| Amber | At least one fan or power supply module is not operating. |
| Off | No alarm |

Table 10: Paulaner Chassis LED definition

## Paulaner Fan Tray LEDs

|  |  |  |
| --- | --- | --- |
| **LED** | **Color** | **Status** |
| STS | Green | Fan is operating normally |
| Amber | One or more fan in the module is faulty |
| Off | Fan tray is not receiving power |

Table 11: Paulaner Fan Tray LED definition

## Paulaner Power Supply LEDs

|  |  |  |
| --- | --- | --- |
| **LED**<http://www.cisco.com/c/dam/en/us/td/i/300001-400000/300001-310000/304001-305000/304505.eps/_jcr_content/renditions/304505.jpg> | **LED** <http://www.cisco.com/c/dam/en/us/td/i/300001-400000/300001-310000/304001-305000/304504.eps/_jcr_content/renditions/304504.jpg> | **Status** |
| Green | Off | Power supply is on and outputting power to the switch. |
| Flashing Green | Off | Power supply is connected to a power source but not outputting power to the switch—power supply might not be installed in the chassis. |
| Off | Off | Power supply is not receiving power. |
| Green | Flashing Amber | Power supply warning—possibly one of the following conditions:   * High voltage * High power * Low voltage * Power supply installed in chassis but not connected to a power source * Slow power supply fan |
| Flashing Green | Amber | Power supply failure—possibly one of the following conditions:   * Over voltage * Over current * Over temperature * Power supply fan failure |

Table 12: Paulaner Power Supply LED definition

# Power Supply Requirements

See section 3.10 for more details

# Mechanical Description

This section describes the mechanical considerations and implementation of Paulaner 2RU system.

## Chassis Metrics

### Physical Dimensions

Chassis length: 22.27 inches (565.62mm)

Chassis width: 17.41 inches (442.34mm)

Chassis height: 3.4 inches (86.4mm)

### Weight

Approximate 44lbs(20kg)

## Mechanical Rendering

A picture containing text

Description automatically generated

Diagram

Description automatically generated

Diagram, box and whisker chart

Description automatically generated with medium confidence

Diagram

Description automatically generated

## Connectors

* 1x SlimSAS connectors is used between MB and Red Dog

## Thermal Considerations and Solutions

Paulaner has following requirements related to operating/storage temperature.

* Operating altitude:  Designed to meet: –500 ft. to 13,123 ft.
* Agency approved:  -500 ft. to 6500 ft.
* Non-operating: -1000 ft. to 30,000 ft.
* Operating temperature: 32 to 104ºF (0 to 40ºC)
* Storage temperature: –40 to 158ºF (–40 to 70ºC)
* Relative humidity: 5 to 90 percent, non-condensing

### Paulaner High Power Devices

|  |  |  |
| --- | --- | --- |
| **Device** | **Max Power** | **Quantity** |
| CPU(6 Core) | 35W | 1 |
| Ararat | 250W | 1 |
| QSFP28 | 4.5W | 64 |
| CDR5-MACSec | 19W | 4 |
| CDR5-Retimer | 16W | 12 |

Table 14: High Power devices

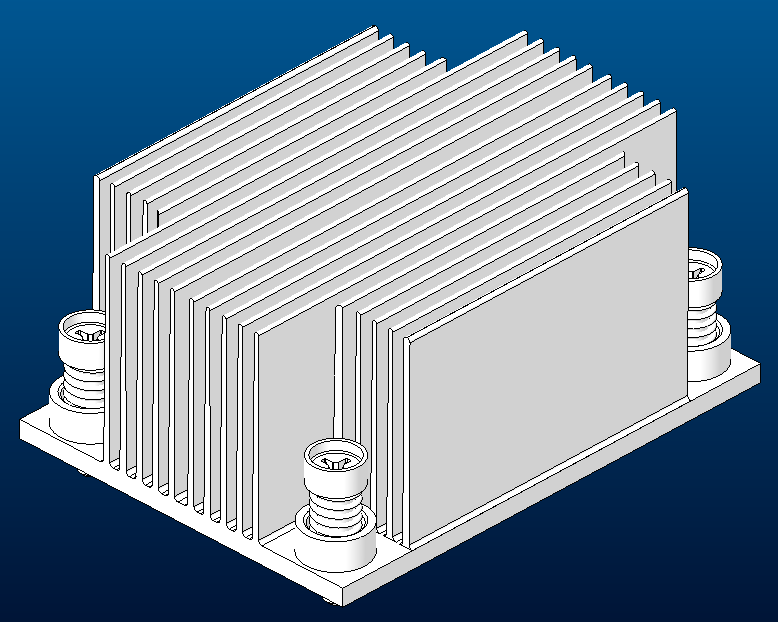
### Paulaner Devices with heat sinks

The devices with heat sinks are,

* CPU on the cpu board
* Ararat on base board
* MTK CDR5M and CDR5 retimer

### Paulaner Heat Sink Views

CPU Heat Sink 700-109611-01



CDR5 Heat Sink 700-130905-01 (X8)

Diagram, engineering drawing

Description automatically generated

Ararat Heat Sink 700-131396-01

A picture containing diagram

Description automatically generated

# Signal Integrity Considerations

## Impedance Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| a)     Edge coupled differential pairs (**DIFF**): | | | | |  |  |  |
| \* Target impedance: 92 Ohm | | | |  |  |  |  |
|  | \* 92 Ohms ±7%: Target trace width/center-line pitch is 5mil / 14mil for **Internal** layers | | | | | | |
|  | \* 92 Ohms ±10%: Target **Neck** trace width/center-line pitch is 4mil / 8mil for **Internal** layers | | | | | | |
|  | \* 92 Ohms ±15%: Target trace width/center-line pitch is 7mil / 14mil for **External** layers | | | | | | |
| \* Target impedance:100 Ohm | | | |  |  |  |  |
|  | \* 100 Ohms ±10%: Target trace width/center-line pitch is 3.8mil / 11.8mil for **Internal** layers S10&S15 | | | | | | |
|  | \* 100 Ohms ±10%: Target trace width/center-line pitch is 4.5mil / 12.5mil for **Internal** layers S6/8/17/19 | | | | | | |
|  | \* 100 Ohms ±10%: Target **Neck** trace width/center-line pitch is 3.5mil / 8mil for **Internal** layers S10&S15 | | | | | | |
|  | \* 100 Ohms ±10%: Target **Neck** trace width/center-line pitch is 4mil / 8mil for **Internal** layers S6/8/17/19 | | | | | | |
|  | \* 100 Ohms ±15%: Target trace width/center-line pitch is 6mil / 14mil for **External** layers | | | | | | |
| \* Target impedance:85 Ohm | | | |  |  |  |  |
|  | \* 85 Ohms ±10%: Target trace width/center-line pitch is 5mil / 14mil for **Internal** layers S10&S15 | | | | | | |
|  | \* 85 Ohms ±10%: Target trace width/center-line pitch is 5.5mil / 12.5mil for **Internal** layers S6/8/17/19 | | | | | | |
|  | \* 85 Ohms ±10%: Target **Neck** trace width/center-line pitch is 4mil / 8mil for **Internal** layers | | | | | | |
|  | \* 85 Ohms ±15%: Target trace width/center-line pitch is 6mil / 14mil for **External** layers | | | | | | |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| b)     Single-ended traces: | | |  |  |  |  |  |
|  | \* 55 Ohms ±10%: Target trace width: 3.41 mils for **Internal** signal layers | | | | | |  |
|  | \* 55 Ohms ±15%: Target trace width: 4.5 mils for **External** signal layers | | | | | |  |
|  |  |  |  |  |  |  |  |
|  | \* 46 Ohms ±10%: Target trace width 4.8mils for **Internal** signal layers | | | | | |  |
|  | \* 46 Ohms ±15%: Target trace width 6 mils for **External** signal layers | | | | | |  |

## PCB Routing Requirements

### Fan-out

A screenshot of a computer

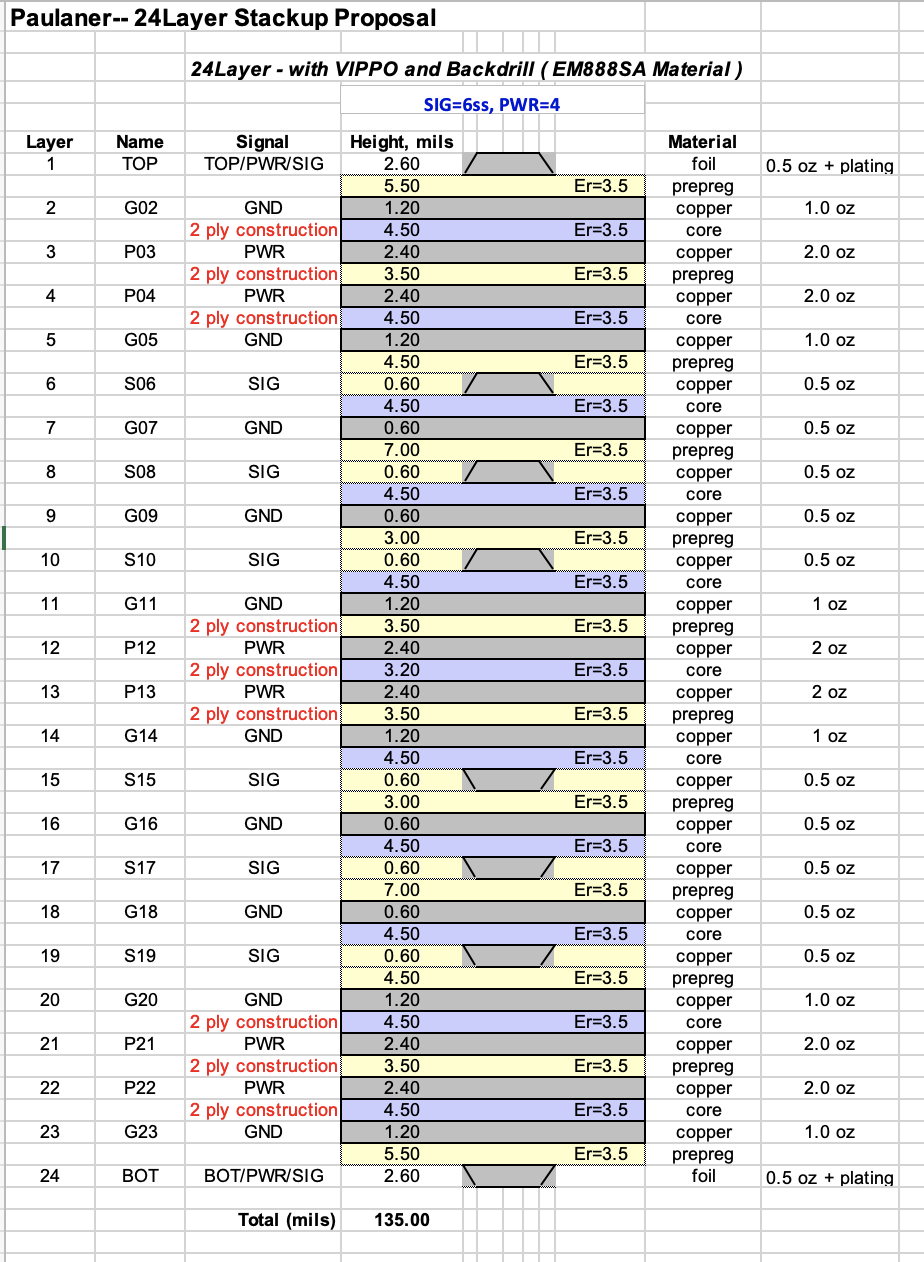
Description automatically generated with medium confidence

Since we are using belly-to-belly connectors, so both TX and RX are distributed on upper half and lower half signals layers in stackup, which will cause the crosstalk at BGA area. In order to decrease the crosstalk between differential pairs, we need to use the Single End signal for CDR5 fan out.

### Anti-pad for High-Speed SerDes Vias / Pins

since we need to use FHS 8mil in CDR5 BGA area, which will cause challenge for the impedance continuity at the pin and via area, so we must use different antipad type for different HSD routing layers.

## PCB Stackup



# Testing Considerations

Please refer Paulaner MFG Test Plan EDCS-xxxxx

# Testability Considerations

Due to the majority of the serdes links are high-speed signals where the performance and reliability are main concerns. For the SI (Signal Integrity) considerations, all signals classified as high-speed will not allow any test point, instead boundary scan become complementary to ICT and increasingly more important to cover the high-speed nets. The ICT (In-Circuit Test) team will generate the report for the nets didn’t have the test points and SI will go over to decide what is needed and what can be waived.

# Manufacturing Considerations

Engage with Cisco manufacture organization to define the test infrastructure, strategy, fixtures and process at early stage. The prototype as well as production will build with the same contract manufacture (CM) to ensure smooth transition. The following Cisco guideline shall be used as reference:

* EDCS-7004080 PCB Design for Test
* EDCS-14099 Generic Cisco ID PROM Specification
* EDCS-148959 GSM Risk Rating Procedure
* EDCS-586342 NPI Risk Analysis & Mitigation Process Flow
* EDCS-718998 Early DFx Engagement Model

# Estimated Costs

Please refer the latest BOM 800-106854-XX in Agile

# Requirements Traceability Considerations

**<<TL 9000: ADDITIONAL REQUIREMENT FOR TL 9000 COMPLIANCE>>**

Requirements traceability is required for TL 9000 registration. Traceability may be performed manually, or with assistance of automated software tools.

If the requirements in the SFS are not of sufficient detail to support traceability to test cases, you may need to trace the product requirements to the more detailed functional requirements specified in this HW functional specification. In this situation, provide unique identifiers for all functional requirements and trace product requirements to functional requirements consistent with your organization’s strategy for requirements traceability. If the project has a separate traceability matrix provide a link to that document.

Refer to the Common [Requirements Traceability Handbook EDCS-400506](http://wwwin-eng.cisco.com/protected-cgi-bin/edcs/edcs_attr_search.pl?doc_num=EDCS-400506) for a thorough description of traceability and some examples of a manual implementation.

# References

* *Red\_Dog HW Functional Specification, EDCS-23269899*
* *Red\_Dog IOFPGA Specification, EDCS-23050746*
* *Paulaner MIFPGA Specification, EDCS-23881782*
* *Paulaner Diag function specification, EDCS-23881806*
* *Paulaner Power budget, EDCS-xxxx*

# Standards

| Specification | Description | Country/product classification |
| --- | --- | --- |
| Safety | UL 60950 Second Edition CAN/CSA-C22.2 No. 60950 Second Edition EN 60950 Second Edition IEC 60950 Second Edition AS/NZS 60950  CNS14336 | USA – ITE  Canada – ITE  Europe – ITE  Europe – ITE  Australia/New Zealand – ITE  Taiwan – ITE |
| EMC - Emissions | 47CFR Part 15 (CFR 47) Class A  AS/NZS CISPR22 Class A  CISPR22 Class A  EN55022 Class A  ICES003 Class A  VCCI Class A  EN61000-3-2 EN61000-3-3  KN22 Class A  CNS13438 Class A | USA – ITE/TNE  Australia/New Zealand – ITE/TNE  International – ITE/TNE  Europe – ITE/TNE  Canada – ITE/TNE  VCCI – ITE/TNE  Europe – ITE/TNE  Europe – ITE/TNE  Korea – ITE/TNE  Taiwan – ITE/TNE |
| EMC - Immunity | EN55024 CISPR24  EN300386[[2]](#footnote-2)♣  KN24 | Europe – ITE  International – ITE  Europe – TNE (includes emissions)  Korea – ITE/TNE |

# Glossary

The following list describes acronyms and definitions for terms used throughout this document:

* **CPOL**: Cisco Patents On-line
* **Term 2 <in bold>**: **<**definition in plain text**>**

# Attachments

End of Document

1. There are 32x 400gbps MACs. Each MAC can be individually configured as 1x 400G port, 2x ports up to 200G, or 4x ports up to 100G, or 1x 200G + 2x up to 100G. In addition, each MAC has 8 multi-rate SERDES (up to 56g) so a valid break-out configuration can use no more than that. [↑](#footnote-ref-1)
2. [↑](#footnote-ref-2)