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Assignment-1

1**. Define analog, discrete time and digital signals.**

Ans:

Analog signal varies continuously between two amplitudes over the given interval of time. Between these limits of amplitude and time, the signal can take any value at any instant of time.

Discrete time signal varies between two given amplitudes, but its value within this range is sampled (or is available) only at discrete time intervals over the specified time range.

Digital signal also varies over the given amplitude limits and is sampled at discrete time intervals over the specified time range, but its amplitude cannot take any value in the given range, but only some specified values. The value it takes is closest to the value of the discrete-time signal at that particular instant of time.

2. What are some of the advantages digital systems compared to analog systems?

Ans:

Compared to analog systems, digital systems are more immune to noise. Because of this property, digital signals can be transmitted with less error. Digital systems are also more reliable because small changes in component values do not affect performance. They are easy to design and easy to replicate and hence performance improvement is easy to implement.

3. Convert the following numbers as required in each case.

123410 = (**10011010010**)2
25.62510 = (**11001.101**)2
603.2310 = (**1001011011.001110101**)2
ABCD16=(**1010 1011 1100 1101**)2
15C.3816=(**000101011100.00111000**)2

4. Explain the difference between positive logic and negative logic.

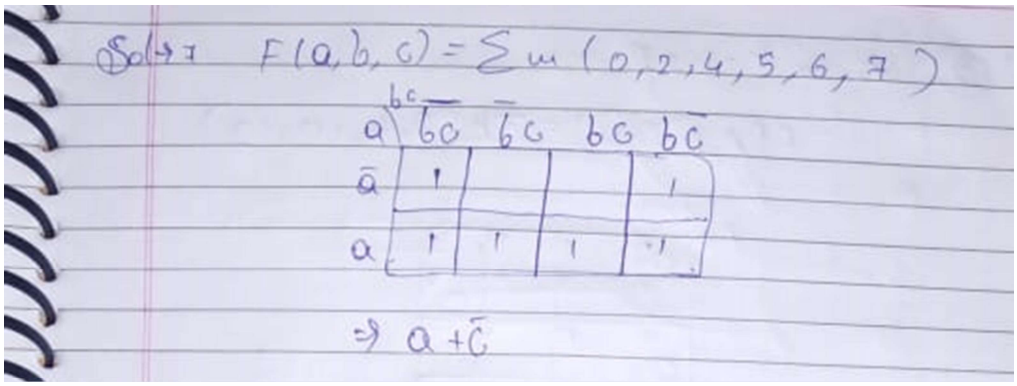
Ans:

In all digital systems and circuits two logic levels are defined, HIGH and LOW, sometimes called “1” and “0”. Taking the example of two voltage levels, in positive logic, the HIGH level is denoted by higher voltage, and the LOW level is denoted by lower voltage, e.g., 5 volts and 0 volts. In negative logic, on the other hand, the HIGH level is denoted by lower voltage and LOW level by higher voltage, e.g., 0 volts and 5 volts. In other words, the two are dual of each other. For example, an AND gate in positive logic will represent an OR gate in negative logic.

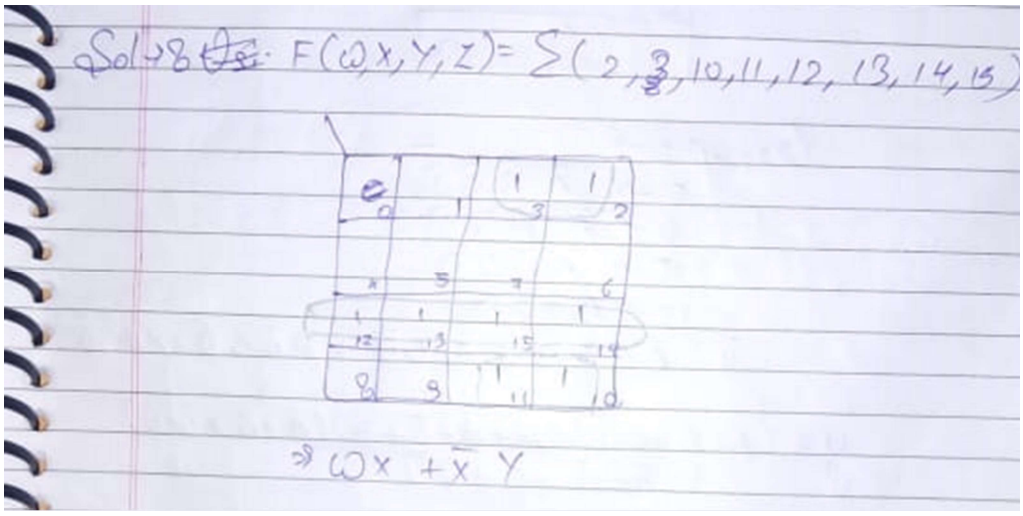
5. What are universal gates? Why are they called so?
Ans:
NAND and NOR gates are called universal gates. Normally any logic circuit will have AND, OR, INVERT gates. These three gates are required to implement any logic function. Individually either NAND or NOR gate can implement AND, OR, INVERT gates, and hence either one of them (NAND or NOR) can implement any logic function.

6. Use Boolean Algebra to show that A'BC'+AB'C'+AB'C+ABC'+ ABC = A+BC'
Ans:
A' BC + AB'C' + A'B'C' + AB'C + ABC
=>A' BC + AB'C' + AB'C' + A'B'C' + AB'C + ABC
=>A' BC + ABC + A'B'C' + AB'C' + AB'C' + AB'C
=>BC (A' + A) + B'C' (A' + A) + AB'(C' + C)
=>**BC + B'C' + AB'**

7. Using 3-variable K'Map simplify the Boolean function given by
F (a, b, c) = Σm (0, 2, 4, 5, 6, 7)
Ans:

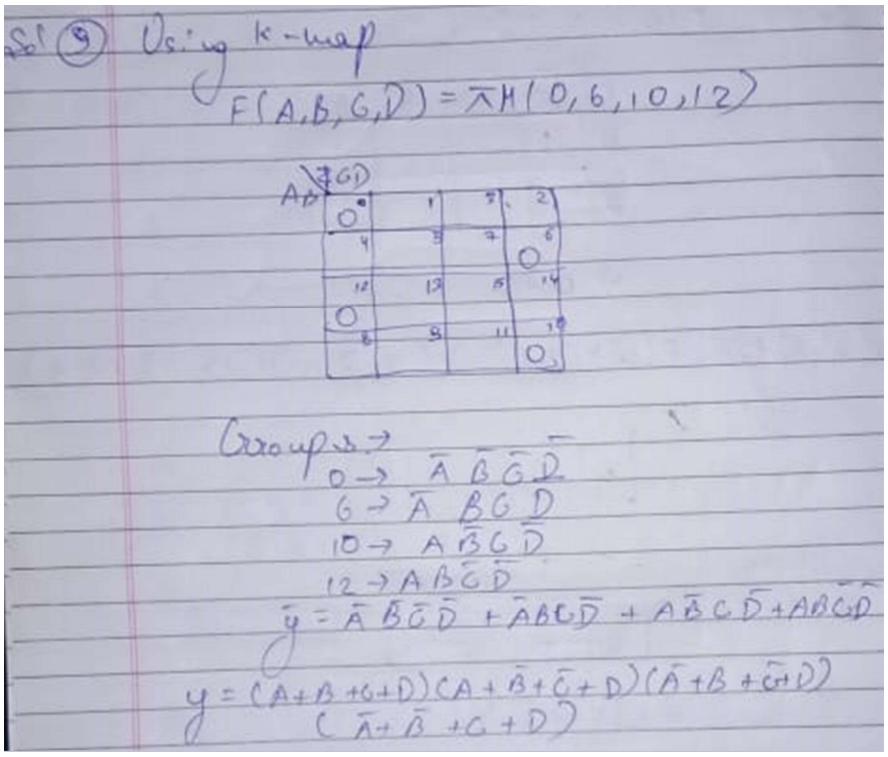


8. Using 4-variable K'Map simplify the Boolean function given by F (w, x, y, z) = Σm (2, 3, 10, 11, 12, 13, 14, 15)
Ans:



9. Using K'Map simplify in the product-of-sum form the function given by F(A,B,C,D} = ΠM (0, 6, 10, 12)

Ans:



10. How many bits are required to represent all the keys on a Keyboard with 108 keys?

Ans:

108 keys Minimum n=7, for which 108 ≤ 2n = 128 7 bits are required.

11. Design a circuit to generate odd parity if the data is represented with 4 bits.

Ans:

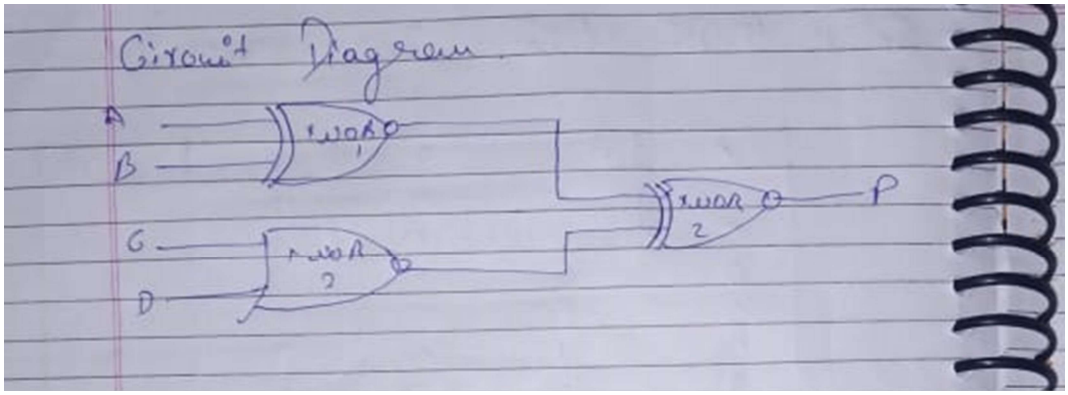
Sol → 4-Bit Odd Parity Generator

A	B	C	D	P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

→ Solving the truth table for all the cases with P using the SOP method we also use K-map to solve the output

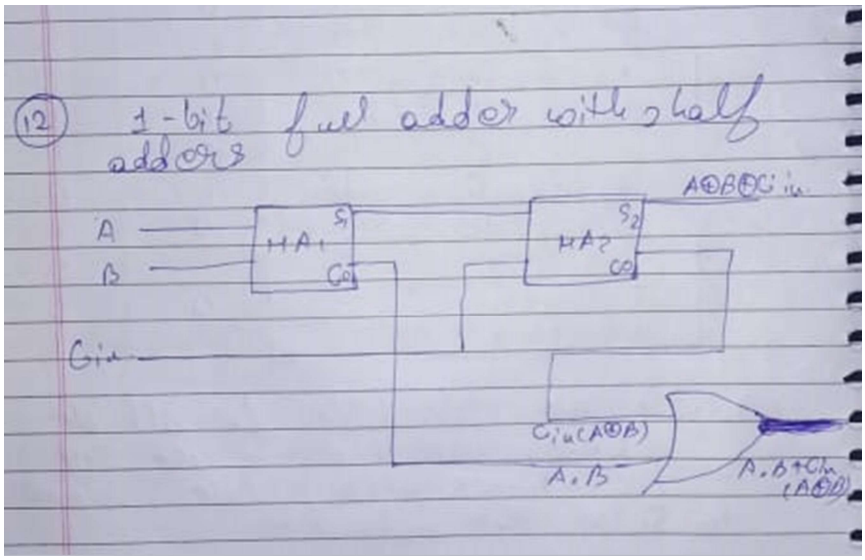
P = A EX-NOR B EX-NOR C EX-NOR

Circuit Diagram



12. Design a 1-bit full adder with two half adders and minimum number of additional gates.

Ans:



13. What is the significance of the equation C i+1 = Gi + PiCi in relation to Carry lookahead Adder? Define Gi and Pi.

Ans:

If Ai and Bi are the two bits to be added in the ith stage of a multi-bit adder, Gi = Ai. Bi and Pi = Ai EXOR Bi These parameters are used to predict Co of each stage if A and B of the stage are known using the first stage's Ciflip-flopsFlipn Ci+1 = Gi + Pi Ci is used to predict the carry out of ith stage if they carry-in of that stage is known, which in turn can be predicted recursively from the first stage

14. Write the 8-bit signed-magnitude, two's-complement, and ones'-complement representation for each decimal number:

a) +25

Ans:

Sign Magnitude:00011001 One's complement:00011001 2's complement:00011001

b) +120

Ans:

Sign Magnitude:01111000 One's complement:01111000 2's complement:01111000

c) +82

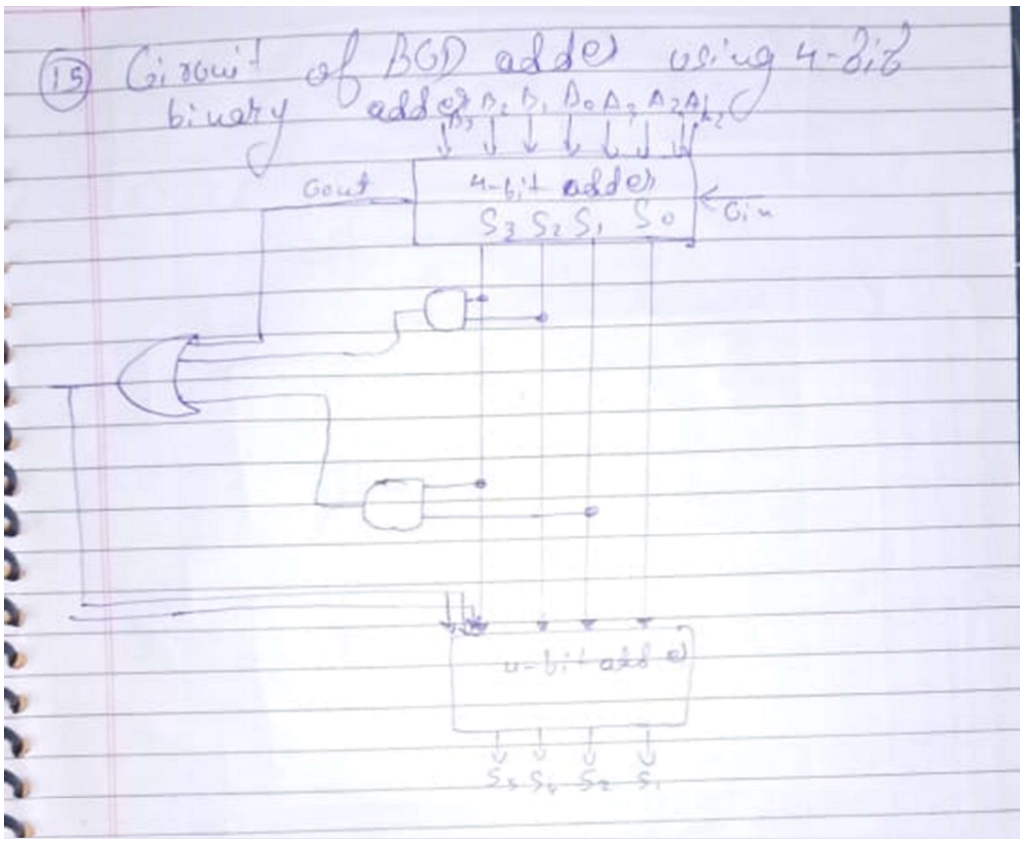
Ans:

Sign Magnitude:01010010 One's complement:01010010 2's complement:01010010

d) -42

Ans:
Sign Magnitude:10101010 One's complement:11010101 2's complement:11010110

15. Draw the circuit of a BCD adder using 4-bit binary adders
Ans:



16. Obtain the JK's flip-flop's excitation table, i.e. A JK flip-flop with an inverter between external input K' and internal input K.
Ans:
Characteristics table of JK' Flip-Flop

J	K'	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
0	1	1

Now we can easily form the Excitation table, which is drawn below:

Q(t)	Q(t+1)	J	K’
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

17. A set-dominate flip-flop has set and reset inputs. It differs from a conventional RS flip-flop in that an attempt to simultaneously set and reset results in setting the flipflop. Obtain the excitation table of such a flip-flop?
Ans:
Characteristic Table for Set Dominate flip flop:

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
0	1	1

Excitation Table :

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	X
1	0	0	1
1	1	X	X

18. Design a binary counter having the following repeated binary sequence. Use JK flipflops. 0, 1, 2
Ans:

State table

Present state			Next table			FF inputs		
A	B	C	A(t+1)	B(t+1)	C(t+1)	$J_A K_A$	$J_B K_B$	$J_C K_C$
0	0	0	0	0	1	0 x	0 x	1 x
0	0	1	0	1	0	0 x	1 x	x 1
0	1	0	0	1	1	0 x	x 0	1 x
0	1	1	1	0	0	1 x	0 x 1	x 1
1	0	0	1	0	1	x 0	0 x	1 x
1	0	1	1	1	0	x 0	1 x	0 x 1
1	1	0	0	0	0	x 1	x 1	0 x
1	1	1	x	x	x	x x	x x	x x

k map of J_A

A \ BC	00	01	11	10
0	0	0	1	0
1	x	x	x	x

$J_A = J_B$

k map for K_A

A \ BC	00	01	11	10
0	x	x	x	x
1	0	0	1	1

$K_A = B$

k map for J_B

A \ BC	00	01	11	10
0				
1				

$J_B = C$

A \ BC	00	01	11	10
0	x	x	1	0
1	x	x	x	1

$K_B = A + C$

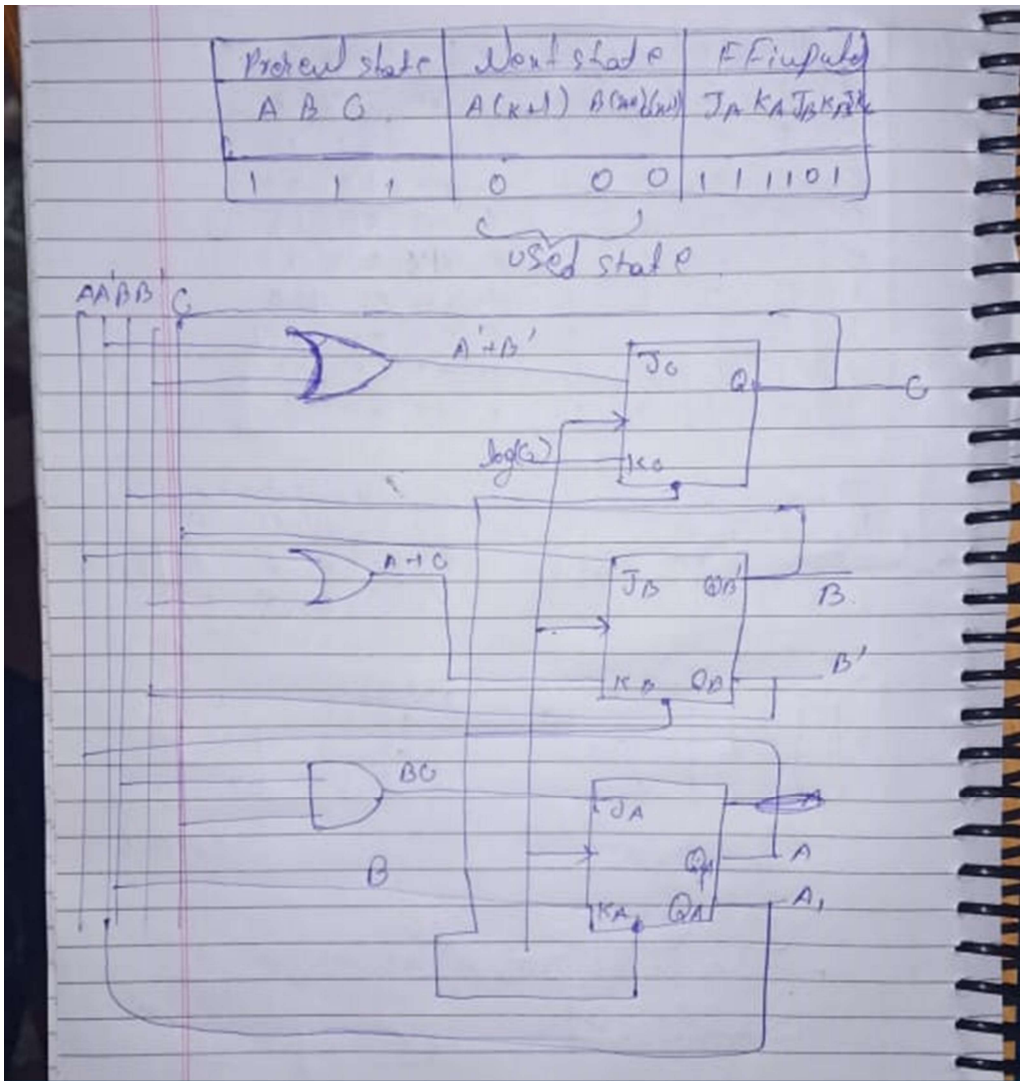
k map for J_C

A \ BC	00	01	11	10
0	1	x	x	1
1	1	x	x	0

J_C

A \ BC	00	01	11	10
0	x	1	1	x
1	x	1	x	x

$K_C = 1$



19. How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after the following count: 1001100111

Ans:

4 flip-flops

20. Explain the Master-Slave operation of a flip flop.

Ans:

Master-Slave flip fop is a set of two identical flip flops (of any type). The clocks of the two flip-flops are of opposite phases. i.e., if the clock of the Master is HIGH, that of the Slave is LOW and vice-versa. When there is a change in the input of the M-S unit, the output of the master changes when its clock is HIGH. This change can not be immediately transmitted to the Slave as its clock is LOW. When the clock of the Master becomes LOW, the clock of the Slave becomes HIGH and changes in the output of the Master are transmitted to the output of Slave, which is the output of the M-S unit. The purpose of this arrangement is to make sure that the output of the flip

flop changes only once in a clock cycle, irrespective of the number of changes in the input.