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M.Sc. (Second Semester)
EXAMINATION, MAY-JUNE, 2022
COMPUTER SCIENCE
Paper Fifth (IV)
(Elective)
(Advanced Computer System Architecture)

Time : Three Hours] *[Maximum Marks:100*

[Minimum Pass Marks:40

Note:- Attempt all sections as directed.

Section-A

(Objective/Multiple Choice Questions)

(1 mark each)

Note:- Attempt all questions.

Chose the correct answer-

1. In the absolute adderssing mode?

   (A) The operand is inside the instruction

   (B) The address of the operand is inside the instruction

   (C) The register containing address of the operand is specified inside the instruction

   (D) The location of the operand is implicit.

2. Main memory stores_____and _____ .

   (A) Data instruction

   (B) Data address

   (C) Address instruction

   (D) None of the above

3. Full form of UMA?

   (A) Undefined Memory Access

   (B) Uniform Memory Access

   (C) Unidentified Memory Access

   (D) Unified Messaging Application

4. 7 lynn's classification is based on

   (A) Serial

   (B) Parallel

   (C) Both (A) and (B)

   (D) None of these

5. Full form of NORANA?

   (A) No Random Memory Access

   (B) Normal Memory Access

   (C) No Remote Memory Access

   (D) None of these

6. Pipeling is a _____technique.

   (A) Serial operation

   (B) Parallel operation

   (C) Scalar operation

   (D) Super scalar operation

7. Parallelism can be achieved by _____technique.

   (A) Hardware

   (B) Compiler

   (C) Software

   (D) All of the above

8. Which one most appropriate static system?

   (A) $y(n) + y(n-1) + y(n+1)$

   (B) $y(n) + y(n-1)$

   (C) $y(n) = x(n)$

   (D) $y(n) + y(n-1) + y(n+3) = 0$

9. Which of the following is not true about RISC processors?

   (A) Addressing modes are less

   (B) Pipelining is key for high speed

   (C) Microcoding is required

   (D) Single machine cycle instruction

10. When an instruction depends on the results of the previous instructions then

    (A) Error occurs

    (B) Software fault occurs

    (C) Data dependency occurs

    (D) Hardware fault occurs

11. These important feature of the VLIW is-

    (A) ILP

    (B) Cost effectiveness

    (C) Performance

    (D) None of the above

12. The parallel execution of operations in VLIW is done according to the schedule determined by-

    (A) Task scheduler

    (B) Interpreter

    (C) Complier

    (D) Encoder

13. One instruction tries to write an operand before it is written by previous instruction this may lead to a dependency called-

    (A) True dependency

    (B) Anti-dependency

    (C) Output dependency

    (D) Control Hazard

14. The CISC stands for

    (A) Computer instruction set compliment

    (B) Complete instruction set compliment

    (C) Computer indexed set components

    (D) Complex instruction Set computer

15. From where interupts are generated?

    (A) CPU

    (B) Memory chips

    (C) Registers

    (D) I/0 devices

16. In CISC architecture most of the complex instructions are stored in-

(A) Register

(B) Diodes

(C) Coms

(D) Transistors

17. Which architecture supports more than one processor working on more than one data stream?

(A) SISD

(B) SIMD

(C) MISD

(D) MIMD

18. Which architecture uses the least power?

(A) SISD

(B) SIMD

(C) MISD

(D) MIMD

19. In the threads model of parallel programming-

(A) A single process can have multiple, concurrent ex-exeution paths

(B) A single process can have single, concurrent ex-ecution paths.

(C) A multiple process can have single concurrent ex-ecution paths.

(D) None of these

20. Non-Uniform Memory Access (NUMA) is-

(A) Here all processors have equal access and access times to memory.

(B) Here if one processor updates a location in shared memory, all the other processors know about the update.

(C) Both (A) & (B)

(D) None of the above

Section- B

(2 marks each)

(Very Short Answer Type Questions)

Note:- Attempt all questions.

1. What is CISC?
2. Define COMA.
3. What are the common component of a Multiprocessor?
4. What static 2 dynamic system?
5. What is delay?
6. What is Hazard detection?
7. Define bitonic sort.
8. What is SIMD?
9. What is linear plpelining?
10. What is Hazard detection?

Section-C

(3 marks each)

(Short Answer Type Questions)

Note:- Attempt all questions.

1. Why symmetric shared memory architecture is called as UMA?

2. Differentiate RISC and CISC instruction set in pipeline.
3. Define pipelining with example.
4. Give an idea of dynamic scheduling.
5. How can you measure the performance of a computer system?
6. Difference between linear and non-linear pilelining.
7. Give basic instruction & floating point instruction formats.
8. What is instruction level parallelism?
9. Explain Benchmarking.
10. What is Blocking? Explain.

Section-D

(6 marks each)

(Long Answer Type Questions)

Note:- Attempt *any five* questions.

1. Write short notes on the following:
   (A) Parallel computers
   (B) Memory models
2. What is hazard detection and resolution?
3. Explain VLIW in detail.
4. Explain parallel Algorithm.

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5. How SIMD processors are differ from MIMD processors? Explain.
6. Briefly explain the characteristic of CISC architecture.
7. Explain virtual memories and its mapping schemes.
8. Explain the hazards of pipeline processing.