StaRFIshrail I2C for driving readers.

The StaRFIshrail readers use a SLRC61003 chip from NXP, and the base datasheet is SLRC610, as there are variants, such as the SLRC61002. This document describes the I2C sequence which is needed for setting up the device, and the sequence for continuously reading the RFID tags.

There are 4 I2C slave addresses available on the SLRC61003, which are set in the upper 7 bits of the address field, the lowest bit of the address field is 0 for write, and 1 for read. The 7 bit slave addresses are 0x28,0x29,0x2a and 0x2b.

So, for address 0x28, the 8 bit address for write is 0x50, and the 8 bit address for read is 0x51. Note also that the SLRC61003 is auto-incrementing,

For a single reader, any of 0x28,0x29,0x2a,0x2b can be selected by the 2 pole switch. One the dual reader, either 0x28 and 0x29, or 0x2a and 0x2b, can be selected by the single pole switch.

On the quad reader, 0x28,0x29,0x2a and 0x2b are present.

So, for the reader chip with slave address 0x28, the following set up procedure needs to be done once only, when a reader is detected as being powered on.

The first double hex digit on each line is a "start" byte, and the last double hex digit on each line is an "end" byte.

0x50, 0x02, 0xb0 Fifo control

0x50,0x05,0x00,0x00 Fifo data and IRQ0 control

0x50,0x00,0x0d Command 0x50,0x02,0xb0 Clears Fifo

0x50,0x05,0x01

0x50,0x00,0x0c, Loads registers

You may need a short (500uS) delay here, to let the registers load

0x50,0x00,0x06 Sets RF On

0x50,0x28,0x8f

0x50,0x37,0x14 Sensitivity

0x50,0x44,0x40 Sets pin 22 to output

The loop that needs to be implemented is

0x50,0x04 Set SLRC61003 address to 0x04 for read 0x51,0x00 Data coming back indicates length in FIFO 0x50,0x05 Set SLRC61003 to 0x05 to read FIFO,

0x50,0x0a Set SLRC61003 to read address 0x0a

0x51,0x00 Reads error flag

0x50,0x45,(led status, 0x40 or 0x00) Write data to LED

0x50,0x02,0x80 Flush Fifo buffer

0x50,0x05,0x76,0xa0,0x04,0x00,0x00,0x00,0x00 Write Fifo with ASK UID

0x50,0x00,0x07 Set to transceive

Wait approximately 8mS for RFID transaction to take place

Repeat

The StaRFIshrail system works at 200KHz I2C clock frequency, as this gives the best compromise between length if I2C bus, and speed of reading. A complete read loop takes 11mS – the actual time taken for the commands in the loop is 2.75mS – there is a little padding in places, and therefore by interleaving 4 loops, 4 readers can be commoned on one I2C bus, each reading at 11mS intervals.

In the StaRFIshrail system, the I2C sequencing is handled by the Xilinx FPGA, and once set up by the processor during the startup routine, needs no further intervention from the processor. If the result of reading register 0x04 is 13, and the result of reading register 0x0a is 0x00, then the UID read is valid. The UID number is the first five bytes of read from the Fifo, in reverse order.