Power Handling Analysis of High-Power W-Band All-Silicon MEMS Phase Shifters

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***Abstract*—This paper analyzes the power handling capability and the thermal characteristics of an all-silicon dielectric-block microelectromechanical-system (MEMS) phase-shifter concept, which is the first MEMS phase-shifter type whose power handling is not limited by the MEMS structures but only by the transmission line itself and by the heat-sink capabilities of the substrate, which enables MEMS phase-shifter technology for future high-power high-reliability applications. The power handling measurements of this concept are performed up to 43 dBm (20 W) at 3 GHz with an automatic gain-controlled setup, assisted by a large-signal network analyzer, and the temperature rises of the devices were measured with an infrared microscope camera. The measurement results are extended to 40 dBm at 75 GHz by calibrating electrothermal simulations with the measurements. A comparative study to conventional state-of-the-art MEMS phase-shifter concepts based on thin metallic bridges is carried out. The simulated results show that the all-silicon phase-shifter designs have the maximum temperature rise of only 30 °C for 40 dBm at 75 GHz, which is 10–20 times less than conventional MEMS phase shifters of the comparable RF performance.**

***Index Terms*—microwave, millimeter wave, phase shifter, radio-frequency microelectromechanical systems (RF MEMSs).**

I. Introduction

MICROWAVE phase shifters are nowadays widely utilized in many high-performance wireless communication and remote sensing systems, including radar sensors based on phased antenna arrays.

Radio-frequency microelectromechanical-system (RF MEMS) phase shifters are well-known for their near-ideal behavior, including very low losses, high linearity, and ease of integration and miniaturization, as compared with other technologies [1]. MEMS switched-line networks offer a good RF performance up to the 40-GHz Ka-band [2]–[7] but have high losses at higher frequencies, as demonstrated in [8], because the performance of multiple switches and the necessary length and discontinuities of the transmission line degrade the performance. Distributed MEMS transmission-line (DMTL) phase shifters offer better performances at millimeter-wave frequencies [9]–[14].

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However, these two conventional MEMS phase-shifter concepts have very limited power handling capability since thin moveable metallic bridges are utilized either for MEMS switches in switched-line phase-shifter designs or for MEMS switched capacitors in DMTL designs. At high signal power, particularly at high frequencies, the induced current density in the thin metallic bridges increases, resulting in a high temperature rise in the freestanding bridges. For commonly used metals such as gold, even only slightly elevated temperatures of 80 °C lead to degraded elastic properties [15]–[17], altering the actuator's performance and reducing the lifetime [18]–[20]. Other metals such as aluminum and platinum [21]–[23], and particularly molybdenum [24], [25] have better elasticity properties at elevated temperatures but experience increased heating and RF losses due to lower electrical conductivity, as compared with gold.

The authors have recently reported on a MEMS phase-shifter concept, which does not require any metallic bridges but is based on loading the transmission line with a dielectric block [26], [27]. This paper analyzes the thermal characteristics and the power handling capability of this recently proposed concept in comparison to conventional MEMS phase shifters. This new concept is the first and, so far, only MEMS phase-shifter concept whose power handling is not limited by the MEMS structures but only by the transmission line itself and by the heat-sink capabilities of the substrate, enabling the MEMS phase-shifter technology for high-power high-reliability applications. Although the recently proposed concept offers excellent RF and mechanical performance at the millimeter-wave frequencies, this concept is however less suitable at the low-frequency bands due to the large size of the phase shifter.

II. Phase-Shifter Concept and Comparisons to Conventional Designs

The schematically functional drawings and concept comparisons of the two conventional MEMS phase-shifter concepts and the recently reported unconventional concept are presented in Fig. 1. The two conventional concepts employ air-suspended thin metallic bridges, either for capacitive switches in a switched-line network in Fig. 1(a) or for the capacitive loading of the coplanar waveguide (CPW) as in the DMTL concept in Fig. 1(b). The thin metallic bridges employed in these conventional designs are the bottleneck in terms of power handling. The bridges must be relatively thin for acceptable actuation voltages, which results in high current densities at elevated power levels, particularly at higher frequencies. These

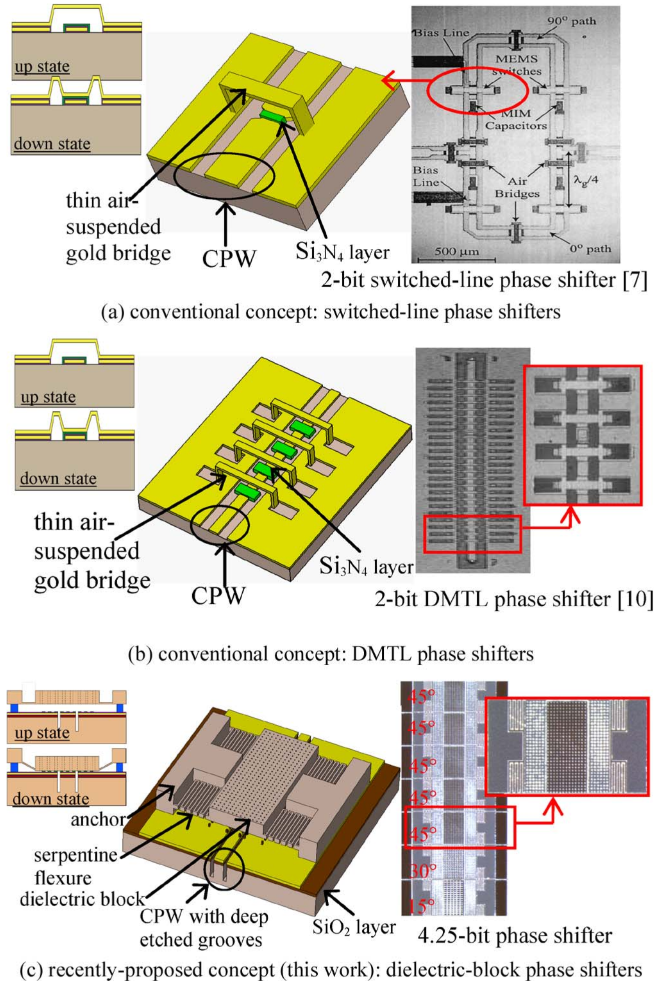

Fig. 1. Operational concept comparison among the (a) switched-line network, (b) the DMTL phase shifter, and (c) the dielectric-block phase shifter (this paper).

high power densities, in connection with the poor thermal conductivity of the freestanding bridges to the substrate heat sink, result in a large temperature rise of the bridges [28]. The electrical resistance of the gold bridges also increases with the temperature and the frequency, resulting in a much higher temperature rise, particularly in the downstate position of the gold bridges. Even at slightly elevated temperatures of 80 °C, the mechanical elasticity of the bridges (particularly when made of gold, which is the most commonly used material) degrades, resulting in the altered actuation behavior and the drastically limited lifetime. At even higher temperatures, significant thermomechanical deformations of the gold bridges occur, resulting in serious reliability issues including permanent plastic deformation, thermal-strain-induced buckling, creeping, or even melting of the gold bridges.

Furthermore, most of the MEMS phase shifters are fabricated on quartz or glass to minimize substrate losses but offer bad thermal properties. For example, fused quartz has approximately 111-times lower thermal conductivity, as compared with silicon [29]. Thus, the fused-quartz substrate acts as a bad heat sink for the thin movable gold bridges. This also greatly limits the power handling capability of the conventional phase-shifter designs. Although the conventional concepts presented in this paper are fabricated with a CPW transmission line, the implementation with a microstrip line was studied [29], and the results are similar to the CPW design.

The all-silicon phase-shifter concept developed by the authors and shown in Fig. 1(c) employs vertically moving dielectric blocks for tuning the effective dielectric constant of the transmission line and, thus, the wave propagation speed, which creates a linear phase shift. Metallic losses are only caused in the t-line itself, as the moving dielectric blocks are subject to very minor dielectric losses only. High-resistivity ($> 4000\ \Omega \cdot \mathrm{cm}$) silicon block with a loss tangent of 0.0006 ($\pm 50\%$ error) was measured at 75 GHz, and a measured dielectric constant of 11.9 is used for the dielectric block, providing excellent RF properties. The silicon block offers the possibility of tailor making the dielectric constant by varying an etch-hole pattern in the block, which can be utilized for binary-coded phase-shifter stages, as previously reported by the authors [26].

All mechanically moving parts, i.e., the dielectric block, the suspending springs, and the anchors, are fabricated out of a single monocrystalline-silicon block, i.e., a concept that offers the best possible mechanical reliability in the microsystem technology.

The micromachined CPW is fabricated on a low-loss high-resistivity silicon substrate, which is also an excellent heat sink for the power dissipated in the transmission line. Because of this concept eliminating the metallic bridges and the all-silicon design, the dielectric-block phase shifter is more suitable for high-power and high-frequency applications, as the power handling is only limited by the transmission line and not by any MEMS moving part. Even more, this concept offers a better RF performance over the whole W-band, as compared with all previously published conventional MEMS phase shifters on any substrate, including quartz and glass [26]. Although this concept also introduces the change in the characteristic impedance between the upstate and downstate positions of the dielectric blocks, no huge mismatch was observed during the measurement because the reflections are very small [26], [27]. Furthermore, as the dielectric block can be made much stiffer, this concept has increased the robustness to self-actuation since the calculated ratio between the active- and self-actuation areas is 8, which is much higher than 1 as in the conventional designs.

III. SUMMARY OF RF PERFORMANCE AND MEMS RELIABILITY CHARACTERISTICS

The RF performance and nonlinearity characteristics have been recently published by the authors [26] and are summarized as follows. For a 5.51-mm-long 4.25-bit binary-coded phase-shifter prototype, the return and insertion losses at the nominal frequency of 75 GHz are -17 and -3.5 dB, respectively. For the whole W-band, it performs with a return loss better than -15 dB and an insertion loss better than -4 dB. These data correspond to phase-shifter efficiency values of -0.82 dB/bit and 71.1°/bit at 75 GHz, and -0.94 dB/bit and 98.3°/bit at 110 GHz. This proposed concept is exceptional broadband even outside the W-band. The measured phase error from 10 to 110 GHz is better than $\pm 3\%$ for all states, and the linearity is excellent with a measured third-order intercept point of

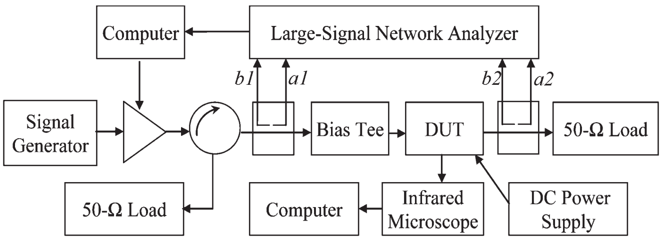

Fig. 2. High-power measurement setup with infrared microscope and large-signal network analyzer with input power up to 43 dBm (20 W) at 3 GHz. The dielectric-block phase shifter is placed on a temperature-controlled chuck with a constant temperature at 65 °C.

49 dBm. The binary-coded MEMS phase shifter presented in this paper has better insertion loss per bit and better return loss than any W-band phase shifters previously reported, both for their respective nominal frequency and for the whole W-band.

The mechanical reliability of the dielectric-block phase shifter was evaluated. All tested phase shifters (pull-in voltage of 29.9 V) survived one billion cycles. Neither stiction nor any tendency of changing of the pull-in voltage was observed, which proves their low susceptibility to dielectric charging. The detailed information of the MEMS actuation and reliability characterization is found in [27].

IV. Power Handling Measurements and Analysis

A. Automatic-Gain-Controlled Measurement Setup

The block diagram of the high-power measurement setup is shown in Fig. 2. The setup is composed of a signal generator connected to a 3-GHz tunable solid-state power amplifier with a maximum tuning rage up to 46 dBm (40 W). A circulator is employed in the setup to protect the power amplifier from the reflected signal; thus, the reflected power is dissipated at a 50-Ω termination connected at the other port of the circulator. Four directional couplers are required to detect the transmitted and reflected signals at the input (a_1 and b_1) and output (a_2 and b_2) ports of the phase shifter. These parameters are used for controlling and stabilizing the gain of the power amplifier to the required RF power level at the input port of the device under test (DUT) by the large-signal network analyzer. Although the direct-current (dc) blockage during the actuation is not required in the setup since the dc probes were launched on the spring anchor and the CPW ground, unlike most of the conventional designs where the actuation probes are placed on the signal line and ground, the bias-tee circuit was placed in the setup to protect the measurement system from all possible dc leakages. The dielectric-block phase shifter is placed on a temperature-controlled chuck to establish the temperature stabilization of the DUT to 65 °C, protecting the measurement environment from the unwanted external heat source. Finally, another 50-Ω load is required to dissipate the power at the end terminal of the measurement setup. The feedback automatic-gain-controlled setup in this paper is more reliable than the commonly used setup [30] where the input RF power at the terminal of the device can drastically alter from the required level by power losses at the circulator, bias-tee circuit, t-line, and RF probes.

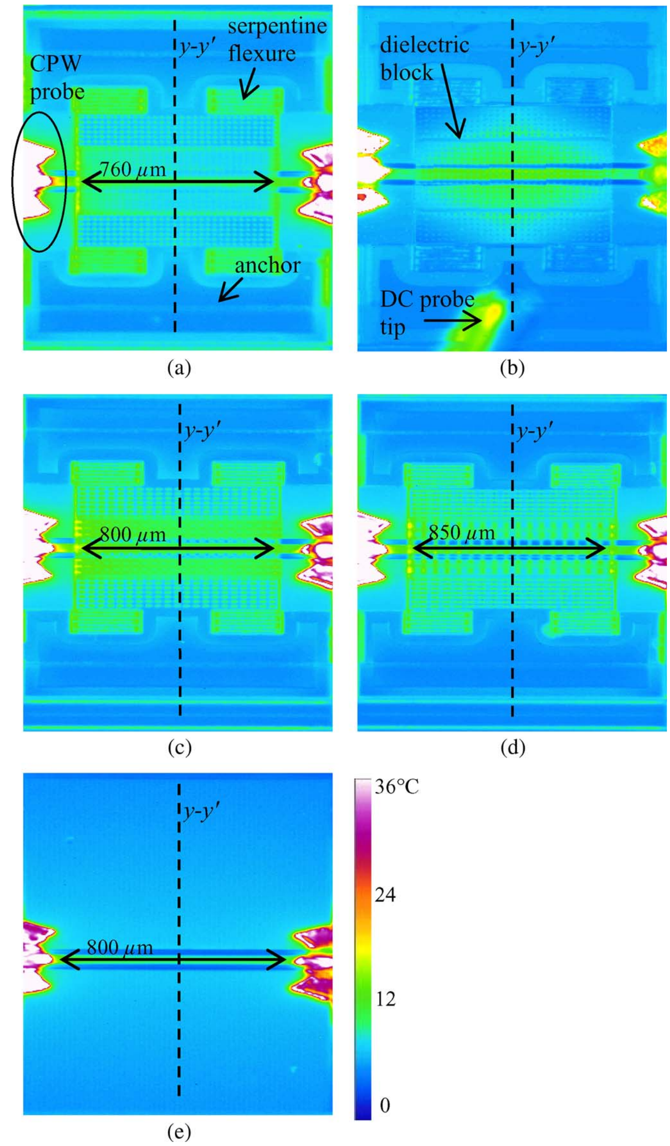

Fig. 3. Top-view infrared-microscope pictures of the 45°, 30°, and 15° single-stage phase shifters (The phase-shift values of 45°, 30°, and 15° are offered at 75 GHz) with 40-dBm (10 W) signal power at 3 GHz. The color scale is for all plots. The measured and simulated cross-sectional plots $(y{-}y')$ of the temperature rise are presented in Fig. 5. (a) 45° (upstate), (b) 45° (downstate), (c) 30° (upstate), and (d) 15° (upstate) single stages. (e) t-line without block (single stage).

B. Thermal Characterization Under High RF Power Up to 43 dBm (20 W) at 3 GHz

Fig. 3 shows the top-view infrared-microscope pictures of the 45°, 30°, and 15° single-stage phase shifters with the input power of 40 dBm (10 W) at 3 GHz. The measurement results along the $y{-}y'$ line show that the maximum temperature rise of the 45° single-stage in the upstate position is 10.56 °C and 12.19 °C for the downstate position. The hottest spots with the input signal power of 37 and 43 dBm (5 and 20 W) in the upstate are 6.37 °C and 27.28 °C, respectively. For the 30° and 15° single stages, the peak temperature increases at 40 dBm in the upstate position are 11.75 °C and 11.67 °C, respectively, while the hottest temperature rise of the unloaded CPW without the dielectric block is only 10.77 °C. These hotspots are located on

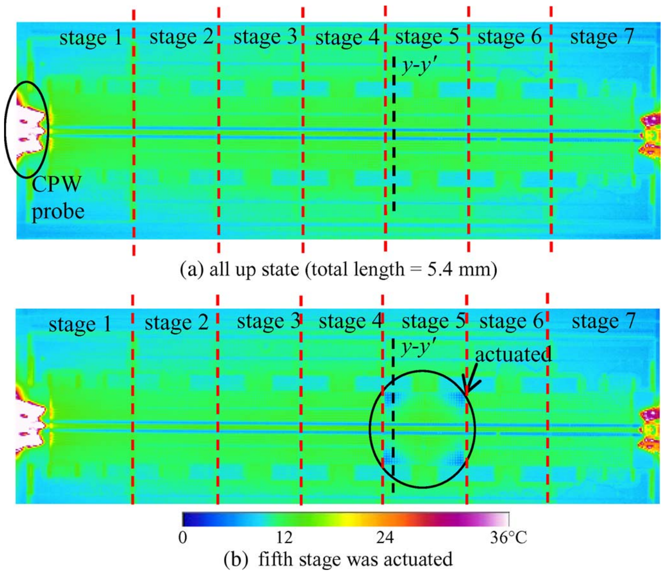

Fig. 4. Top-view infrared-microscope pictures of the $7 \times 45°$ multistage dielectric-block phase shifters with 40-dBm (10 W) signal power at 3 GHz. (a) All stages are in the upstate position. (b) The fifth stage is in the downstate. All pictures have the same color scale. The cross-sectional plots $(y{-}y')$ of the temperature rise are presented in Fig. 5.

the signal line of the gold CPW, which are determined by the skin effect and the input power of the signal line.

The thermal measurements of the $7 \times 45°$ linear-coded multistage phase shifter are presented in Fig. 4. For all silicon blocks in the upstate position, the peak-temperature rise along the $y{-}y'$ line is 11.06 °C and 10.63 °C when the fifth-stage silicon block is actuated, i.e., pulled down. The hottest spots occur on the signal line of the CPW, which are determined by the skin effect and the power level of the input RF signal. As shown in Fig. 4(b), the actuated silicon block performs as an additional heat sink of the devices, resulting in a temperature rise of approximately 3 °C lower at the corners of the silicon block, as compared when it is in the upstate position.

The $y{-}y'$ cross-sectional plots of the 45° single stage, both in the upstate and the downstate, as compared with the unloaded t-line, and the $7 \times 45°$ linear-coded multistage phase shifters are presented in Fig. 5(a) and (b), respectively.

C. Comparison of Simulation Results and Automatic-Gain-Controlled High-Power Measurements

The measurement results at 3 GHz with the signal power of 40 dBm (10 W) in Fig. 3 were mapped by the RF/electrothermal simulations (CST Studio Suite), and the simulation parameters were calibrated from both microwave and thermal measurement results. Fig. 6 shows the simulated temperature rise of the cross-sectional $y{-}y'$ of the phase shifter with the thermal contour plot. In the upstate position, the temperature rise of the phase shifter is 9 °C and is distributed uniformly across the suspended silicon block. In the downstate, the thermal resistance between the movable silicon block and the structures underneath (t-line and substrate) decreases, resulting in much better heat-flow properties. Thus, heat can flow from the heat source (signal line) through the middle of the movable silicon block and flows

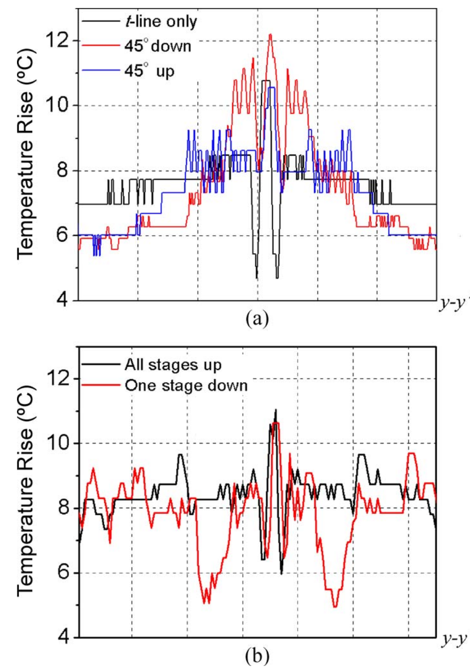

Fig. 5. The cross-sectional plots $(y{-}y')$ of the temperature rise: (a) 45° single-stage phase shifter compared with the t-line from Fig. 3; (b) Multistage phase shifter in Fig. 4. The high-power measurement is performed at 3 GHz and 40 dBm (10 W).

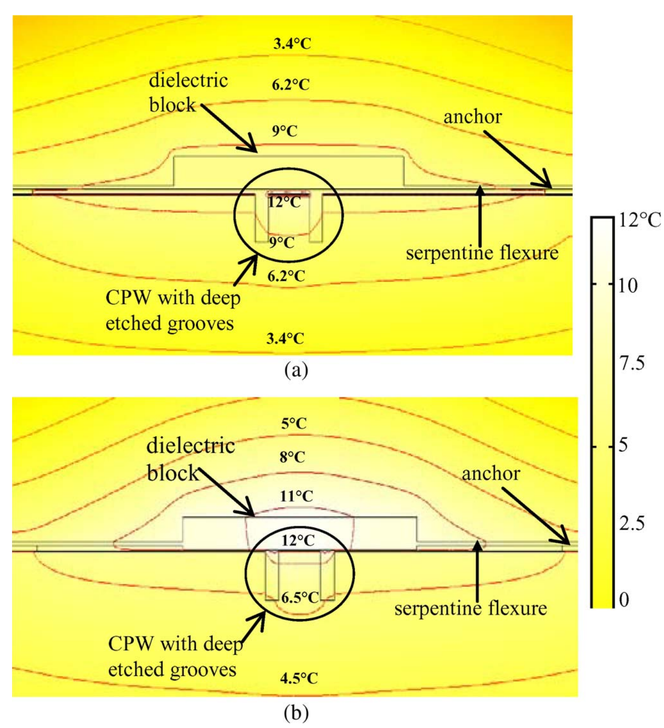

Fig. 6. Simulated results at 3 GHz and 40-dBm power of the 45° single stage with contour plots of the temperature-rise distribution of cross sections of the dielectric-block phase shifters. (a) Upstate and (b) downstate positions.

to the heat sink (substrate) at the edges where the temperature is slightly lower. Therefore, the temperature-rise distribution decreased from 12 °C in the middle of the silicon block to 8 °C at the edges.

To fully correlate the thermal simulations with the infrared measurements, it must be understood that silicon is considered

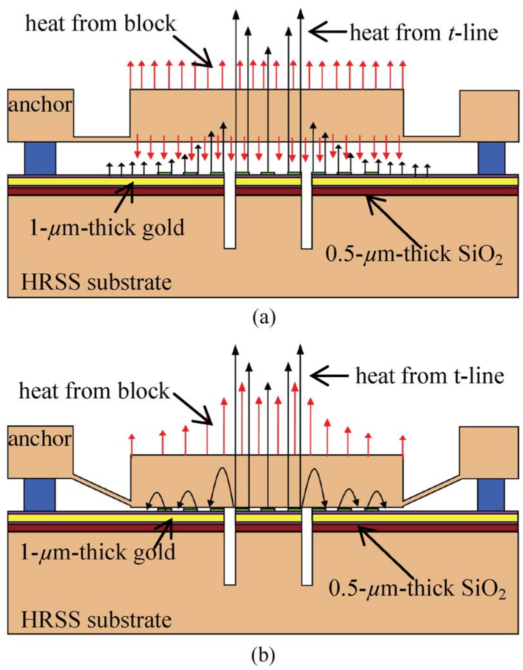

Fig. 7. Demonstrations of heat-transfer characteristics of the dielectric-block phase shifter under infrared microscope measurement. (a) Upstate and (b) downstate positions.

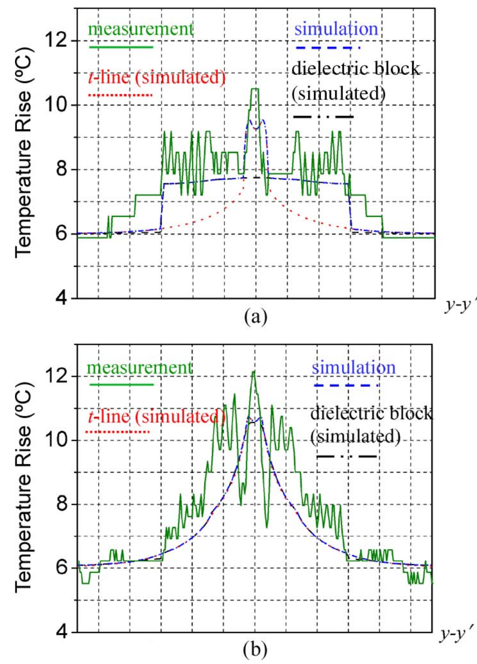

Fig. 8. Temperature-rise distribution comparisons (at 3 GHz and 40-dBm power) between simulated and measured results of the cross section $y-y'$ of the 45° single-stage dielectric-block phase shifters. (a) Upstate and (b) downstate positions. The simulated maximum temperature rise was calculated by the maximum value between the temperature rise of the t-line and the dielectric block.

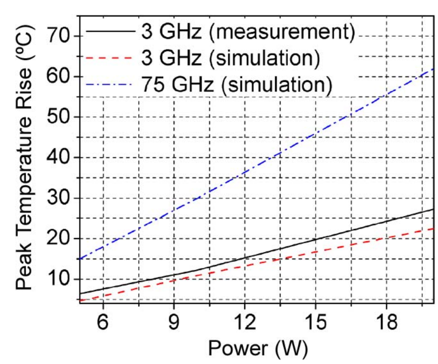

Fig. 9. Comparison of the peak-temperature rises of the 45° single-stage dielectric-block phase shifter with the power sweep from 37 to 43 dBm (5–20 W) at 3 and 75 GHz.

to have good transparency at the infrared wavelength. However, due to the lattice vibration, impurity, free-carrier absorption, plasma resonance, and surface roughness, the transparency in silicon can decrease up to 50% [31]. Thus, the movable silicon blocks of the phase shifters are partially transparent during the thermal power measurements with an infrared microscope camera. Therefore, the temperature measured by the infrared camera in Figs. 3 and 4 consists of two infrared-radiation components: 1) the emission of the heated transmission line due to metallic losses, which is radiated through the silicon block, and (2) the actual temperature radiation of the air-suspended silicon block itself, as illustrated in Fig. 7. From the simulation, the thermal results were mapped, and the two components for the silicon block and the CPW were extracted. The superposition of these two components agrees well with the measurements. Fig. 8 plots the measured temperature rise of the 45° single-stage phase shifter, both in the upstate and the downstate, with the comparison to the simulated results from CST Studio Suite.

D. Extension of Thermal Characteristics to 75 GHz

As no power sources of 10 W at 75 GHz were available, the temperature rise at the 40-dBm (10 W) signal power was measured up to 3 GHz, and these measurement results were used as calibration points for mapping RF/thermal simulations, done with CST Studio Suite, from 3 up to 75 GHz. Thus, frequency-dependent thermal effects such as increased metallic losses and skin effect are taken into account.

Fig. 9 shows the comparison of the measured and simulated peak-temperature rises of the 45° single-stage dielectric-block phase shifter at 3 GHz with a power sweep from 37 to 43 dBm (5–20 W). The extended results of the maximum temperature rise at 75 GHz are also plotted. The cross-sectional plot of the temperature rise of the 45° single-stage dielectric-block phase shifter is shown in Fig. 10.

V. Comparisons of the Power Handling Capability to Conventional MEMS Phase-Shifter Concepts

A comparative study of the thermal heating induced by the RF power was carried out for the all-silicon MEMS phase-shifter concept, in comparison with the two conventional MEMS phase-shifter concepts (DMTL and switched-line concepts).

Fig. 11 shows a comparison of the simulated temperature rise of single MEMS phase-shifter modules of the three concepts at 75 GHz and 40-dBm signal power for both discrete states (up and down positions). The geometry and material parameters of the switched-line and DMTL W-band phase shifters for the RF

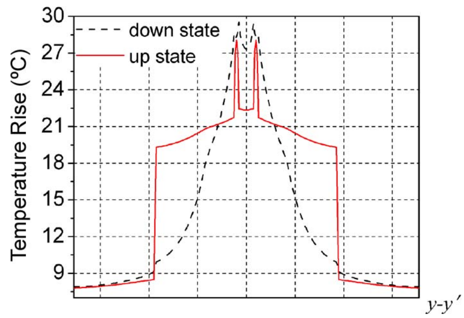

Fig. 10. Simulated temperature rise of the 45° single-stage phase shifter, $y-y'$ plot, with 40-dBm (10 W) RF power at 75 GHz.

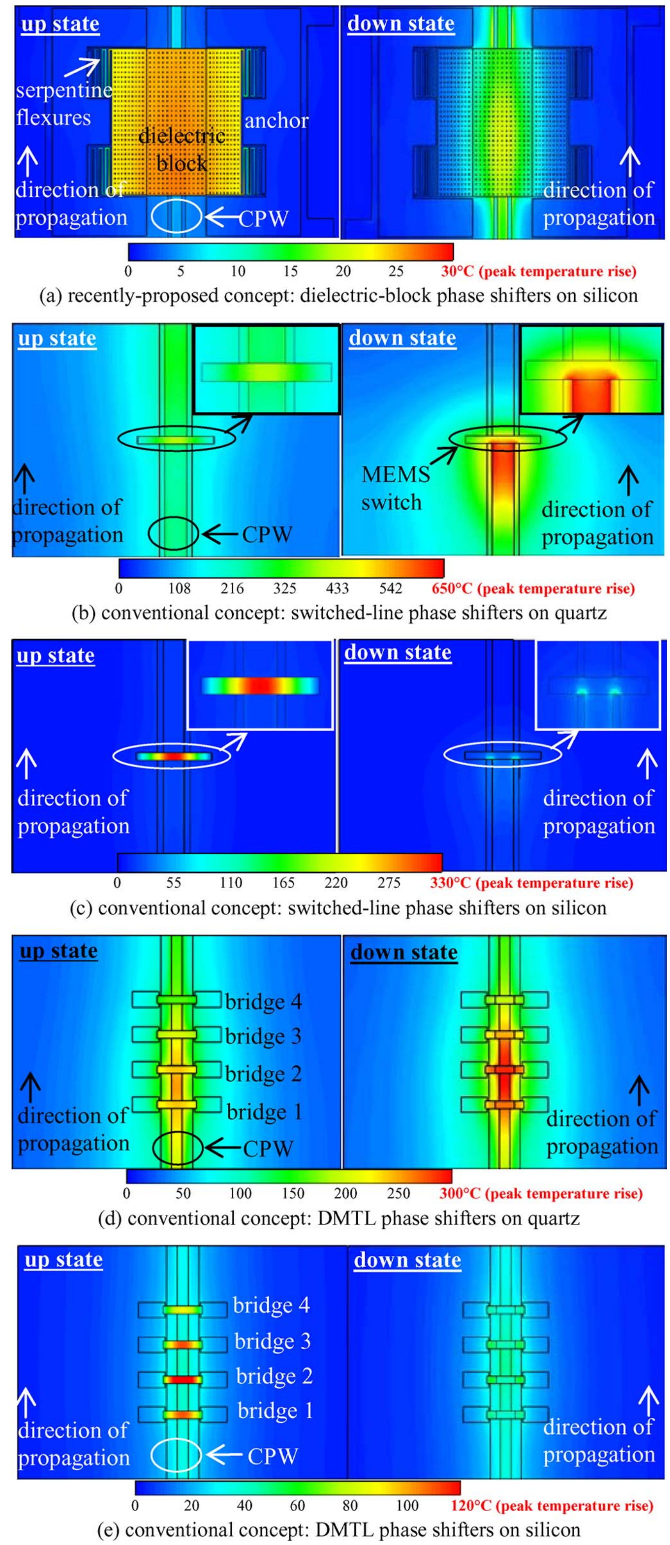

Fig. 11. Simulated temperature rise at 75 GHz and 40 dBm of (a) a 45° single-stage dielectric-block phase shifter on high-resistivity Si substrate, (b) a single switch of switched-line phase shifter on quartz, and (c) on high-resistivity silicon substrate; and (d) a 45° stage of a DMTL phase shifter on quartz and (e) on silicon substrate, respectively. The thermal simulations were done at 75 GHz with 40-dBm (10 W) signal power with the same chip areas for all simulations. Note that the color scales are different for the different subfigures.

and electrothermal simulation models are taken from [7] and [10], respectively, in an effort to reproduce the RF performance of state-of-the-art designs of these conventional MEMS phase-shifter types.

Fig. 12 plots the simulated temperature increase in the hottest spots for the different designs at 75 GHz over signal powers from 20 to 40 dBm (10 W). For the recently reported dielectric-block phase shifter (45° stage), the maximum temperature rise is only 30 °C, whereas the maximum temperature rises for the switched-line and DMTL phase shifters (45°) are as high as 650 °C and 300 °C, respectively, which is by a factor of more than 20 and 10 times more than the novel dielectric-block phase shifter, respectively. Even if a silicon substrate, offering a better heat sink, would be used for the conventional phase shifters, which, however, would drastically degrade their RF performance by 2.5–4 dB in the W-band, the temperature increase would still be 330 °C and 120 °C for the switched-line and DMTL designs, respectively (11 and 4 times more than the novel design, respectively). For the single-pole multi-throw switched-line phase shifter, the thermal robustness of the switches may increase only in the downstate position for the shut-switch design. However, as the numbers of the switches in the single-pole multithrow system increase, the RF losses and the design complication increase.

Furthermore, it is noted that the conventional MEMS phase-shifter concepts are much more susceptible to even small temperature increases, as they are made of soft metals whose mechanical elasticity and, thus, actuation reproducibility and reliability are degrading at increased temperatures. For gold, which is a very common material for fabricating the bridges of the conventional phase shifters, the peak temperatures should be kept below an absolute temperature of 80 °C in order not to degrade the metallic bridges [15]–[17]. Thus, the MEMS switched-line and DMTL designs can be only operated up to 31 and 34 dBm (1.5 and 2.5 W) on quartz substrates or 33.8 and 38.39 dBm (2.4 and 6.9 W) on silicon substrates, which give a much worse RF performance for these phase-shifter types than for the concept recently reported by the authors. For the proposed dielectric-block phase shifter, however, aside from the fact that its peak-temperature rise is only 30 °C even at 40 dBm at 75 GHz, all mechanically active parts are fabricated in monocrystalline silicon, which maintains its mechanical properties well up to 900 °C [32]; therefore, this phase-shifter concept is much better suited for high-power handling than the conventional phase shifters. The thermal power handling of the novel device concept is only limited by the t-line, not by the MEMS part, and by self-actuation, which is calculated

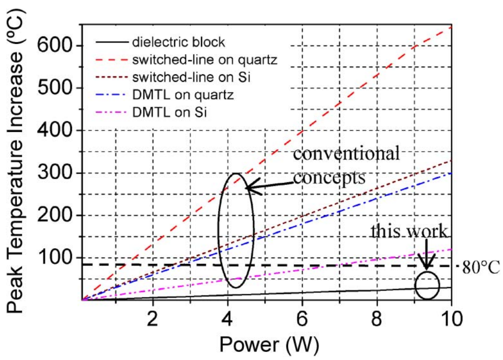

Fig. 12. Simulated peak-temperature rises of the three MEMS phase-shifter concepts at a signal power from 0.1 to10 W (20–40 dBm) at 75 GHz.

TABLE I
COMPARATIVE FIGURE-OF-MERIT PERFORMANCE SUMMARY OF THE THREE MEMS PHASE SHIFTER CONCEPTS

	dielectric block (this work)	DMTL (conventional)	switched-line (conventional)
commonly-used substrates	**Si***	glass/quartz/ (Si**)	glass/quartz/ GaAs/(Si**)
structural material	**Si***	metals (Au)	metals (Au)
substrate thermal conductivity	**very good**	Poor	very poor
dissipated power in moving elements	**extremely low**	very high	extremely high
temperature rise at high signal power	**very low**	very high	extremely high
overall high-power handling capability	**excellent**	very bad at high frequency	extremely bad
peak temperature rise (40 dBm at 75 GHz)	**30**°C	300°C	650°C
power handling at 75 GHz	**> 40 dBm (> 10 W)**	34 dBm (2.5 W)	31 dBm (1.5 W)
limitation of power handling	***t*-line**	metallic bridge***	MEMS switches***
plastic deformation temperature of the MEMS part	**very high**	very low	very low
RF losses for the whole *W*-band	**low**	low/moderate	high
MEMS reliability at high power	**very good**	Moderate	low-moderate
linearity	**very good**	very good	very good
design complexity at high frequency	**low**	Low	moderate

*high-resistivity silicon.
**Si improves thermal behavior, but drastically decreases RF performance
***power handling capability is lower due to plastic deformation of the gold bridges (only around 80°C).

to be 42.52 dBm. Table I summarizes the overall performance comparison of the different concepts.

VI. CONCLUSION

The thermal characteristics and the power handling capability analysis of the all-silicon dielectric-block MEMS phase-shifter concept have been evaluated and compared with two conventional true-time-delay and DMTL phase-shifter concepts, which utilized the air-suspended thin gold membrane. The recently proposed concept has been found to be the first MEMS phase-shifter concept whose thermal power handling capability is not limited by the MEMS structures but only by the transmission line itself and by the heat sink capabilities of the substrate. The peak-temperature rise due to the high signal power at 75 GHz of the novel dielectric-block phase shifter is only 30 °C at 40 dBm, which is 10 and 20 times lower than the conventional MEMS phase-shifter concepts, respectively.

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