Binary-Coded 4.25-bit W-Band Monocrystalline–Silicon MEMS Multistage Dielectric-Block Phase Shifters

Nutapong Somjit, Göran Stemme, *Fellow, IEEE*, and Joachim Oberhammer, *Member, IEEE*

***Abstract*—This paper presents a novel concept of a microwave microelectromechanical systems (MEMS) reconfigurable dielectric-block phase shifter with best loss/bit at the nominal frequency and best maximum return and insertion loss ever reported over the whole W-band. A seven-stage phase shifter is constructed by $\lambda/2$-long high-resistivity silicon dielectric blocks, which can be moved vertically by MEMS electrostatic actuators based on highly reliable monocrystalline silicon flexures on-top of a 3-D micromachined coplanar transmission line. The dielectric constant of each block is artificially tailor made by etching a periodic pattern into the structure. Stages of 15°, 30°, and 45° are optimized for 75 GHz and put into a binary-coded $15^\circ + 30^\circ + 5 \times 45^\circ$ configuration with a total phase shift of 270° in $19 \times 15^\circ$ steps (4.25 bits). Return and insertion losses are better than −17 and −3.5 dB at 75 GHz, corresponding to a loss of −0.82 dB/bit, and a phase shift efficiency of 71.1°/dB and 490.02°/cm. Return and insertion losses are better than −12 and −4 dB for any phase combination up to 110 GHz (98.3°/dB; 715.6°/cm). The intercept point of third order, determined by nonlinearity measurements and intermodulation analysis, is 49.15 dBm for input power modulation from 10 to 40 dBm. The power handling is only limited by the transmission line itself since no current-limiting thin air-suspended metallic bridges as in conventional MEMS phase shifters are utilized. This is confirmed by temperature measurements at 40 dBm at 3 GHz with skin effect adjusted extrapolation to 75 GHz by electrothermal finite-element method simulations.**

***Index Terms*—Microelectromechanical systems (MEMS), microwave, millimeter wave, phase shifter, RF MEMS.**

I. Introduction

MICROWAVE phase shifters are widely employed in many wireless communication and remote sensing systems, including radar sensors based on phased antenna arrays. Conventional electronic phase shifters use GaAs, MESFET, and p-i-n diode switches with high insertion loss, poor nonlinearity performance, and large power consumption. Ferrite-based phase shifters perform well, but large size and high cost prevent the use in commercial applications.

Microelectromechanical systems (MEMS) phase shifters are known for their exceptionally low insertion loss and high linearity over a large bandwidth as compared to solid-state technology [1] and are inexpensive since employing large-volume standard clean-room fabrication processes.

MEMS-switched true-time delay-line (TTD) phase shifters have excellent performance, but are not suitable for millimeter-wave frequencies, including the 75-110-GHz W-band, because the performance of multiple switches and the necessary length of the transmission line degrade the performance [2]–[6]. Distributed MEMS transmission line (DMTL) phase shifters [7]–[12], i.e., periodically capacitive-loaded high-impedance transmission lines using MEMS capacitive bridges, perform well at high frequency, but are, like switches, composed of thin metal bridges that cannot handle large induced current densities at high RF power [13], [14] because of limited heat conductivity to the substrate due to their suspension above the substrate. This results in reliability issues due to buckling (plastic yielding) or even melting of the thin metal layer [15]. Additionally, thin gold bridges, as employed in both types of MEMS phase shifters, are subject to drastically losing their elastic behavior even at slightly elevated temperatures of just around 80 °C, resulting in decreased reliability.

This paper introduces a novel concept of ultra-broadband digital-type multistage binary-coded microwave MEMS phase shifters based on tuning the loading of a 3-D micromachined transmission line by a dielectric block placed on top of the line and moved by MEMS actuators. In a recent conference publication, the authors have shown that such a dielectric block affects the wave propagation in a transmission line [16], and that it can be used as a variable phase shifter by placing stages of equal delay in series [17]. In this paper, the authors present for the first time a multistage programmable phase shifter with binary-coded individual blocks, which is achieved by artificially tuning the effective dielectric constant of the blocks to achieve a tailor-made phase delay in separate stages. Additionally, this paper presents extensive device performance evaluation of the binary-coded phase shifters as compared to linear-coded designs in the whole W-band, and presents nonlinearity/intermodulation analysis, as well as an error analysis of the multiple-stage phase shifters. The mechanical reliability of the devices was investigated with lifetime measurement in the nonhermetic environment.

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The authors are with the Microsystem Technology Laboratory, School of Electrical Engineering, KTH–Royal Institute of Technology, Stockholm SE-100 44, Sweden (e-mail: nutapong.somjit@ee.kth.se; goran.stemme@ee.kth.se; joachim.oberhammer@ee.kth.se).

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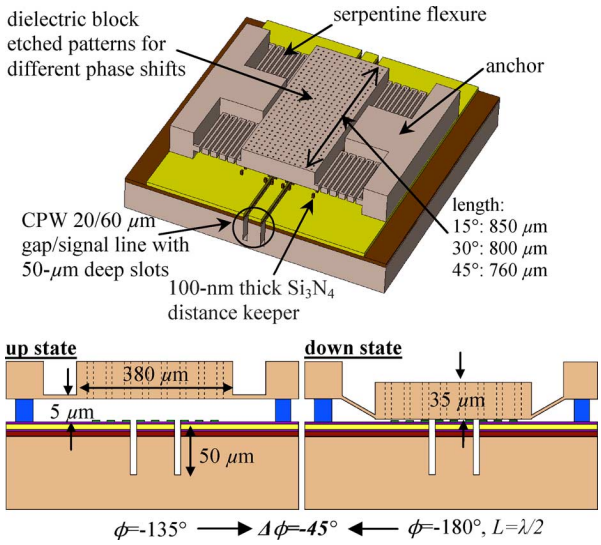


Fig. 1. Working principle of a single stage of the phase shifters [16].

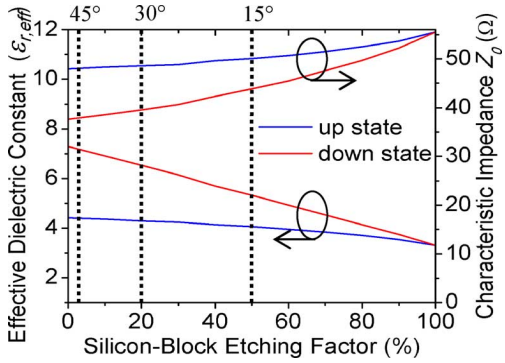


Fig. 2. Effective dielectric constant and the characteristic impedance of the transmission line loaded by the dielectric block, depending on the etch hole size. The etching factors are 3.4% for the 45°, 20% for the 30°, and 50% for the 15° phase-shifter stage.

II. Concept and Design

A single stage of the dielectric-block MEMS phase shifter consists of a high-resistivity monocrystalline silicon block placed upon and loading a 3-D high-impedance ($>$ 50 Ω) micromachined coplanar waveguide (CPW). The relative phase shift ($\Delta\phi$) is achieved by vertically moving the dielectric block above the t-line by electrostatic actuation, which results in different propagation constants of the microwave signal depending on the vertical displacement of the dielectric block (Fig. 1). The additional deep-etched slots of 50 μm into the high-resistivity silicon substrate decrease substrate loss and increase the sensitivity of the propagation speed to changes in the displacement of the dielectric block. The length of the dielectric blocks is chosen to be $\lambda/2$ at the nominal frequency of 75 GHz to minimize the RF signal reflection from both edges of the dielectric block. For digital-type operation, an optimum operation point of high phase-shift sensitivity with displacements realizable with MEMS electrostatic actuators was chosen to a displacement between up and down state positions of 5 μm.

All mechanically moving parts of this phase-shifter concept are fabricated out of a single monocrystalline silicon block. Monocrystalline silicon is the best available mechanical material in microsystems due to its strength and the highly elastic properties, which ensure creep free actuation, and because it is inherently free from stress gradients that would cause warping of the moving parts. This is an inherent reliability advantage as compared to all conventional MEMS phase-shifter concepts based on metallic bridges, which are subject to stress-related warping and plastic deformation limiting their life time, especially at slightly elevated operation temperatures.

Periodic patterns are etched into the dielectric block, and the ratio of the etched area to the unetched area, i.e., the pulsewidth modulation of the etch pattern, allows for artificially tuning the macroscopically effective dielectric constant of each individual block. Fig. 2 shows the effective dielectric constant and the characteristic impedance of the transmission line loaded by the dielectric block, depending on the etch hole size. Three different embodiments are used as building blocks for the binary-coded multistage phase shifters presented in this paper with a relative phase shift of 45°, 30°, and 15° for the design frequency of 75 GHz.

The multistage phase-shifter designs presented in this paper comprise binary coded $15^\circ + 30^\circ + 5 \times 45^\circ$ phase shifters with a total phase shift of 270° in 15° steps, i.e., 19 different phase states corresponding to a resolution of more than 4 bits, which are compared to linear-coded $7 \times 45^\circ$ phase shifters with a total phase shift of 360° in 45° steps, i.e., eight different phase states (3 bits). The main design and measured performance data of these types is shown and compared in Fig. 3.

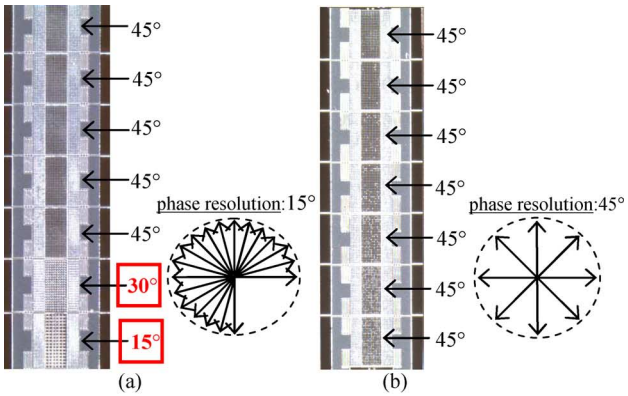
III. Fabrication

The 1-μm-thick sputtered-gold CPW is fabricated on a high-resistivity silicon substrate ($>$ 4000 Ω·cm). 100-nm thick Si_3N_4 bumps are deposited on the metal layer as distance keepers to prevent stiction and dc short circuiting of the pulled-in block. The slots of the CPW are etched 50 μm into the substrate by deep reactive ion etching (DRIE). A high-resistivity silicon-on-insulator (SOI) wafer is transfer bonded to this wafer by adhesive polymer bonding with mr-I 9250xp thermal nanoimprint lithography photoresist [18], and the SOI handle wafer is afterwards removed by plasma etching. Its 35-μm-thick device layer is patterned by two DRIE steps to shape the thick dielectric block, the release-etch holes of varying sizes to determine the tailor-made dielectric properties and the 9-μm-thick serpentine flexures. The structures are released by O_2 plasma etching of the bonding layer. Fig. 4 shows a top-view scanning electron microscope (SEM) photograph of a binary-coded three-stage phase-shifter embodiment comprising a 15°, 30°, and 45° stage (75 GHz).

IV. Characterization and Analysis

A. S-Parameters Characterization and Performance Comparison to Previous Work

Fig. 5 shows the measured insertion and return loss of the binary-coded $15^\circ + 30^\circ + 5 \times 45^\circ$ phase shifter for one to



	binary-coded 15°+30°+5x45°	*linear coded 7x45°*
design data		
stage numbers	7	7
phase-shift combinations	8	19
max. $\Delta\phi$ at 75 GHz (°)	270	315
phase resolution at 75 GHz (°)	15	45
single stage length (μm)		
- 45° stage	760	760
- 30° stage	800	-
- 15° stage	850	-
total length (mm)	5.51	5.4
measured key performance		
max. IL 75-110 GHz (dB)	-4	-5.1
max. RL 75-110 GHz (dB)	-12	-12
$\Delta\phi$/loss at 75 GHz (°/dB)	71.05	74.1
$\Delta\phi$/length at 75 GHz (°/cm)	490.02	592.1
$\Delta\phi$/loss at 110 GHz (°/dB)	98.3	97.1
$\Delta\phi$/length at 110 GHz (°/cm)	715.6	916.7

Fig. 3. Microscope pictures and key performance data of fabricated seven-stage phase shifters consisted of $15° + 30° + 5 \times 45°$ (*left*) and $7 \times 45°$ (*right*) phase shifters. (a) Binary-coded $15° + 30° + 5 \times 45°$. (b) Linear-coded $7 \times 45°$.

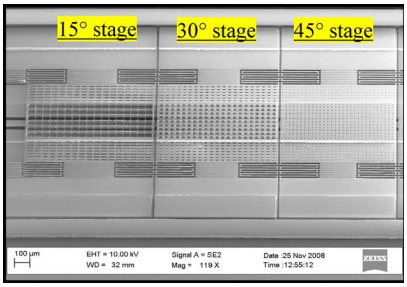


Fig. 4. SEM photograph of fabricated phase shifter blocks within seven-stage phase shifter: 15° (*left*), 30° (*middle*), and 45° (*right*).

all seven stages actuated. At the design frequency of 75 GHz, maximum return and insertion loss are -17 and -3.5 dB, respectively, which is corresponding to a loss of -0.82 dB/bit, and a phase shift efficiency of 71.1°/dB and 490.02°/cm. The phase shifter behaves exceptionally broadband over the whole W-band with the maximum return loss better than -12 dB and the maximum insertion loss of less than -4 dB (98.3°/dB; 715.6°/cm at 110 GHz). Fig. 6 plots the phase-shifter efficiency (phase shift/length and phase shift/loss) for the frequency range from 75 to 110 GHz. Table I compares the novel phase shifter designs to HEMT, MEMS switched delay line, and DMTL phase shifters [9], [19]–[22]. The binary coded MEMS phase shifter presented in this paper has better insertion loss per bit

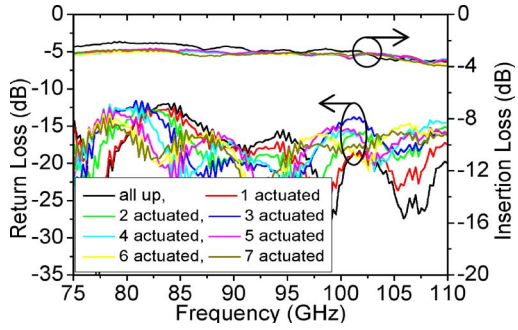


Fig. 5. Measured return and insertion losses of the binary-coded $15° + 30° + 5 \times 45°$ phase shifter.

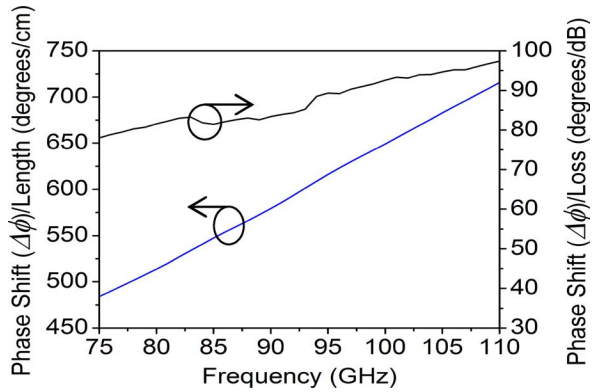


Fig. 6. Figure-of-merit performance of the $15° + 30° + 5 \times 45°$ phase shifter: measured phase shift per length and phase shift per loss for the frequency range from 75 to 110 GHz.

and better maximum return loss than any phase shifter previously reported, both for their respective nominal frequency and for the whole W-band. Designs [9] and [21], 3-bit, and 1-bit phase shifters, respectively, have better phase shift per loss at their nominal frequencies, but perform worse than the presented 4.25-bit phase shifter over the rest of the W-band. This performance data, already of the first prototype designs, demonstrates the advantage of the new MEMS phase-shifter concept over other MEMS and GaAs-switch phase shifters despite the fact that the present technology is utilizing silicon both as a substrate and for the dielectric block, in contrast to the other high-performance phase shifters fabricated on low-loss glass or GaAs substrates.

B. Phase-Shift and Phase-Error Measurements

The phase-shift performance, including phase shift per loss and phase shift per length, along with other design and measured performance parameters, is summarized in Fig. 3. Fig. 7 shows the phase-shift analysis of the binary-coded $15°+30°+5\times45°$ phase shifter measured from 1 to 110 GHz. Fig. 7(a) shows the very linear relative phase shift over the whole spectrum for all 19 possible phase states. The absolute phase error for all states is shown in Fig. 7(b). The absolute error is increasing with frequency since the phase shift increases with frequency as well. To compensate for that, Fig. 7(c) shows the relative phase error, calculated by the absolute phase error for all combinations, divided by the maximum phase shift (all stages down) at the respective frequencies. For frequencies above

TABLE I
COMPARISON FOR SEVERAL W-BAND PHASE SHIFTERS

reference	[19]	[9]	[20]	[21]	[22]	*This work*	
						binary coded	***linear coded***
substrate	GaAs	glass	Si	quartz	quartz	Si	Si
nominal frequency f_n (GHz)	94	78	76.5	90	80	75	75
number of bits	4	3	3	1	2	4.25	3
config. possibilities	16	8	8	2	4	19	8
max. $\Delta\phi$ of f_n (°)	337.5	315	315	180	282	270	315
max. IL of f_n (dB)	>-8	>-3.2	>-5.8	>-2.5	>-6.1	>-3.5	>-4.5
max. IL/bit of f_n (dB/bit)	-2	-1.07	-1.93	-2.5	-3.05	-0.82	-1.5
max. $\Delta\phi$/loss of f_n (°/dB)	56.25	95.75	55.26	85.71	70.5	71.05	74.1
max. $\Delta\phi$/loss[a] (°/dB)	-	83.3	-	32.85	-	98.3	97.1
max. RL of f_n (dB)	<-15	<-12	<-12	<-12	<-9.5	<-17	<-12
max. IL at W (dB)	>-10	>-6	>-8	>-6	>-7	>-4.1	>-5.1
max. RL at W (dB)	<-8	<-9	<-7.5	<-3	<-9	<-12	<-12

at W: over the whole W-band 75-110 GHz. [a] at 110 GHz

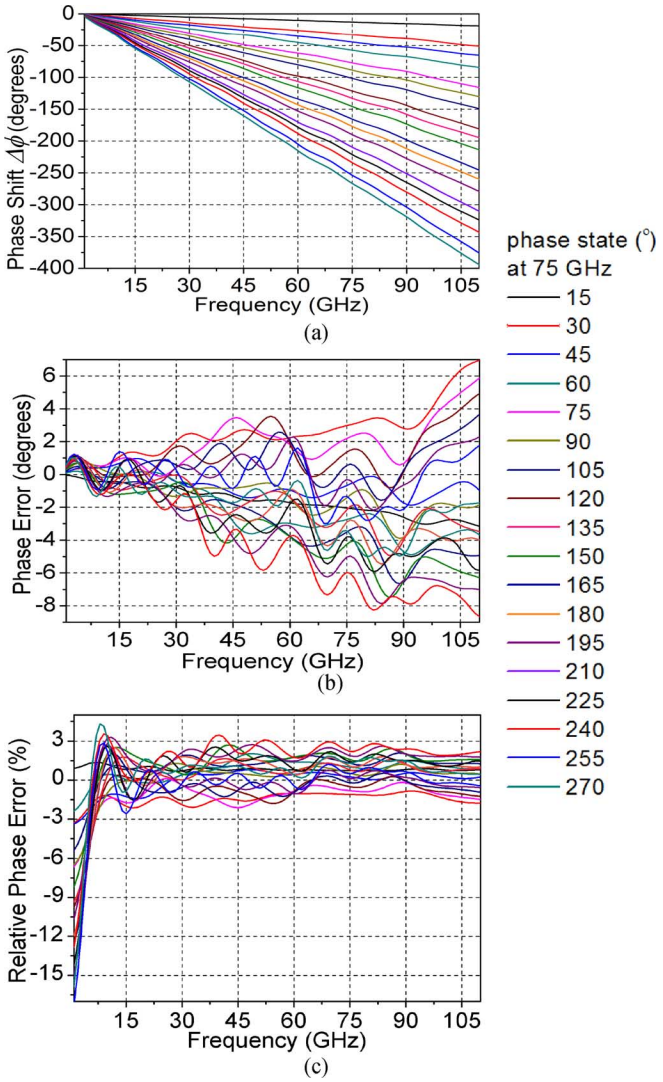


Fig. 7. (a) Measured phase shift for all states of binary-coded 15°+30°+5×45° phase shifter. (b) Absolute phase error. (c) Frequency-normalized phase error: phase error of all states relative to the maximum phase shift at the given frequency.

10 GHz, all combinations have a relative phase error of less than 3%. Table II lists the nominal and measured phase shifts for all combinations including the absolute and relative phase errors for the nominal frequency of 75 GHz. Here, the relative phase error is calculated by the absolute phase error of a state in relation to the phase shift of the specific state. The absolute value of the phase deviation from its nominal value has an average of 2.61° and a standard deviation of 1.58° for all possible combinations, and the maximum deviation is 6° (for the combination resulting in 240°).

C. Nonlinearity Analysis: Response to Power Modulation

Despite the mechanical resonance frequencies of the device being a magnitude of at least 10^4 lower than electrical signals in the gigahertz range, the effective value of the signal line voltage creates force acting on the moveable parts in any RF MEMS device. Thus, even though the component is passive and inherently linear since a single-tone input signal also results in a single-tone output signal, variations in the voltage (power) level of the electrical signal result in variations of the up-state position of the dielectric block, causing a nonlinear phase modulation. This phenomenon occurs for every MEMS phase shifter, and the degree of the nonlinearity depends on the stiffness of the mechanical suspension of the moving parts [23]–[27].

TABLE II
MEASURED PHASE SHIFT AND PHASE ERROR AT 75 GHz
($\Delta\phi_d$ = Nominal Design Phase Shift; $\Delta\phi_m$ = Measured Phase Shift)

$\Delta\phi_d$ (°)	15	30	45	60	75	90
$\Delta\phi_m$ (°)	12.95	32.98	44.33	57.25	77.19	88.58
err. (°)	-2.05	2.98	-0.67	-2.75	2.19	-1.42
err. (%)	-13.67	9.93	-1.49	-4.58	2.92	-1.58
$\Delta\phi_d$ (°)	105	120	135	150	165	180
$\Delta\phi_m$ (°)	101.4	121.3	132.85	145.7	165.5	177.1
err. (°)	-3.6	1.3	-2.15	-4.3	0.5	-2.9
err. (%)	-3.34	1.13	-1.59	-2.87	0.34	-1.61
$\Delta\phi_d$ (°)	195	210	225	240	255	270
$\Delta\phi_m$ (°)	189.9	209.6	221.2	234	253.6	266.56
err. (°)	-5.1	-0.4	-3.8	-6	-1.4	-3.44
err. (%)	-2.58	-0.16	-1.68	-2.5	-0.52	-1.27

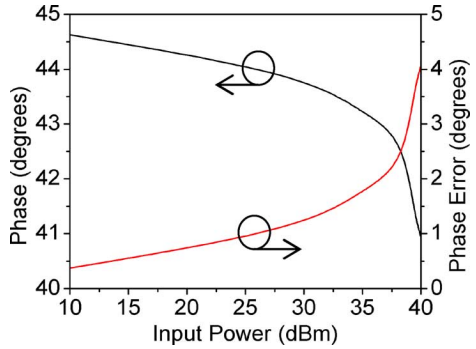


Fig. 8. Measured phase shift depending on input RF power.

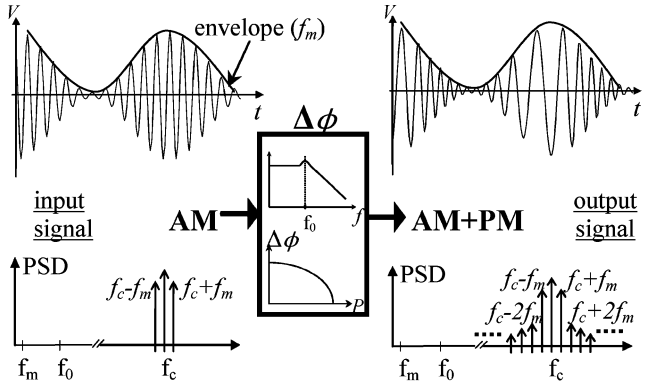
The phase shift in S_{21} depending on the input power level was measured for the presented devices by involving a power amplifier, filters for filtering the nonlinearities of the amplifier, two 50-Ω high-power impedances and two circulators at the ports to protect the signal generator and the power amplifier from the reflected mismatched power. Fig. 8 shows the measured deviation in the phase shift of a 45° single stage plotted over the input power level, measured at 3 GHz and up to 40 dBm (the phase shift is extrapolated to the nominal frequency of 75 GHz).

The simulated mechanical resonant frequency is 63.1 kHz and the acceleration sensitivity is $0.0056° \cdot s^2 \cdot m^{-1}$ for the 45° phase shifter block at 75 GHz in the up-state position. The down state is even less sensitive to the external acceleration because the block is electrostatically clamped, which drastically increases its effective spring constant.

Thus, a power modulation (amplitude modulation) with a modulation frequency f_m of the RF signal f_c will result in an additional phase modulation with the frequency f_m, as displayed in Fig. 9 for a single 45° stage, if the frequency f_m of the amplitude modulation is below the mechanical resonance frequency f_0 of the device, which is in the order of a few tens of kilohertz. The output power spectrum will, therefore, include phase-modulation sidebands at $f_c \pm n \bullet f_m$ beside the amplitude modulation sidebands, as shown in this figure for different power modulation parameters. For a power modulation from 10 to 20 dBm, the sidebands created by the phase modulation are below −11.71 dBc, and for a power modulation from 10 to 40 dBm, these sidebands rise to −6.57 dBc.

D. Intermodulation Products, Dual-Tone Test

Similar to the phase modulation resulting from an amplitude modulation of a single-tone signal as discussed in Section IV-D, a dual-tone, unmodulated signal may cause phase modulation if the $\Delta f = f_1 - f_2$ is smaller than the mechanical cutoff frequency f_m of the device. This is caused by the envelope of the total power of the two steady-state signals being modulated with Δf, and thus resulting in a phase modulation as discussed in Section IV-D for the up-state position of the device. The nonlinearity characteristics 45° stage can be calculated from the capacitance modulation derived by measurements (Fig. 8) and by using the models introduced in [23]–[27]. The third intermodulation level and intercept point of third order (IIP3) with different RF input power of the transmitted signal are plotted in Fig. 10(a), showing an IIP3 of 49.27–47.97 dBm for total input power levels of 10–30 dBm. With larger mechanical stiffness of the structure, the nonlinearity decreases, as shown in Fig. 10(b) with the additional parameter of the block distance from the transmission line in the up-state position. The effective spring constant of 36.67 N/m and initial gap of 5 μm of the presented design are a good compromise between an acceptable low actuation voltage of 30 V, which is characterized by white-light interferometric profilometer, and good RF performance in terms of nonlinearity and phase shift per unit length.



input signal modulation (dBm)	carrier and modulating signal frequency		spectral components (single-sideband power spectral density: SSB PSD)			
	f_c (GHz)	f_m (kHz)	f_c+2f_m (dBc)	f_c+3f_m (dBc)	f_c+4f_m (dBc)	f_c+5f_m (dBc)
10-12 dBm	75	10	-84.1	-149.3	-218.1	-265.7
10-20 dBm	75	10	-61.4	-117.1	-176.4	-238.1
10-30 dBm	75	10	-50.1	-98.5	-150.4	-204.7
10-40 dBm	75	10	-42.4	-84.2	-129.4	-177.2

(b)

Fig. 9. Responses of a single 45° stage to a power modulated signal. (a) Schematic illustration of phase modulation caused by a power modulated signal if the modulation frequency f_m is smaller than the mechanical cutoff frequency f_0. (b) Spectral components of the input and output signals, calculated from the measured power dependent phase shift (Fig. 8) for modulating power as listed in the table.

E. Thermal Behavior and MEMS Reliability

Conventional MEMS phase shifters, both true-time delay lines and DMTL phase shifters, are based on thin moveable metal bridges, either capacitive switches or varactors. Such bridges are the power-limiting bottleneck of these phase shifters, since the thermal conductivity of thin suspended metal bridges to the substrate heat sink is relatively small, which limits the current handling of the bridges and thus the whole phase shifter [13]–[15].

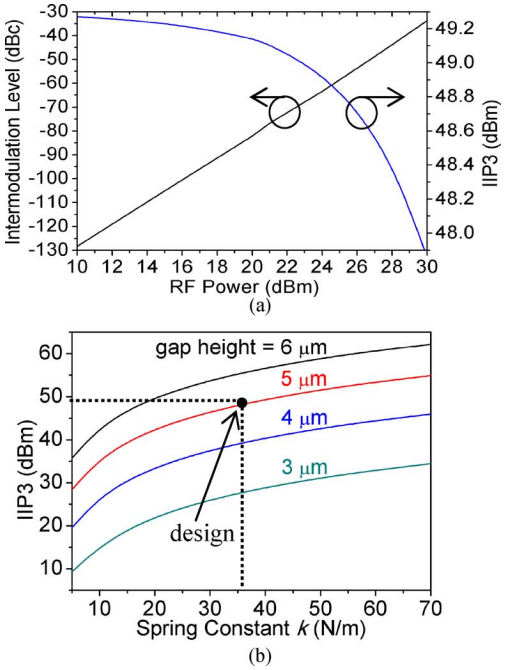


Fig. 10. Nonlinearity characteristic of a single 45° stage phase shifter with two-tone signal at 75 GHz + 10 kHz (Δf). (a) Third IM level and IIP3 with different RF input power. (b) IIP3 for different initial distances of the block for varied mechanical spring constant (for 40 dBm total signal power).

For the presented phase shifter, no metal bridges are used at all, which means that the power handling is only limited by the power handling of the transmission line as such [28], which is directly fabricated on the substrate heat sink. Temperature measurements at 40 dBm and 3 GHz were done with infrared cameras, and the measurement data was extrapolated to 75 GHz by comparing thermal-electrical simulations at 3 and 75 GHz, taking the skin depth into account, resulting in a temperature increase of the hottest spot on the CPW of only 30 °C at a power level of 40 dBm and a frequency of 75 GHz.

The mechanical reliability of the devices was characterized by lifetime measurements with a unipolar rectangular-pulse actuation voltage of 10 kHz. Three samples were evaluated and all of them passed one billion actuation cycles, even the test was carried out in the nonhermetic environment, after which the tests were stopped without observing any failure.

V. Conclusion

A novel ultra-broadband digital-type multiple-stage binary-coded microwave MEMS phase shifter concept with best loss/bit at the nominal frequency and best maximum return- and insertion-loss performance over the whole W-band applications is introduced. The relative phase shift is controlled by vertically moving a dielectric, monocrystalline silicon block above the 3-D micromachined CPW. Periodically etched patterns in the dielectric block with three different sizes are introduced for artificially tuning the effective dielectric constant resulting in relative phase shift of 45°, 30°, and 15° for single stages at 75 GHz. The measurements show a maximum return loss better than −17 dB with a maximum insertion loss less than −3.5 dB for 75 GHz, and −12 and −4 dB at 110 GHz, respectively, of a seven-stage binary-coded phase shifter with total phase shift of 270° in 15° steps. The binary-coded phase shifter also has an excellent loss of −0.82 dB/bit, while the linear-coded phase shifter has −1.5 dB/bit. The binary-coded phase shifter performs with 71.05°/dB and 490.02°/cm at 75 GHz, and 98.3°/dB and 715.6°/cm at 110 GHz,, whereas the linear coded phase shifter performs 74.1°/dB and 592.1°/cm at 75 GHz, and 97.1°/dB and 916.7°/cm at 110 GHz. The nonlinearities were characterized to an IIP3 of 49.27 dBm at 10-dBm total power.

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Nutapong Somjit was born in Bangkok, Thailand, in 1978. He received the Dipl.-Ing. (M.Sc.) degree in electrical engineering from the Dresden University of Technology, Dresden, Germany, in 2005, and is currently working toward the Ph.D. degree at the KTH–Royal Institute of Technology, Stockholm, Sweden.

Following his diploma study, he was with the Computational Electromagnetics Laboratory (TEMF), Darmstadt University of Technology, Darmstadt, Germany, where he developed RF components for the Superconducting Darmstadt Linear Accelerator (S-DALINAC). In 2006, he joined the Microsystem Technology Laboratory, KTH–Royal Institute of Technology. His main research is focused on RF MEMS including MEMS fabrication and packaging.

Mr. Somjit is an Associate Member of the European Network of Excellence on RF MEMS and RF Microsystems (AMICOM) Forum. He was the recipient of the Best Paper Award (EuMIC Prize) presented at European Microwave Week 2009, Rome, Italy.

Göran Stemme (M'98–SM'04–F'06) was born in Stockholm, Sweden, in 1958. He received the M.Sc. degree in electrical engineering and Ph.D. degree in solid-state electronics from the Chalmers University of Technology, Göteborg, Sweden, in 1981 and 1987, respectively.

In 1981, he joined the Department of Solid State Electronics, Chalmers University of Technology, where, in 1990, he became an Associate Professor (docent) heading the Silicon Sensor Research Group. In 1991, he became a Professor with the Royal Institute of Technology, Stockholm, Sweden, where he heads the Microsystem Technology Group, School of Electrical Engineering.

Dr. Stemme is a member of the Royal Swedish Academy of Sciences (KVA). He has been a member of the Editorial Board of the IEEE/ASME JOURNAL OF MICROELECTROMECHNICAL SYSTEMS since 1997. From 1995 to 2001, he was a member of the International Steering Committee of the Conference series IEEE MEMS, and was general co-chair of that conference in 1998. He was corecipient (with two colleagues) of the final of the 2001 Innovation Cup in Sweden. He has authored or coauthored over 260 research journal and conference papers. He holds over 22 patents proposals or patents pending.

Joachim Oberhammer (M'06), was born in Brunico, Italy, in 1976. He received the M.Sc. degree in electrical engineering from the Graz University of Technology, Graz, Austria, in 2000, and the Ph.D. degree from the Royal Institute of Technology in Stockholm, Sweden, in 2004. His doctoral research concerned RF MEMS switches and microsystem packaging

He was involved with automotive sensor electronics and RF identification (RFID) systems with the Graz University of Technology and Vienna University of Technology, Vienna, Austria, prior to joining the Microsystem Technology Laboratory, KTH–Royal Institute of Technology. Following a period as a Post-Doctoral Research Fellow with Nanyang Technological University, Singapore, he returned to the Royal Institute of Technology in 2005, as an Assistant Professor heading a research team with activities in RF MEMS. In 2007, he became an Associate Professor with the Royal Institute of Technology. In 2007 and 2008, he was a Guest Researcher with both Nanyang Technological University and Kyoto University, Kyoto, Japan, respectively. He has authored or coauthored over 40 reviewed research papers. He holds three patents.

Dr. Oberhammer has been a Steering Group member of the IEEE Microwave Theory and Techniques Society (MTT)/Antennas and Progation (AP) Swedish Chapter since 2009.