



**Workflow &
Solver Overview**

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Chapter 1 — Introduction

Welcome

Welcome to CST PCB STUDIO, the powerful and easy-to-use program for the analysis of electromagnetic characteristics of complex PCBs.

CST PCB STUDIO is embedded into the CST STUDIO SUITE which is referred to in the *CST STUDIO SUITE Getting Started* manual. The following explanations assume that you have already installed the software and familiarized yourself with the basic concepts of the user interface.

How to Get Started Quickly

We recommend that you proceed as follows:

- Read the *CST STUDIO SUITE Getting Started* manual.
- Work through this document carefully. It should provide you with the information necessary to understand the advanced documentation found in the online help.
- Please look at the ‘Examples’ folder in the installation directory. Different applications will give you a good idea of what can be accomplished. Please note that these examples are designed to give you a basic insight into a particular application domain.
- After working through this booklet, use your own example. Choose a reasonably simple example that will allow you to quickly become familiar with the software.

What is CST PCB STUDIO?

CST PCB STUDIO is an electromagnetic simulation tool specially designed for the fast and accurate simulation of real-world PCBs and can be used for pre-layout and post layout analysis. It allows the simulation of effects like resonances, reflections or crosstalk on any kind of PCBs from single-layer up to multilayered high-speed PCBs.

CST PCB STUDIO easily integrates into any existing design flow by importing PCB designs directly from many popular EDA layout tools and provides a powerful tool for the automated layout checking and correction of geometric errors.

CST PCB STUDIO has an intuitive user interface that makes it easy to define a design from scratch for pre-layout analyses. There are advanced functions to navigate through a design and to select, hide or visualize any objects like traces or areas.

CST PCB STUDIO incorporates three different solver techniques to account for all kinds of PCBs. Single- or two layer PCBs are normally designed without any special ground reference layers and therefore dedicated to the lower- or medium frequency range. The method best suited to this kind of application is the quasi-static Partial Element Equivalent Circuit method (PEEC). The program generates equivalent circuits out of any selected combination of conductors. Skin effect and dielectric loss are modeled in both the frequency and the time domain.

CST PCB STUDIO offers a 2D transmission line modeling technique to analyze classical signal integrity issues on high-speed multilayer boards like time delay, reflection and crosstalk on multiple transmission lines. The program automatically performs the partitioning and decides on adequate segments where the transmission line parameters should be calculated.

CST PCB STUDIO uses CST DESIGN STUDIO to define passive and active devices on the modeled PCB layout with the help of an easy-to-use schematic editor. The powerful built-in network simulator inside CST DESIGN STUDIO enables the simulation of the whole system consisting of the equivalent circuit of the PCB and its termination in both frequency and time domain. Broadband equivalent circuits can be exported in several SPICE formats for a further usage in other commercial network simulators.

CST PCB STUDIO offers a modeling technique dedicated to the analysis of power distribution networks (PDN) in multi-layer PCBs. Given a set of PDN nets to be characterized, the full-wave three-dimensional Finite Element Frequency Domain solver, hereafter referred to as 3D (FE FD), is able to compute PDN impedances directly. The results can be used to check whether the design margins imposed by the IC component are met. Using the CST PCB STUDIO component library, this modeling option enables the assessment of different decoupling capacitor strategies, taking into account the full-wave electromagnetic effects in the PDN.

Applications

- SI-analysis on single/multilayer PCBs
- PI-analysis on single/ multilayer PCBs

CST PCB STUDIO Key Features

An overview of the main features of CST PCB STUDIO is provided in the following list. Please note that not all options may be available to you due to license restrictions. Please contact your local sales office for details.

For the circuit simulator only some selected key features are listed below. A full list can be found in the *CST DESIGN STUDIO Workflow* manual.

General

- Native graphical user interface based on Windows operation systems.
- Tight interface to CST DESIGN STUDIO.
- PEEC method specializing in the simulation of single- and two-layer boards.
- Transmission line modeling method for SI analysis of high-speed multi-layer PCBs.
- Specialized FEM method for PI analysis of high-speed multi-layer PCBs.

PCB Structure Modeling

- Import of PCB designs from Cadence Allegro/ADP/SiP.
- Import of PCB designs from Mentor Graphics Expedition.
- Import of PCB designs from Mentor Graphics Hyperlynx.
- Import of PCB designs from Mentor Graphics PADS.
- Import of PCB designs from Zuken C-R5000/8000 ASCII.
- Import of PCB designs from ODB++.
- PCB layout checker with automatic correction.
- Interactive PCB editing tools.
- Advanced navigation through the PCB.
- Hiding/visibility selections.

PCB Electric Modeling

- Automatic meshing and extraction of 3D PEEC models.
- Automatic meshing and extraction of 2D transmission line models.
- Automatic meshing and extraction of 3D (FE FD) models and PDN impedances.
- Consideration of skin-effect and dielectric loss in time and frequency domain.
- Export of equivalent SPICE circuits.
- Export of current distribution and near fields for radiation analysis.
- Advanced Export of PCB sub structures to CST MICROWAVE STUDIO.

Circuit Simulator

- Schematic editor enables the easy definition of passive and active devices.
- Fast circuit simulation in time and frequency domain.
- Import of SPICE sub circuits (Berkley Spice and HSpice syntax).
- Support of IBIS models.
- Import and Export of S-Parameter data via TOUCHSTONE file format.
- Parameterization of termination circuitry and parameter sweep.

About This Manual

This manual is primarily designed to enable a quick start to the modeling capabilities of CST PCB STUDIO. It is not intended as a reference guide of all available features, but rather as an overview of the key concepts. Understanding these concepts will allow you to learn the software efficiently with help from the online documentation.

To learn more about the circuit simulator please refer to the *CST DESIGN STUDIO Workflow* manual.

The next chapter *Overview* is dedicated to explaining the principal concepts behind CST PCB STUDIO and to show the most important objects and related dialog boxes. The chapter *Examples* will guide you through the three important analysis types. We strongly recommend studying both chapters carefully.

Document Conventions

- Buttons that should be pressed within dialog boxes are always written in italics, e.g. *OK*.
- Key combinations are always joined with a plus (+) sign. *Ctrl+S* means that you should hold down the “Ctrl” key while pressing the “S” key.
- The program’s features can be accessed through a Ribbon command bar at the top of the main window. The commands are organized in a series of tabs within the Ribbon. In this document a command is printed as follows: *Tab name: Group name ⇨ Button Name ⇨ Command name*. This means that you should activate the proper tab first and then press the button *Command name*, which belongs to the group *Group name*. If a keyboard shortcut exists it is shown in brackets after the command. Example: *View: Visibility ⇨ Wire Frame (Ctrl+W)*
- The project data is accessible through the navigation tree on the left side of the application’s main window. An item of the navigation tree is referenced in the following way: *NT: Tree folder ⇨ Sub folder ⇨ Tree item*. Example: *NT: 1D Results ⇨ Port Signals ⇨ i1*

Your Feedback

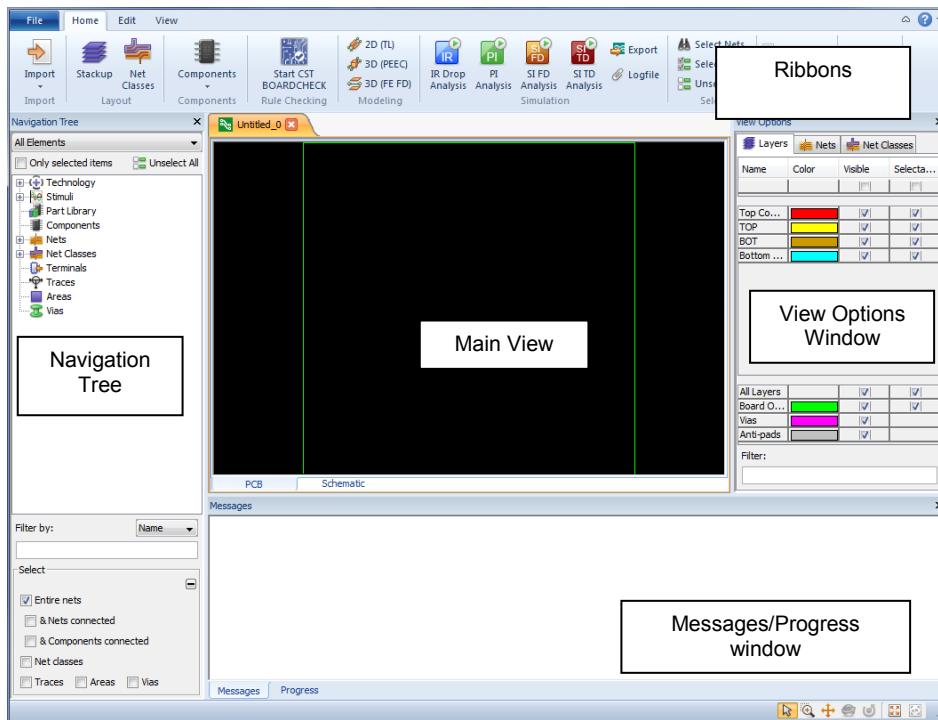
We are constantly striving to improve the quality of our software documentation. If you have any comments regarding the documentation, please send them to info@cst.com.

Chapter 2 — Overview

CST PCB STUDIO is designed to be easy to use. However, to get started quickly you will need to know your way around the interface and have knowledge of the basic features and concepts. The main purpose of this chapter is to provide an overview of the general interface.

User Interface

Launch CST STUDIO SUITE from the Start menu or by clicking on the desktop icon. In the *Modules* list double click on *CST PCB STUDIO*. A new CST PCB STUDIO project is opened with an empty *Main View*.



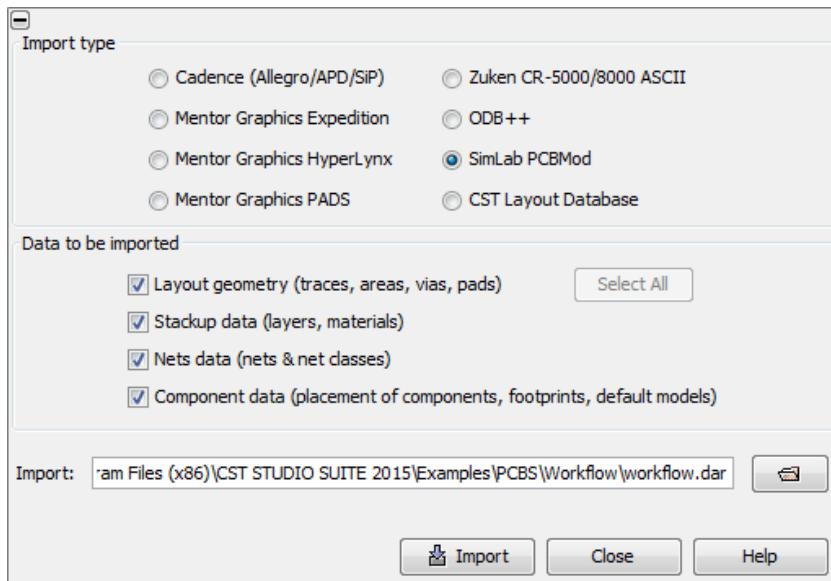
The user interface is divided into five sub-windows:

- The **Main View** shows the 2D visualization of the PCB design.
- The **View Options** window allows the setting of specific visualization and selection properties for many objects.
- The **Navigation Tree** allows access to all objects of the project. It is organized into folders and subfolders with specific contents. When selecting an item it will be highlighted in the *Main View*. It also includes a powerful tool for a more convenient selection of different objects. It makes it possible to track logical net list relations in a physical geometry due to its hierarchical tree structure and due to the connection with the *Main View*.

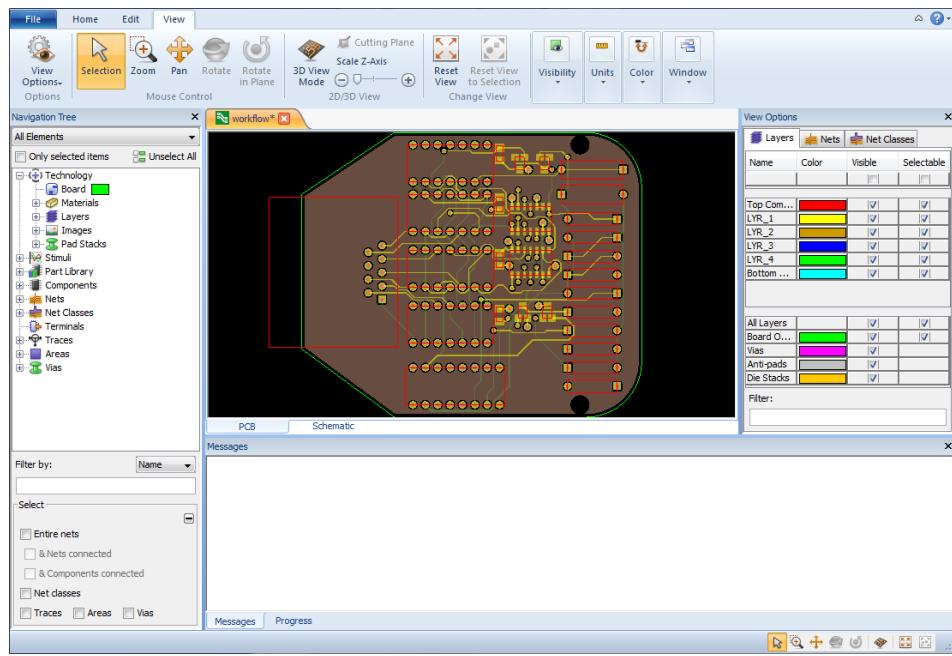
- The **Messages** window shows general information, solver progress, warnings and errors during project set-up or simulation.

Importing a PCB

In order to import an existing PCB layout into an empty PCBS project, press *Home: Import*. The following dialog will appear where you set the *Import type* to *Simlab PCBMod*. Use the file browser to navigate to the folder *Examples* of your CST STUDIO SUITE installation directory and select the file *workflow.dar* under the subfolder *PCBS/Workflow*:



Next press *Import*. After a few seconds the PCB design will appear in the *Main View* as shown in the next figure. There will be a warning in the message window which can be ignored in our case.



We have now imported our first PCB design. Save the project as ‘**workflow**’.

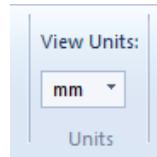
Exploring the PCB

This section will explain the most important tools for exploring a PCB. The *Main View* window includes a powerful 2D layout viewer that allows a fast investigation even for very complex PCBs. The three main modes to manipulate the view on the layout are *Selection*, *Zoom* and *Pan*. They control the behavior of the mouse for the viewer and can be called via *View: Mouse Control* as shown in the figure below:

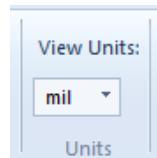


There are two different 2D-layout viewers available: the default viewer and the legacy viewer. The default viewer is based on a fast rendering engine, which is suitable for viewing complex boards.

An important characteristic of the board is its overall size. When importing an existing board, the corresponding units will be set automatically and displayed in *Home: Units* ↪ *View Units*:

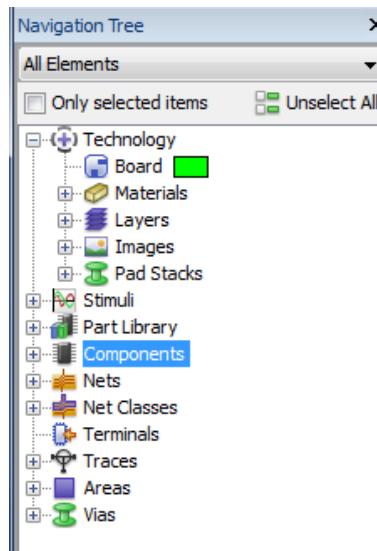


The view unit can be changed by selecting any unit which is available in the drop down menu. The change of the view unit will not change the size of any structure on the PCB. The structure size stays the same. The PCB will only be displayed in the new chosen unit. We will change the view unit to *mil* as shown in the figure below and continue our exploration.

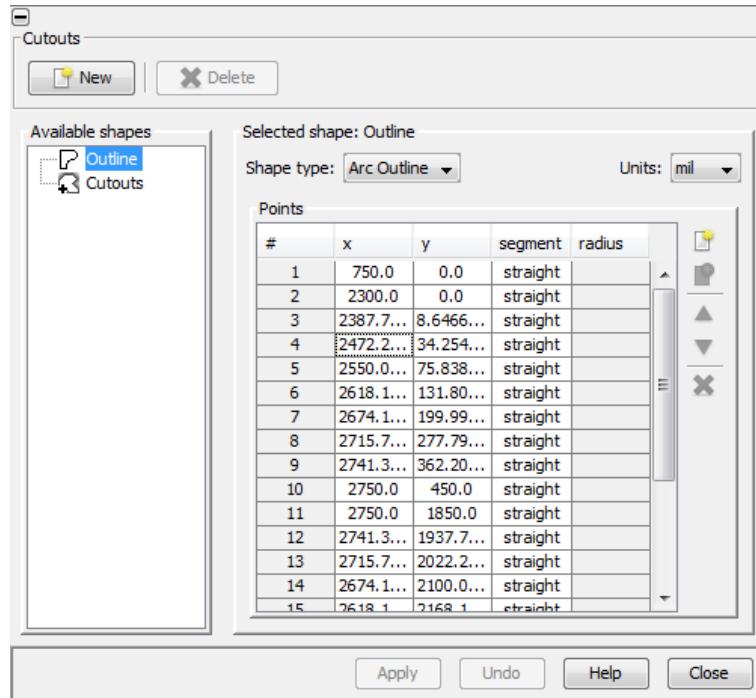


Note: changing the unit size is possible with many other dialog boxes inside CST PCB STUDIO.

The best way to get an overview of the available objects and functions is with the help of the *Navigation Tree*. After expanding the folders *Technology* we have the following view:



First we inspect the objects inside *Technology*. When selecting the object *Board*, the displayed PCB in the *Main View* will change. *Board* defines the outline of the PCB and this outline could be edited by choosing *Edit Outline* with the right mouse button or double click with the left mouse. After clicking on *Edit Outline*, the following dialog box will appear where we see the polygon defining the outline:

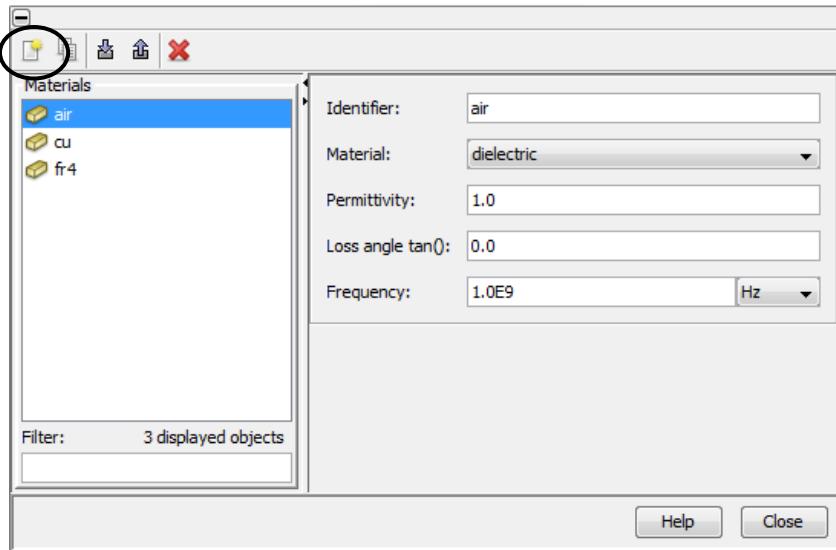


We can change its form either by changing the coordinates from the table or by dragging the point interactively using the mouse in the *Main View*. But we will close the dialog box without changing anything.

There are three existing material types that can be seen when expanding the *Materials* folder:

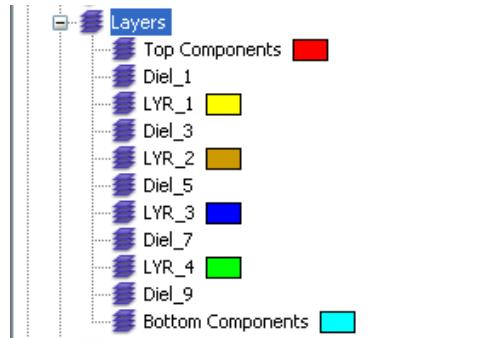


After choosing *Edit* by using the right mouse button the following dialog box will appear:



We are able to edit the existing materials or to create new materials by pressing the marked symbol. We close the dialog box without applying any changes.

After expanding the *Layers* folder, a list appears defining the layer stack-up:



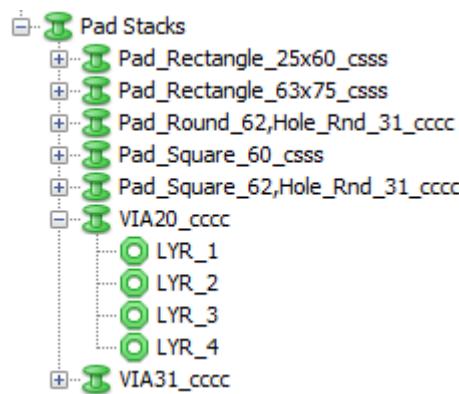
We see four metallic layers (*LYR_1*, *LYR_2*, *LYR_3*, *LYR_4*) and the corresponding dielectric layers in between. The editing of such a layer stack-up will be explained in sub-chapter *Stack up Manager*.

After expanding the *Images* folder, a list of items will appear as shown in the figure below:

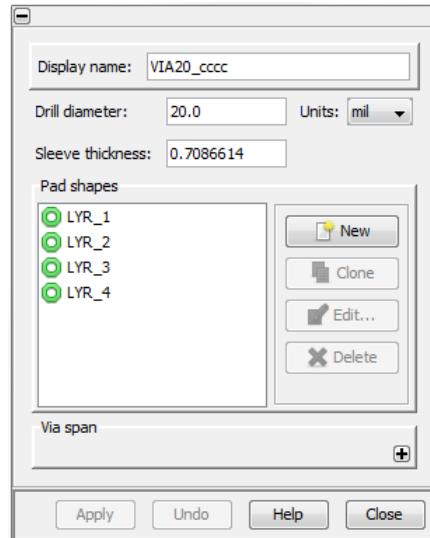


These items are supporting objects which can't be edited. The items are automatically generated during the EDA-import of an existing PCB design. They define the graphical appearance of the components on the top and bottom layer.

Expanding the *Pad Stacks* folder opens up a list of items which defines the different pad stacks. If you select *VIA20* and expand the object you will see a list of four items defining a stack of pads in all four metallic layers:

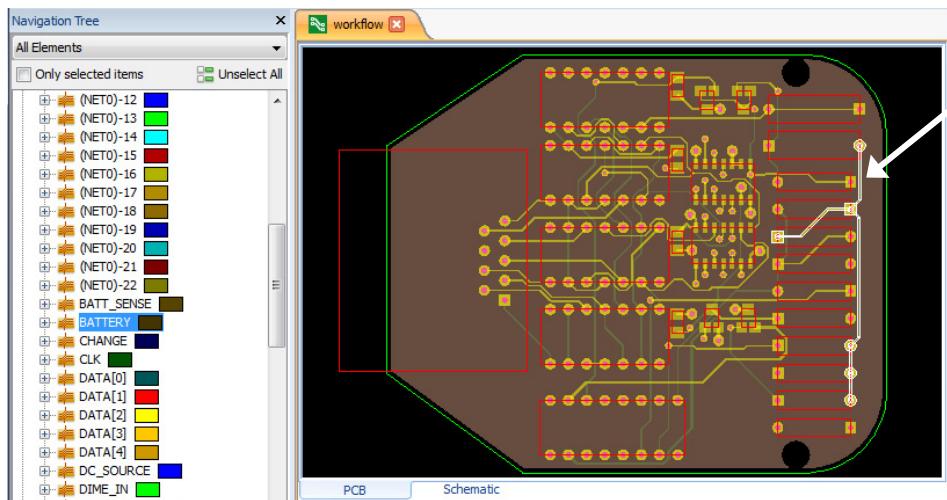


Choosing *Edit* by using the right mouse button will open up the following dialog box:

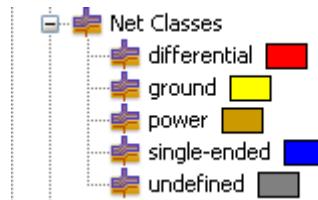


We recognize the list of pads shown in the *Navigation Tree*. Each pad could be edited by selecting the corresponding item and pressing *Edit*. It is assumed that the pads in the different layers are connected by a conductive tube. The diameter of the tube can be defined by *Drill diameter* and its thickness by *Sleeve thickness*. Similar to the *Images* item, the *Pad Stacks* are not for a direct manipulation in the project. They serve as support-objects and are referenced by the objects *vias*.

Next we open the *Nets* folder. A *Net* is a group of conductive shapes that are electrically connected. If you scroll down the *Navigation Tree* and select the *Battery* item, the corresponding net is displayed in the *Main View* as can be seen in the figure below:



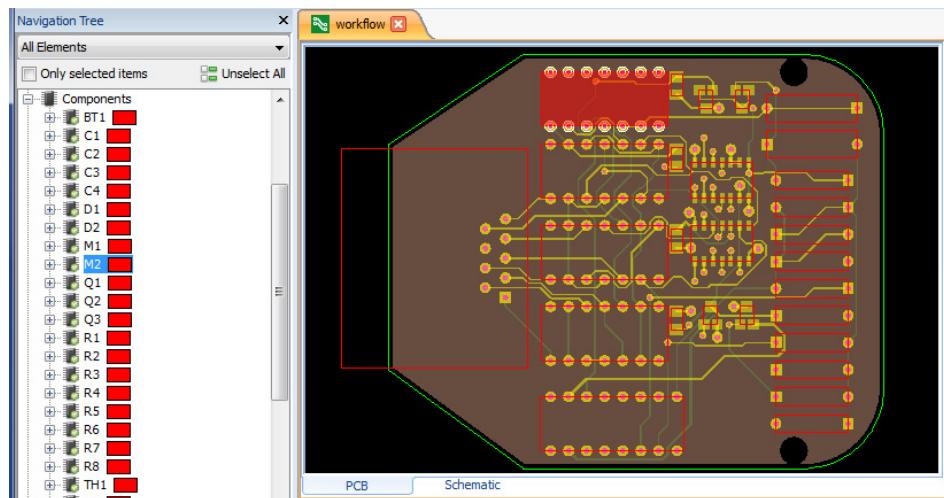
Now we select the *Net Classes* object and expand it. A list will appear showing the five different net classes sorted in alphabetic order:



Net class *differential* and net class *single-ended* are both nets meant to transport signals. Net class *differential* is a special class type necessary to identify a pair of different nets that are (more or less) symmetrically aligned along their path through the PCB and they establish a complete transmission line. A net from type *single-ended* needs another net serving as path for the return current. Normally a net from the *ground* net class is used to complete the transmission line.

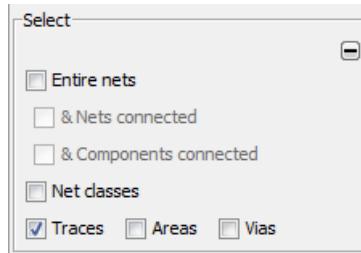
The *power* net class is used to identify all nets that do not transport *signals* but supply *power* for the active devices. Nets of the *ground* net class serve as return current path for all other nets. All nets that are not classified belong to the *undefined* net class. During the import the program tries to assign the different nets to their corresponding net classes by means of the net's names (e.g. net *GND* will automatically be assigned to net class *ground*).

Next we expand the *Components* object. While selecting different items in the list we see the corresponding components highlighted in the *Main View*. Scrolling down the *Navigation Tree* and selecting *M2* will highlight the upper rectangle with a red frame and a white crosshair as shown in the figure below:

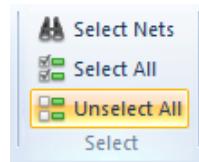


The next folder is called *Terminals*. A terminal is a geometric point that can be placed on conductors. In a further modeling phase terminals are interpreted as spots for measuring voltages or drawing currents. The creation and use of terminals will be explained in more depth in the chapter examples.

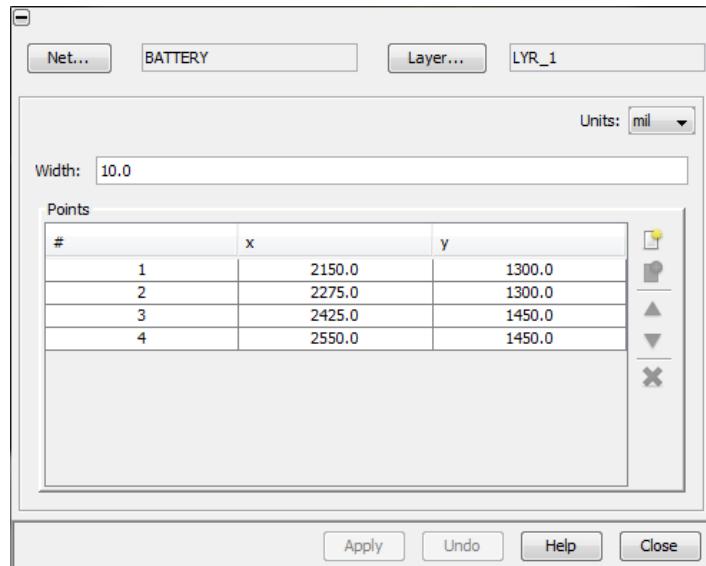
The next three folders *Traces*, *Areas* and *Vias* include all geometric objects a net can contain. First we expand the *Select* frame at the bottom of the *Navigation Tree* and check *Traces* instead of *Entire nets*. This allows the selection of exactly one single trace instead of all traces that belong to a certain net:



In order to remove all selections done so far we press *Home: Select* \Rightarrow *Unselect All*:

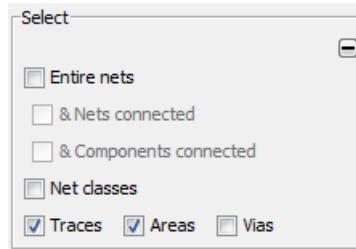


Next we expand the *Traces* folder, scroll down the *Navigation Tree* and select *trace_14*. You will see the corresponding trace highlighted in the *Main View*. Choosing *Edit* by clicking the right mouse button the following dialog box will appear showing the definition of the trace:

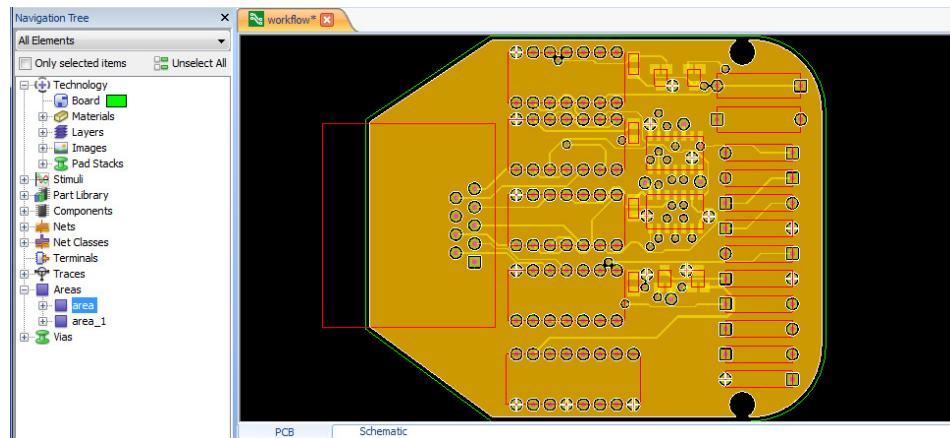


The trace belongs to the *Battery* net, it is placed on Layer *LYR_1* and its width is 10 mil. The path of the trace is defined by the list of points.

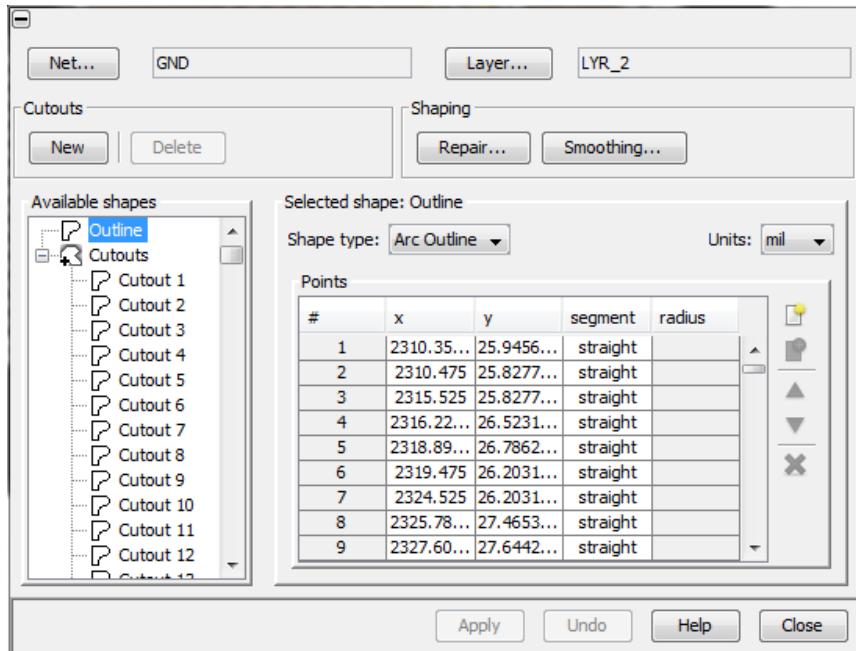
Next we remove the selection by pressing *Unselect All* again, change to the *Select* frame and check *Areas* as shown in the figure below:



Next we deselect *View: View Options* \Rightarrow *Legacy Viewer*. Then we expand the folder *Areas* and select the first item *Area*. The corresponding area is highlighted in the *Main View* as can be seen in the figure below:



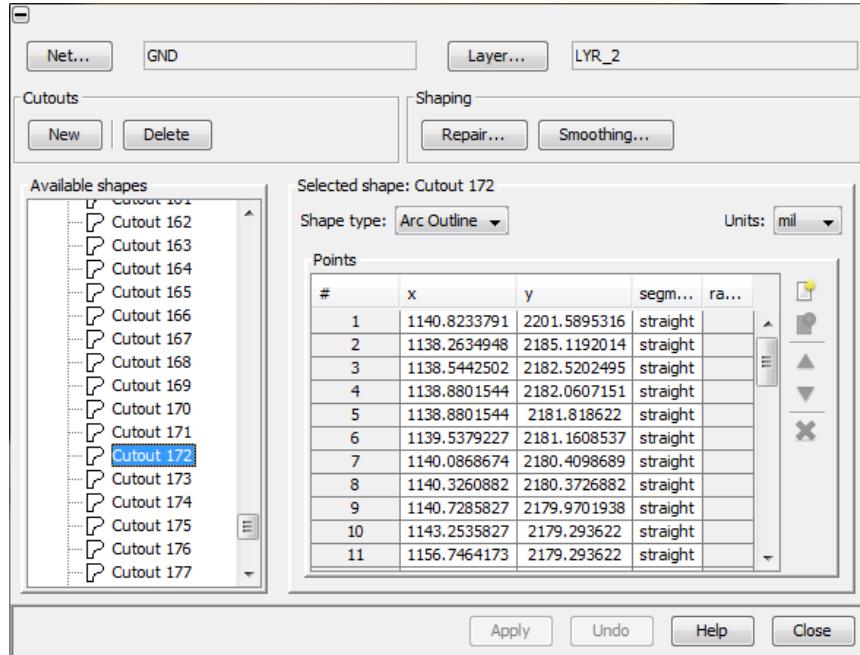
We right mouse click and choose *Edit*. The following dialog box will appear showing the definition of the area:



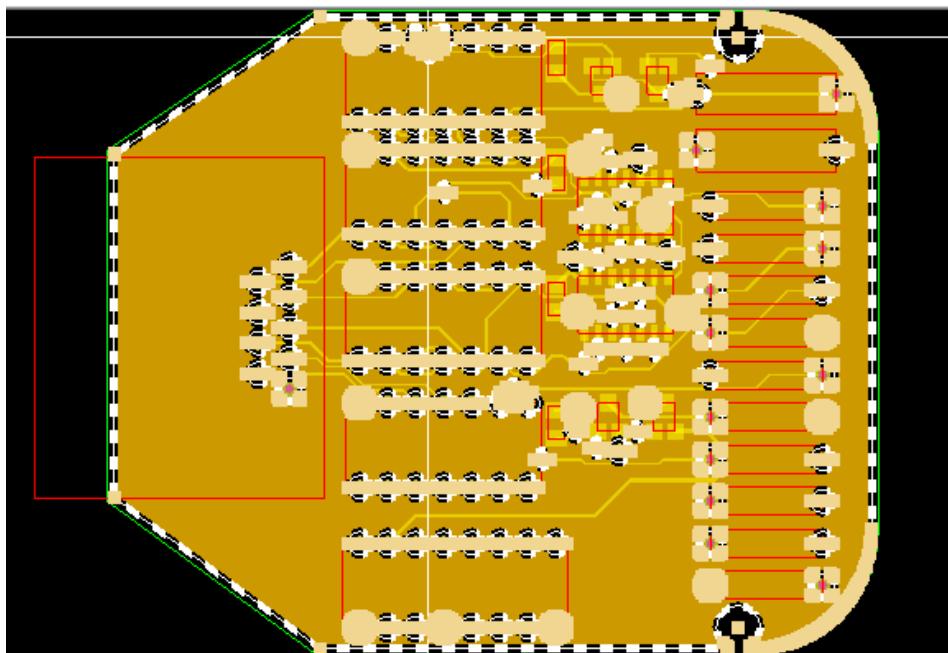
The area belongs to the *GND* net and is located on Layer *LYR_2*. An area consists of exactly one outline shape and it optionally also contains an additional number of cutout shapes.

All shapes are listed in the frame *Available Shapes* on the left side of the dialog box. If you select an item in this list the highlighted lines of all shapes change in the *Main View* and the definition of the selected shape will appear in the table on the right side of the dialog box. Besides the general *Arc Outline* (which supports a special description for round corners) a *Polygon*, a *Rectangle* and a *Circle* shape type are also available and can be used for a quick creation of an area by hand.

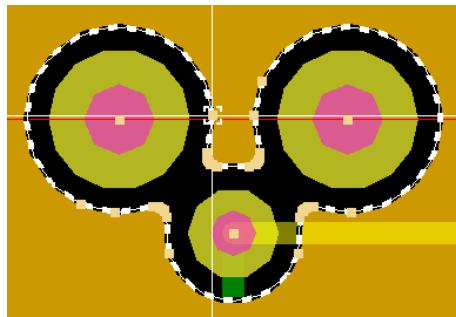
In order to investigate the object more deeply we go into *Cutouts* to see the list of all cutouts:



After selecting the item *Cutout 172*, we see a crosshair in the *Main View* showing the location of the cutout:



To have a closer look we zoom into the location of the cutout. For zooming select *View: Mouse Control* \Rightarrow *Zoom*. The mouse cursor changes to a magnifying glass and allows zooming into the location of the selected cutout. The magnified spot can be seen in the figure below:

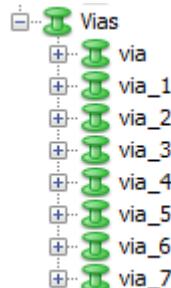


Now we switch back into the *selection mode* in order to return to the default behavior of the mouse cursor (by selecting *View: Mouse Control* \Rightarrow *Selection*).

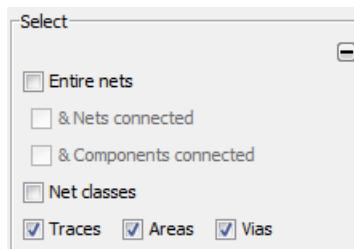
After that we change back to the dialog box, select the first point in the arc outline definition, and start clicking through all other points by using either the left mouse button or the up and down arrows on your keyboard. We will see the synchronized movement of the crosshair in the *Main View*.

Every shape can be edited by either changing the values in the table or by selecting and dragging a certain point with the mouse inside the *Main View*. We will now close the dialog box without changing any values and reset the *Main View* by selecting *View: Change View* \Rightarrow *Reset View*. There will be a more-in-depth explanation on the editing possibilities in sub-chapter *Editing and Checking the PCB*.

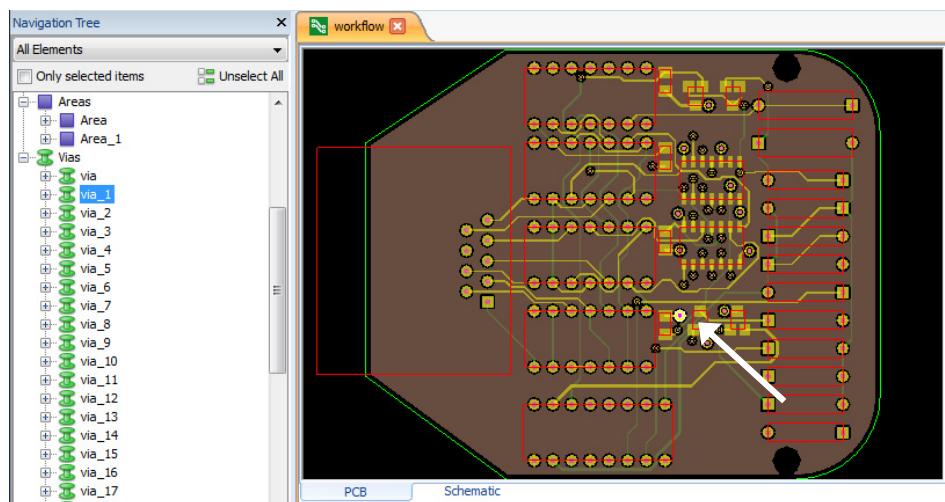
As the last object of the *Navigation Tree* we select and expand the object *Vias*:



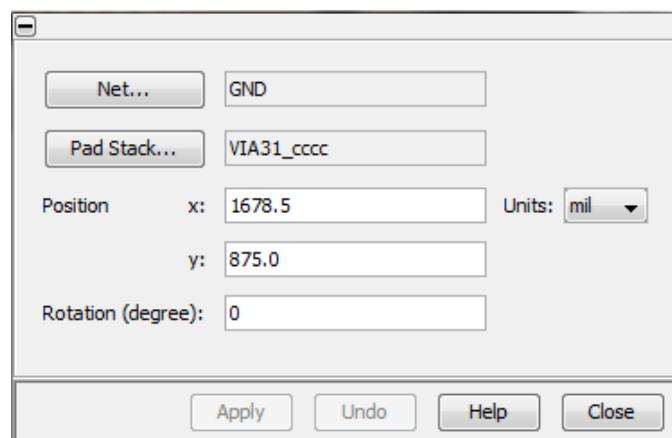
First we unselect all selected objects by using *Home: Select* \Rightarrow *Unselect All* and check *Vias* inside the *Select* frame as shown in the figure below:



Now we move down the list of vias, select *via_1* and see it highlighted in the *Main View*:



We choose *Edit* by clicking the right mouse button and see the following dialog box:

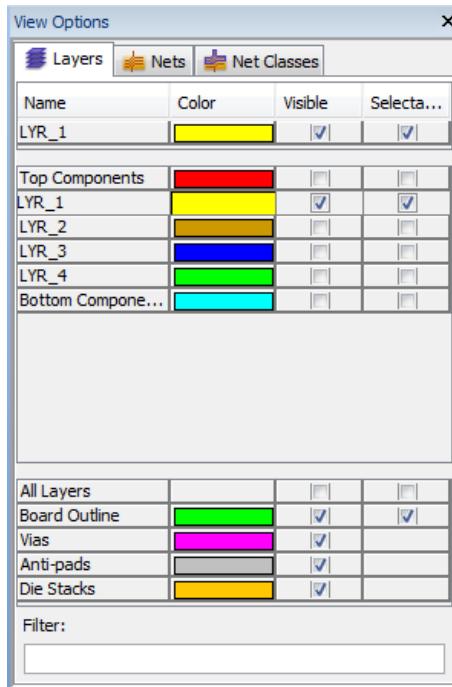


The via belongs to the *GND* net and refers to the pad stack *VIA31_cccc*. The position is defined in two separate fields.

We now have completed the presentation of all important objects of CST PCB STUDIO and in the next step we are going to explain the most important supporting tools.

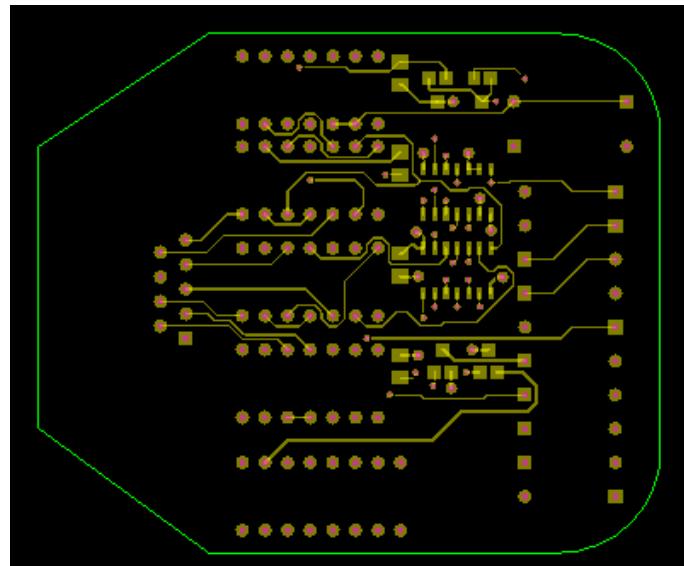
View Options window and Color Modes

A central tool for manipulating the view on the PCB is the *View Options* window as shown in the figure below:



The dialog box consists of three different tabs where important view characteristics of the objects *Layers*, *Nets* and *Net Classes* can be edited. The default tab is *Layers*. All tabs are organized in the same kind of table. The columns define the view characteristics *Color*, *Visible* and *Selectable*. The rows are filled with the corresponding items of the objects *Layers*, *Nets* and *Net Classes*.

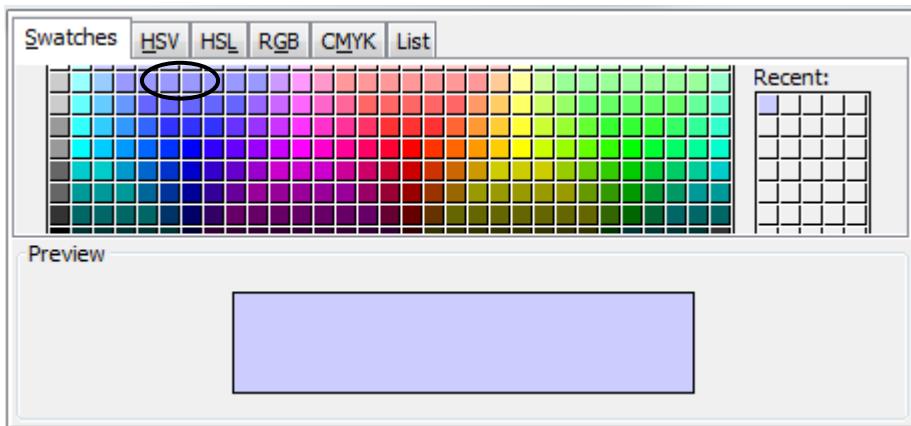
Let's first investigate the behavior by selecting the *Top Components* item in the first column on the left side. After doing this only the top side of the board with its components is displayed. Stepping downwards with the cursor you will notice that only the selected layer with its corresponding structures will be displayed. In the figure below you see the layer *LYR_1*:



We can get back the display of all layers by selecting cell *All Layers* in the last row:

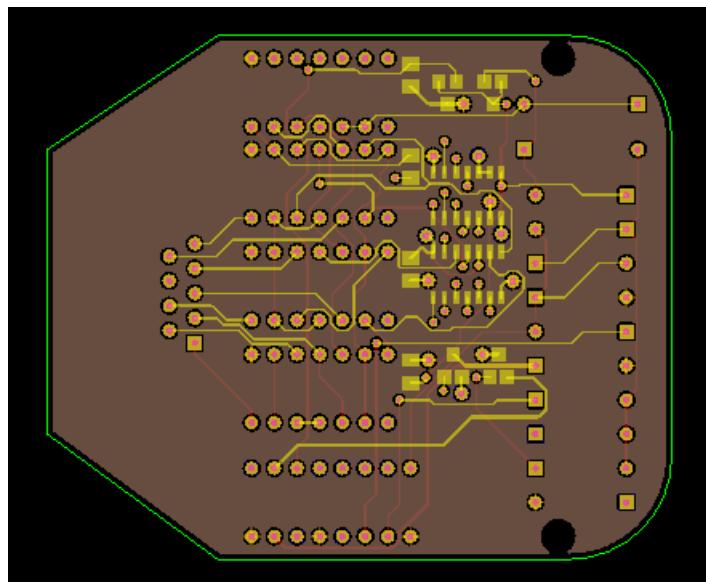
Top Components		<input checked="" type="checkbox"/>	<input type="checkbox"/>
LYR_1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LYR_2		<input checked="" type="checkbox"/>	<input type="checkbox"/>
LYR_3		<input checked="" type="checkbox"/>	<input type="checkbox"/>
LYR_4		<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bottom Compone...		<input checked="" type="checkbox"/>	<input type="checkbox"/>
All Layers		<input checked="" type="checkbox"/>	<input type="checkbox"/>
Board Outline		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Vias		<input checked="" type="checkbox"/>	
Anti-pads		<input checked="" type="checkbox"/>	
Die Stacks		<input checked="" type="checkbox"/>	

Next we investigate the different view characteristics. Therefore we select *Top Components* again and double-click on the red cell in column *Color*. A dialog box appears where you can choose another color.



We select for example a light blue-grey color, press *Ok* and see the new color for all components in the *Main View*.

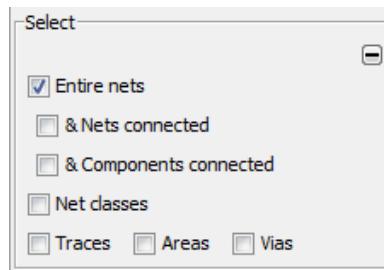
If we uncheck the cell in column *Visible*, we will notice that all components will disappear in the *Main View* as shown in the figure below:



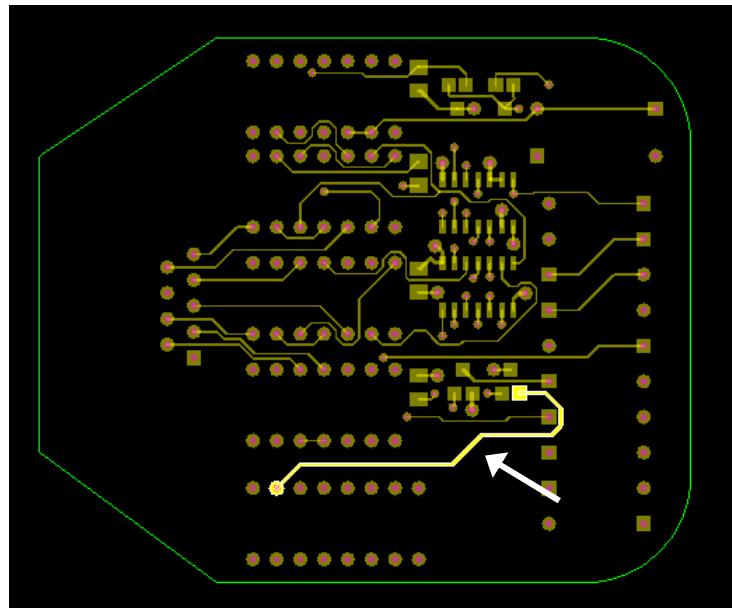
In order to investigate the meaning of the column labeled *Selectable*, we first check *Visible* again and then select layer *LYR_1* as shown in the figure below:

View Options			
Layers	Nets	Net Classes	
Name	Color	Visible	Selectable
LYR_1	Yellow	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Top Components			
LYR_1	Yellow	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LYR_2	Orange	<input type="checkbox"/>	<input type="checkbox"/>
LYR_3	Blue	<input type="checkbox"/>	<input type="checkbox"/>
LYR_4	Green	<input type="checkbox"/>	<input type="checkbox"/>
Bottom Components	Cyan	<input type="checkbox"/>	<input type="checkbox"/>

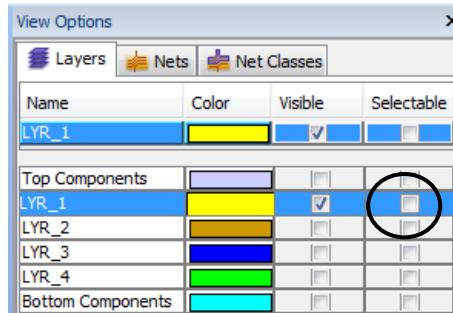
Next we check *Entire nets* in the *Select* frame as shown below:



Inside the *Main View* we now double-click at net *DISCHARGE_MODE* as shown in the figure below:



Next we uncheck the cells in column *Selectable* as shown in the figure below and try to select another component.



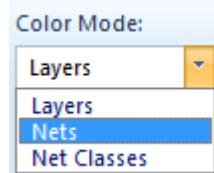
The screenshot shows the 'View Options' dialog box with three tabs: 'Layers', 'Nets' (selected), and 'Net Classes'. Under the 'Nets' tab, there is a table with columns: Name, Color, Visible, and Selectable. A row for 'LYR_1' has its 'Selectable' checkbox checked. Below this, under 'Top Components', there are four rows: 'LYR_1' (checkbox checked), 'LYR_2' (checkbox checked), 'LYR_3' (checkbox checked), and 'LYR_4' (checkbox checked). A red circle highlights the 'Selectable' checkbox for 'LYR_1' in the 'Top Components' section.

Name	Color	Visible	Selectable
LYR_1	Yellow	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LYR_1	Yellow	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LYR_2	Orange	<input type="checkbox"/>	<input type="checkbox"/>
LYR_3	Blue	<input type="checkbox"/>	<input type="checkbox"/>
LYR_4	Green	<input type="checkbox"/>	<input type="checkbox"/>
Bottom Components	Cyan	<input type="checkbox"/>	<input type="checkbox"/>

With the selectable box unchecked it will not be possible to select this net by mouse click on the main view. This function is very useful when selecting an object in a layer which is covered by objects in other layers. In this case the other layers can be set to *not selectable* and afterwards we are able to select the object in a convenient way. You are encouraged to try the behavior of the settings for tab *Nets* and tab *Net Classes* by yourself.

The function **Color Mode** corresponds to the functions provided in the *View Options* window. With the help of *Color Mode* we can decide whether different colors are assigned to distinguish between different layers, between different nets or between different net classes.

The default color mode is *Layer* and this means all objects inside a layer have a special but identical color. In order to switch into the color mode *Nets* (or *Net Classes*), we select *View: Color* \Rightarrow *Color Mode* \Rightarrow *Nets* as shown in the figure below:

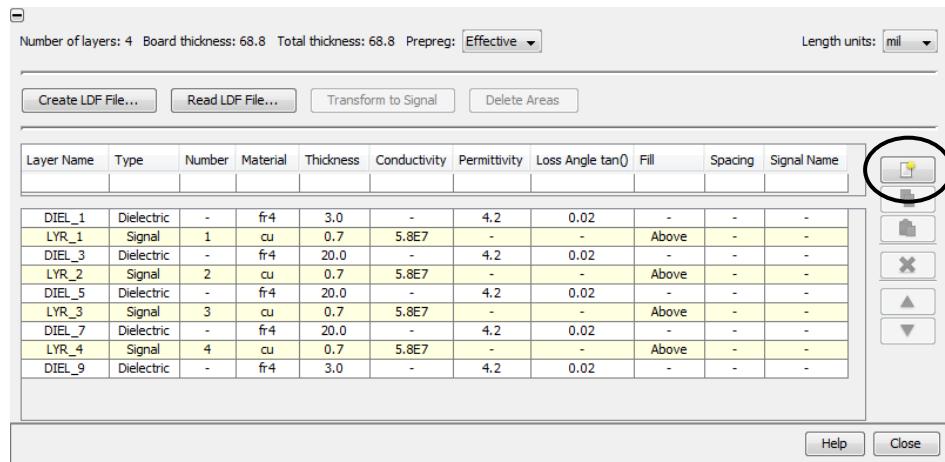


You are also encouraged to try the behavior of the settings for tab *Nets* and tab *Net Classes* by yourself.

Stackup Manager

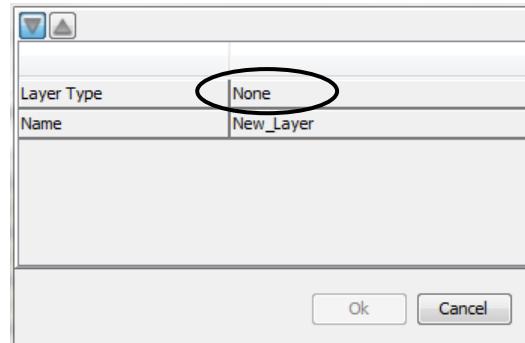
The definition of the layer stack-up is very important to the overall electromagnetic behavior of the PCB. Importing a layout design via an EDA-import does not mean that the layer stack-up has been defined correctly. Many designs neglect this important parameterization and the user has to make sure the layer stack-up is correctly defined.

The layer stack can be edited in the *Stackup Manager* dialog. We can open the dialog box by selecting *Home: Layout* \Rightarrow *Stackup*. The following dialog box will appear:



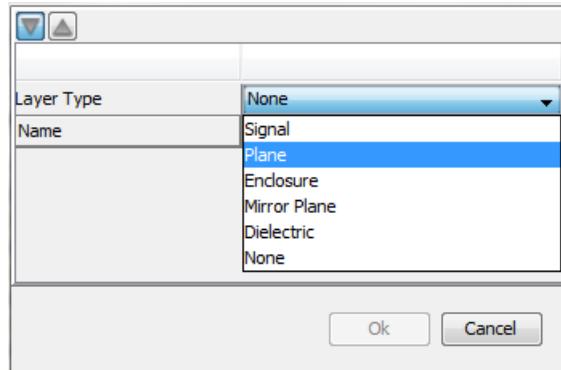
We see the number of layers and the thickness of the board. There are four metallic layers *LYR_1*, *LYR_2*, *LYR_3* and *LYR_4* in the table. These metallic layers are separated by dielectric layers and normally there are two additional dielectric layers on the bottom and the top of the board.

The different columns in the table provide all the relevant settings. The *Layer Name* and the *Type* can only be defined during the creation of a new layer. In order to do this, we press the *Create New Layer* button (marked symbol in the dialog box above). The following dialog box will appear:



To choose whether the layer is metallic or dielectric, we select the marked cell in the dialog box above.

A list will drop down giving us the selection list as shown in the figure below:



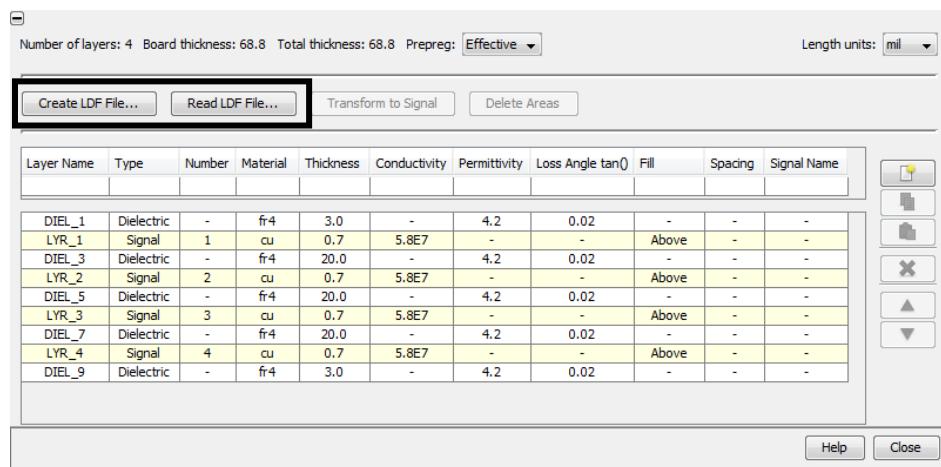
Signal and *Plane* are both of type metallic. Besides the *Dielectric* type, there are two additional types, namely *Enclosure* and *Mirror Plane*. Both are metallic layers but do not belong to the board itself but rather they provide the possibility to define the environment around the board. We don't want to create a new layer, therefore we press *Cancel*.

The *Material* column allows the selection of a material type from the material library. The selection depends on the layer type: for metallic layers only metallic materials can be selected and for dielectric layers only dielectric materials can be selected. According to the chosen material, the columns *Conductivity*, *Permittivity* and *Loss Angle tan()* are set automatically.

In the *Fill* column we are able to define the position of the conductive structures in the metallic layer relative to the boundary line of the dielectric underneath. The situation is best explained for *Diel_9*, *Diel_7* and *LYR_4* with the help of the next figure:



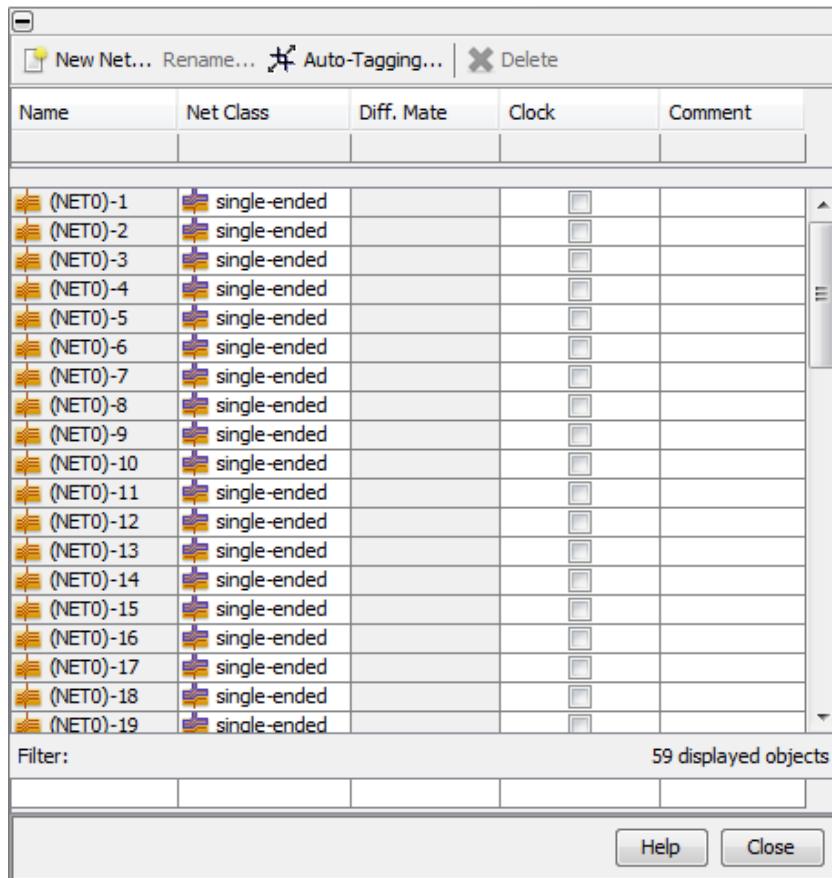
The *Stackup Manager* allows saving or loading of a certain layer definition. This can be done by simply pressing the *Create LDF File* button or the *Read LDF File* button as shown in the figure below:



LDF stands for Layer Definition File. This storage function is useful when importing different designs based on the same layer stack-up technology. It can also be useful when optimizing the electromagnetic behavior of a certain design by trying different layer stack-up technologies. We now close the dialog box and examine the Net Class Manager.

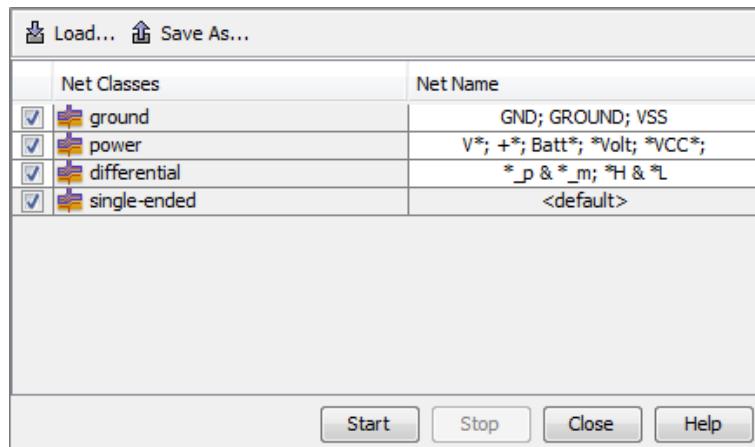
Net Editor

In order to assign the different nets to the corresponding net classes we open the Net Class Manager with *Home: Layout* \Rightarrow *Net Editor*.

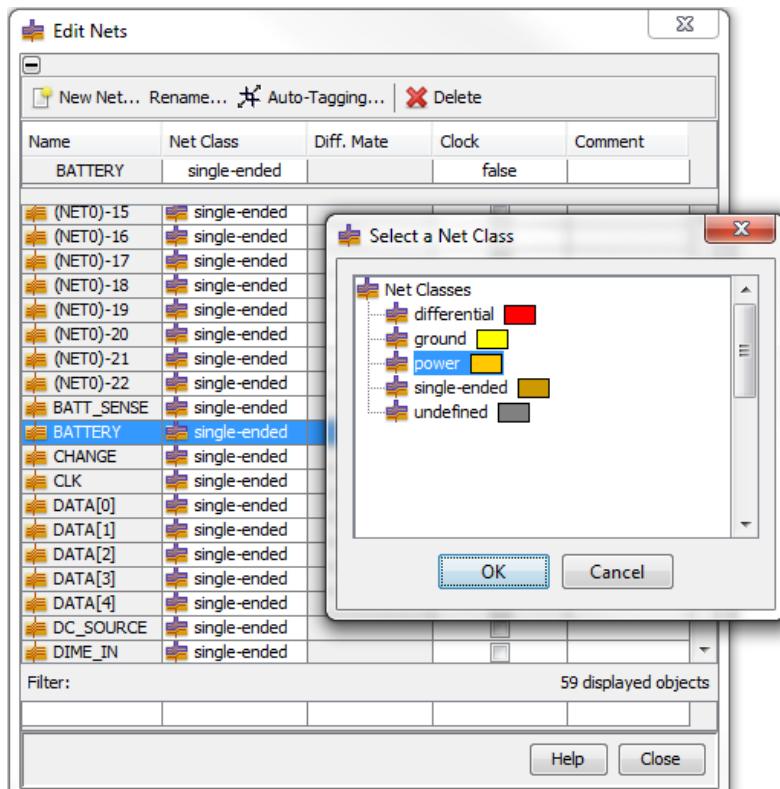


The dialog box consists of several columns, but we are interested in the first and second only. The first column lists the nets and the second the corresponding net classes. We scroll down and see that net GND is automatically assigned to net class *ground* and the net VCC is automatically assigned to the net class *power*.

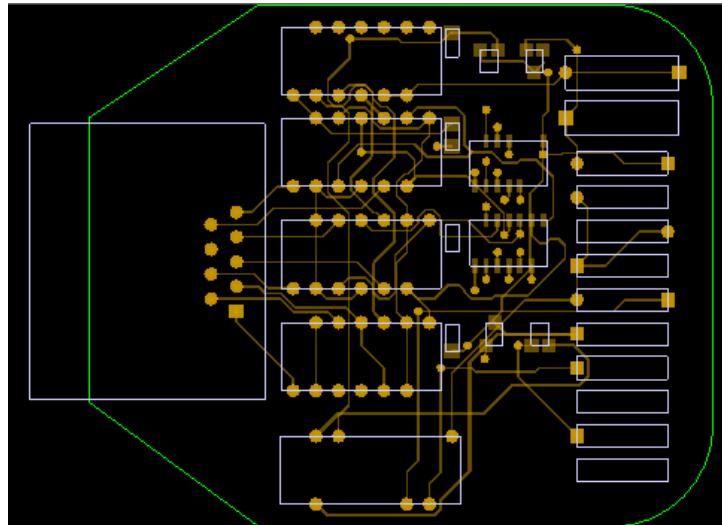
This automated assignment can be controlled by defining special syllables the program can search during the import of the layout. To see the syllables which are defined by default we press the *Auto-Tagging* button on the upper menu bar of the dialog box. The *Nets Auto-Tagging* dialog box will appear as shown in the figure below:



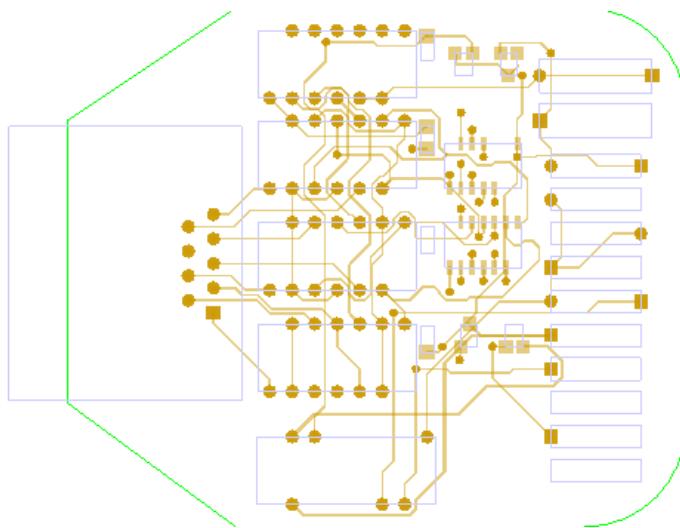
In order to assign e.g. net *Battery* to net class *power*, we just double-click on the corresponding cell in the *Net Class* column and



To see the effect of the assignment we now select *View: Color* \Rightarrow *Color Mode* \Rightarrow *Net Classes*. Then we move to the *View Options* window and select the *Net Classes* tab. Finally we select the row *single-ended*. All single-ended nets will be displayed as shown in the figure below:

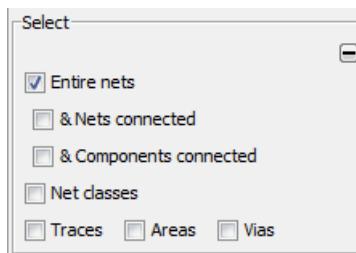


In order to remove the black background color, we uncheck the button *View: Color ⇔ Black Background*. Now, the *Main View* should look like in the figure below:



Select Filter

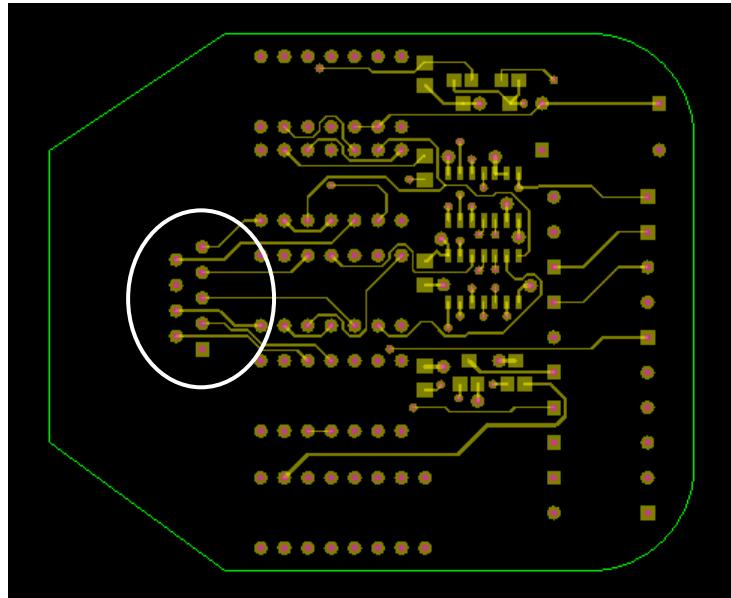
The *Select filter* supports many actions related to the selection of objects on the PCB and we have already seen in the last chapter how to control the selection mechanism by checking different buttons inside the *Select* frame (see also figure below):



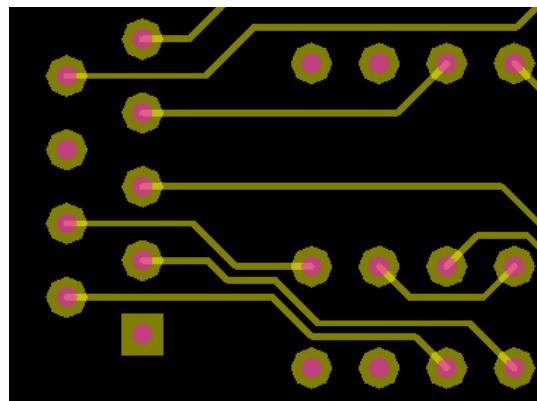
We can either select the entire nets, even if we just select one single trace of the net (if it is checked as in the figure above), or you can select a single trace e.g. by checking *Traces* instead of *Entire nets*. If we check the button “*& Nets connected*” not only an entire net will be selected but also other nets that are separated from the original selected net by components like resistors or resistor arrays. We will see this powerful function in the example *SI on Multilayer* in chapter 3.

In general there are two possibilities to select an object. It can be done either by selecting the object inside the *Navigation Tree* or by simply clicking on it in the *Main View*. Navigating and selecting on the PCB can be a difficult task because of the large number of layers, conductors and components. The built-in select mechanism observes the selection actions of the user and notes the selected objects for a further treatment.

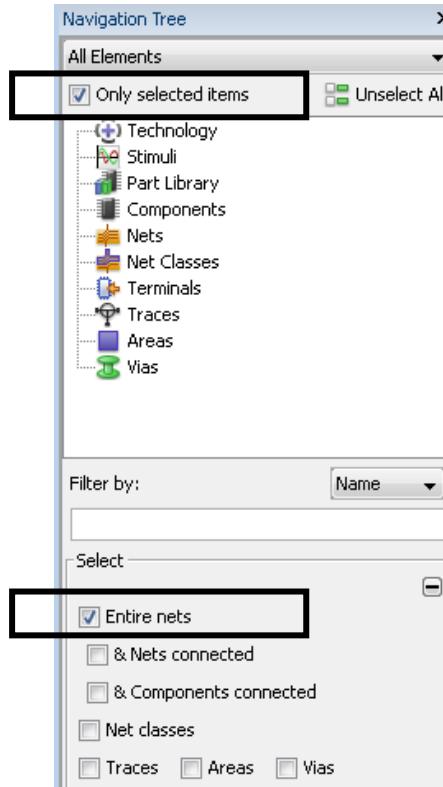
To show some further select functions we first switch the *Color Mode* back to layer (*View: Color* \Rightarrow *Color Mode* \Rightarrow *Layer*) and activate the black background color again (*View: Color* \Rightarrow *Black Background*). Then we go into the *View Options* window, change to the *Layers* tab and select layer *LAYER_1*. The *Main View* should look like in the figure below:



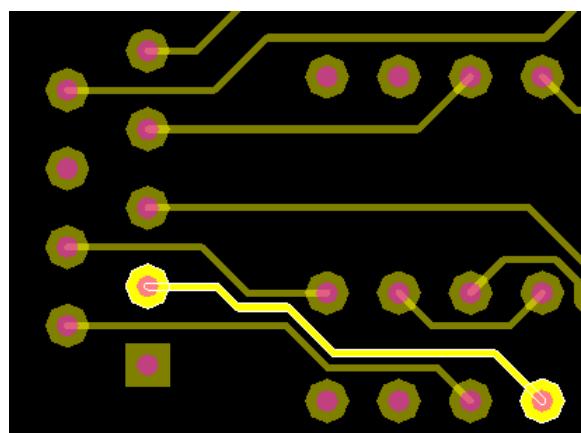
Next we zoom into the marked region of the figure above and get a display as shown in the figure below:



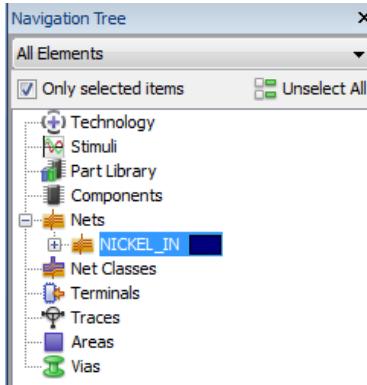
Now, before we select a net, we first make sure that *Entire nets* is marked inside the *Select* frame. Next we check the button *Only Selected Items* at the top of the *Navigation Tree*:



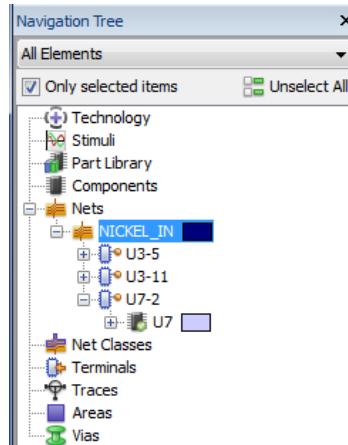
All listed items inside the *Navigation Tree* vanish immediately and we will see the top folder structure only. We now select a net in the *Main View* as shown in the figure below:



Now we observe the following effect: The net is noted in the *Navigation Tree* as shown in the figure below:



We can now expand the item and navigate to the available connected objects:



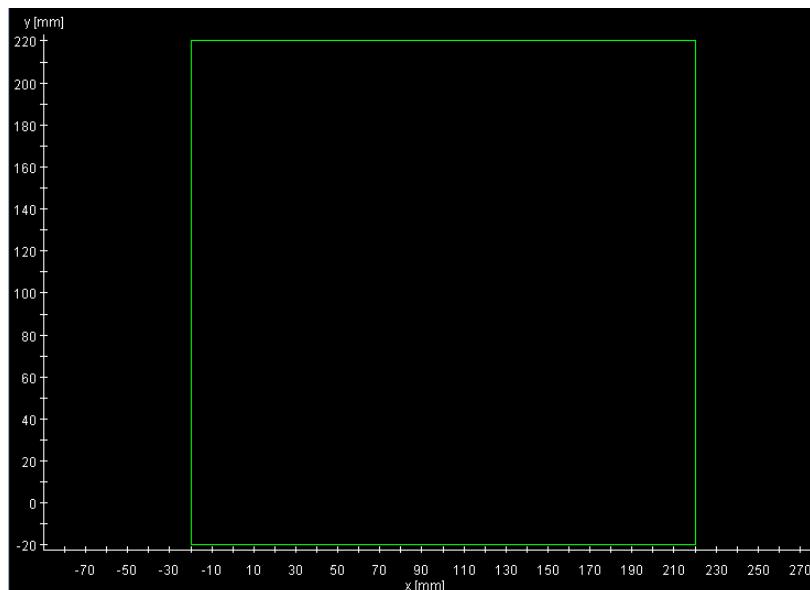
Once you are familiar with this function it will prove to be useful when navigating around the PCB. In order to fit the PCB view to the original size again, we can either use *View: Change View* \Rightarrow *Reset View*, or click with the right mouse button inside the *Main View* and select *Reset view to structure* from the drop-down menu, or simply press the spacebar on the keyboard.

Editing and Checking the PCB

This section explains how to edit traces and areas and how to check and repair overlaps. First we close the existing project and create a new, empty project.

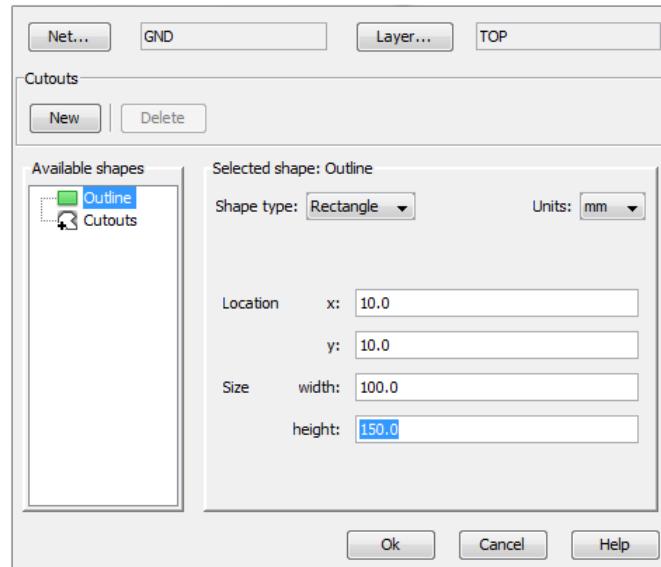
Drawing a new Trace and Area

Before we start drawing a simple rectangular area we first switch to *the Legacy Viewer* (*View: Options* \Rightarrow *View Options* \Rightarrow *Legacy Viewer*). Next we press *View: Visibility* \Rightarrow *Axes* to get the following display in the *Main View*:

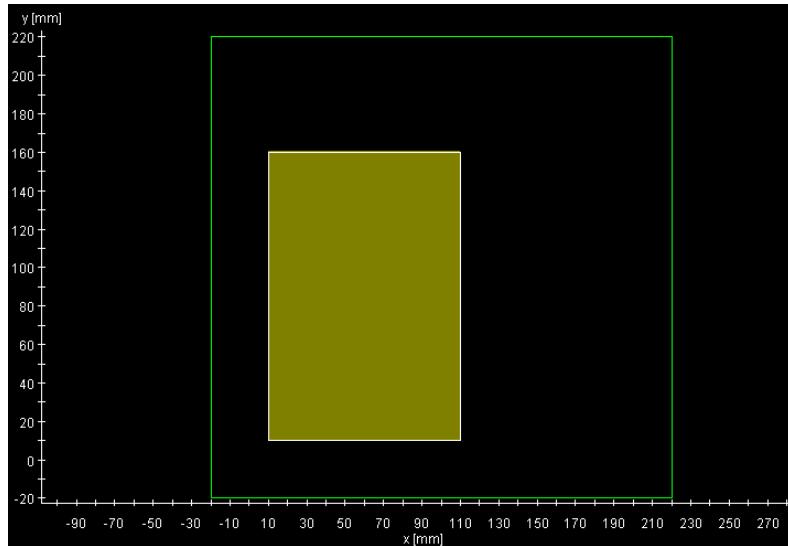


Next we press *Edit: Edit Layout* \Rightarrow *New Area*.

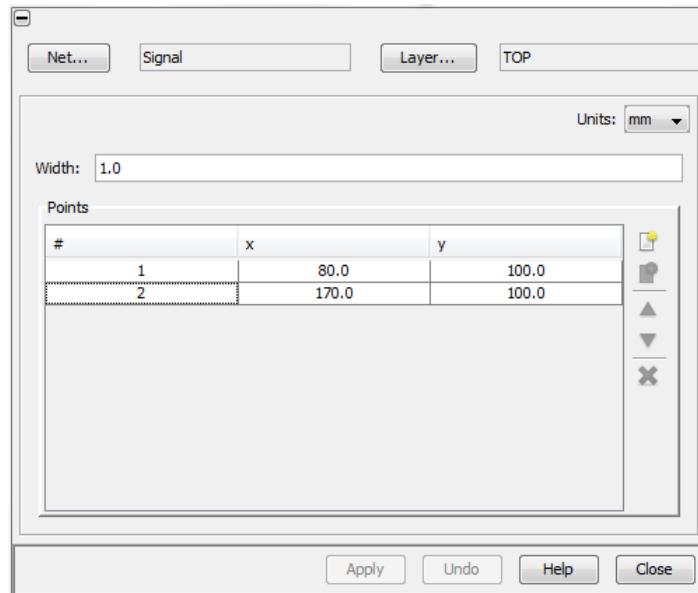
In the appearing dialog box we assign the new area to the standard net *GND*, choose *Rectangle* as *Shape Type* and enter the coordinates and size as shown in the figure below:



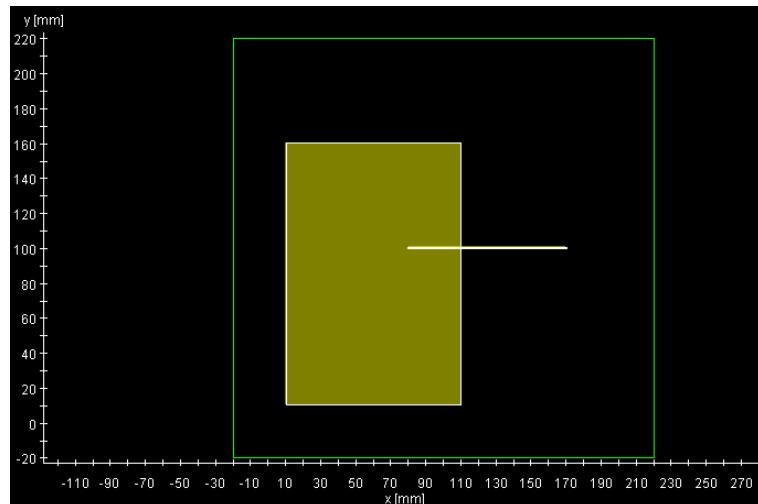
The new area should look like the figure below:



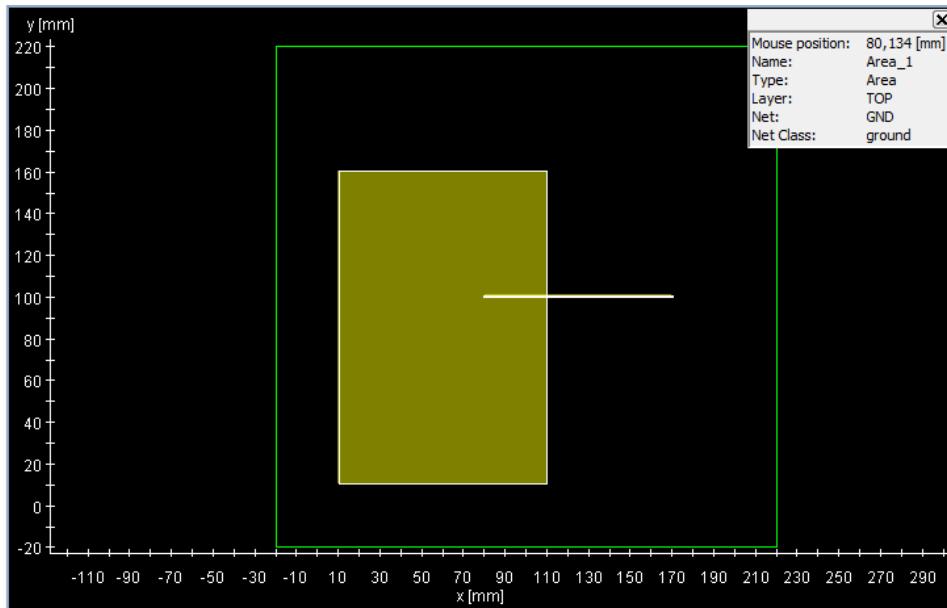
Next we create a new trace by pressing *Edit: Edit Layout* \Rightarrow *New Trace*. A dialog box will open, and then we enter the data as shown in the figure below. It is important to leave the trace to the default net *Signal*.



After pressing *Ok* and *Close*, we have two different overlapping nets as shown in the figure below:



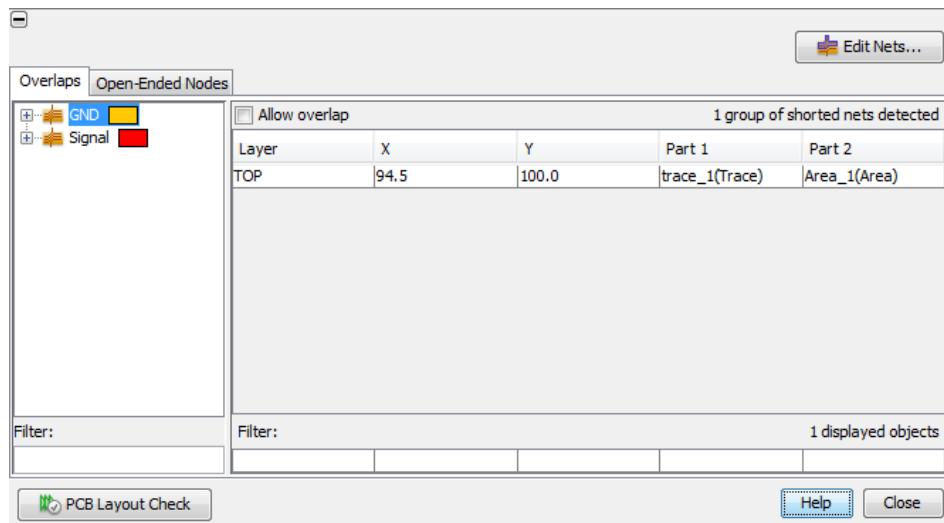
Before we go to the next section we will take a look at a useful feature: Check the button *View: Visibility* \Leftrightarrow *Object Spy*, then move the mouse cursor over the *Main View*. We will see the separate window, top right of the main view, showing the corresponding structure definition according to the current mouse position:



Layout Checker

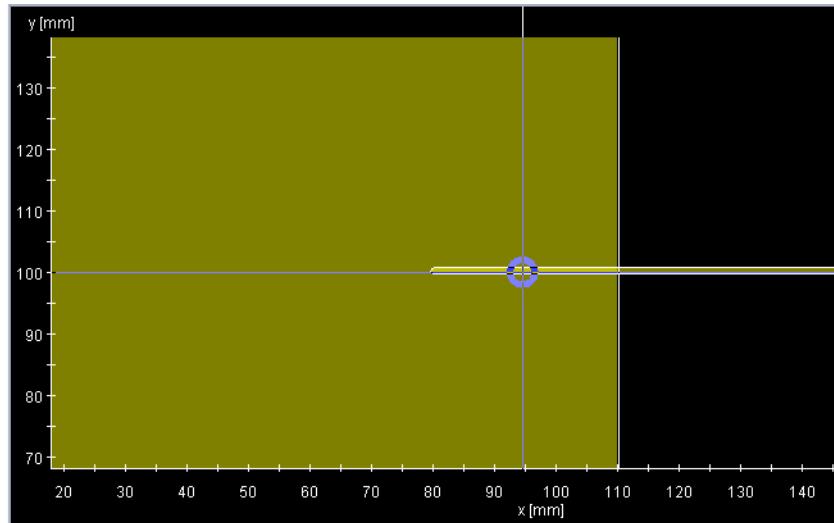
The two overlapping nets from above represent a very simple layout. Nevertheless this simple layout reproduces an issue that often occurs when importing a complex PCB layout. The input data of a complex layout may be incorrect and in order to generate a valid mesh (for the modeling phase that occurs later) it is necessary to find and repair these overlapping spots.

To find potential geometry problems we press *Edit: Check Layout* \Rightarrow *Layout Check*. A dialog box will appear where we press the *PCB Layout Check* button. The tool immediately starts to analyze the geometry of the whole PCB in order to find overlapping or open ended nets. When using this feature for a complex PCB you will see progress information in the *Messages Window*. In this simple case the report dialog box appears quickly as shown in the figure below:



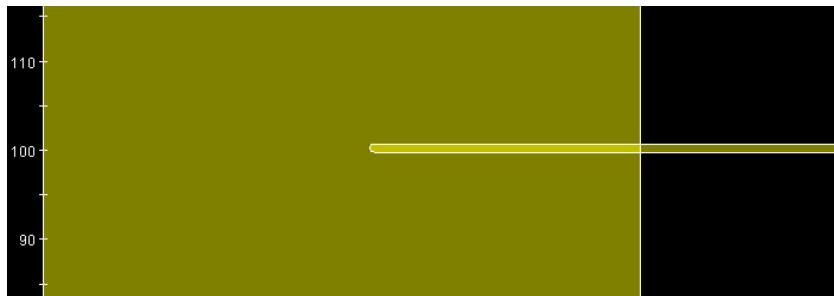
All nets contributing to an overlap will be shown in the tree on the left side of the dialog box. In our case both nets *GND* and *Signal* are listed because *GND* overlaps *Signal* and *Signal* overlaps *GND*. Upon expanding of the nets we will find all other nets that overlap with the root element. On the right side of the dialog box all positions where an overlap occurs will be listed. In our case there is only one position.

We select the cell *TOP* with the left mouse button and see the crosshair appear in the *Main View* showing the zoomed location of the overlap (in the figure below it is zoomed out again):

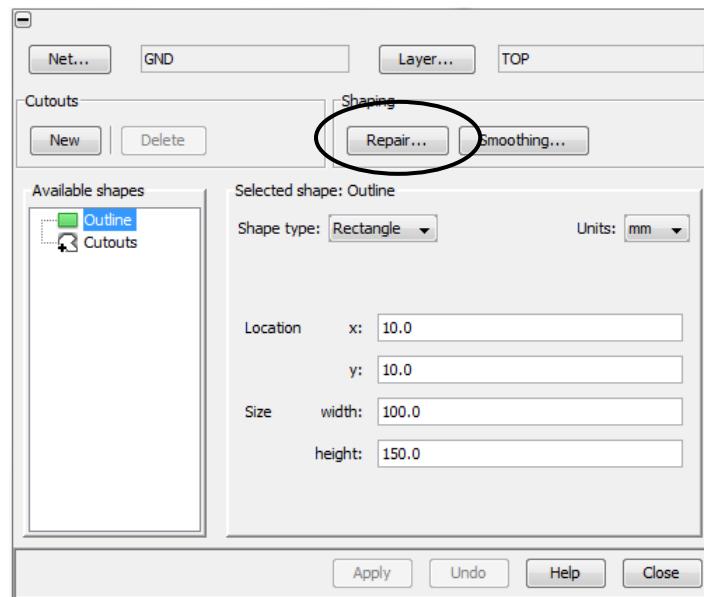


Repair Function

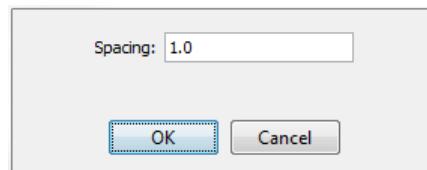
It is important to find critical regions with overlapping nets and to repair such configurations. In order to repair the overlap in a complex layout there is a powerful built-in repair function. First let's zoom into the existing layout to have a closer look at the overlap:



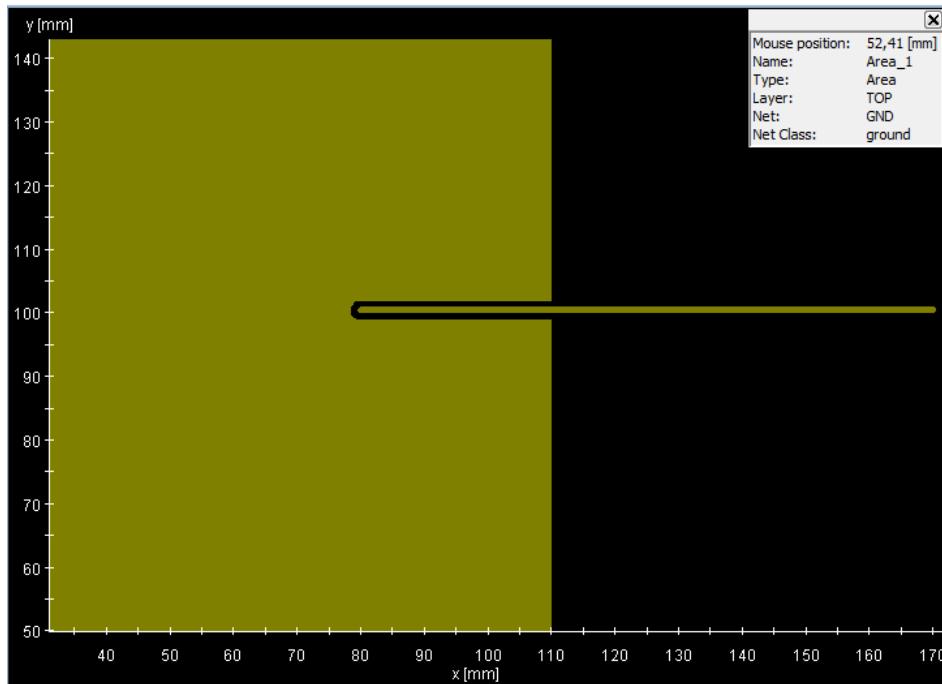
Next we go into the *Navigation Tree*, select the area and choose *Edit* by using the right mouse button. After the dialog box opens we press the *Repair* button:



A further dialog box will prompt us to enter a *Spacing* distance. The spacing distance defines the minimal distance between two conductive but not connected objects after the repair procedure. The value is interpreted in the general unit that can be set by *View: Units* \Leftrightarrow *View Units*.



We leave the default value and press **OK**. The repair algorithm now tries to separate the overlapping conductors with the given distance. A message will appear telling the successful separation. After pressing **OK** we have a layout without overlapping conductors:



We now close the project (saving is not necessary) and try out some examples.

Chapter 3 — Examples

Chapter 1 and 2 are an introduction to the handling and interface of CST PCB STUDIO. This chapter will present three simple examples offering an insight into the numerical techniques (solvers) available in CST PCB STUDIO. The first example uses the *PEEC-solver*. The second explains how to use the *2DTL-solver* and the third presents the *3DFE-solver*.

Crosstalk on Split Power Planes using PEEC Modeling

The purpose of this example is to acquaint you with the

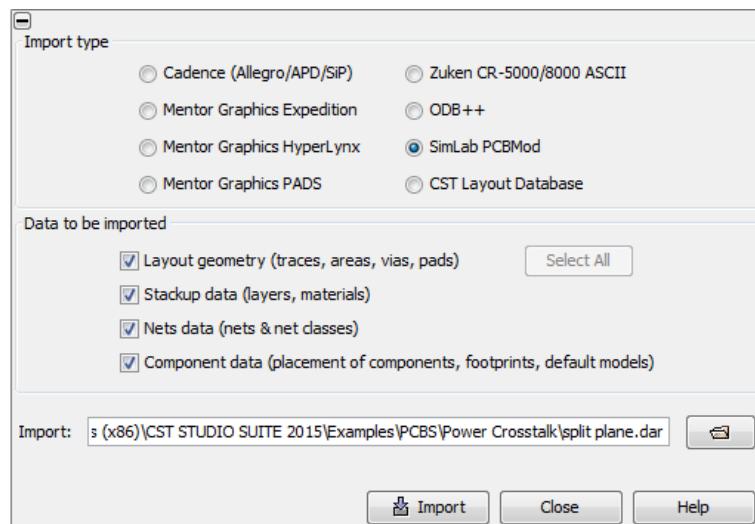
- Most important tools to edit and navigate through a PCB.
- Selection, Meshing and Modeling dialog box for PEEC.
- Usage of the PEEC model in the circuit simulator.
- Frequency domain analysis.

Task Definition

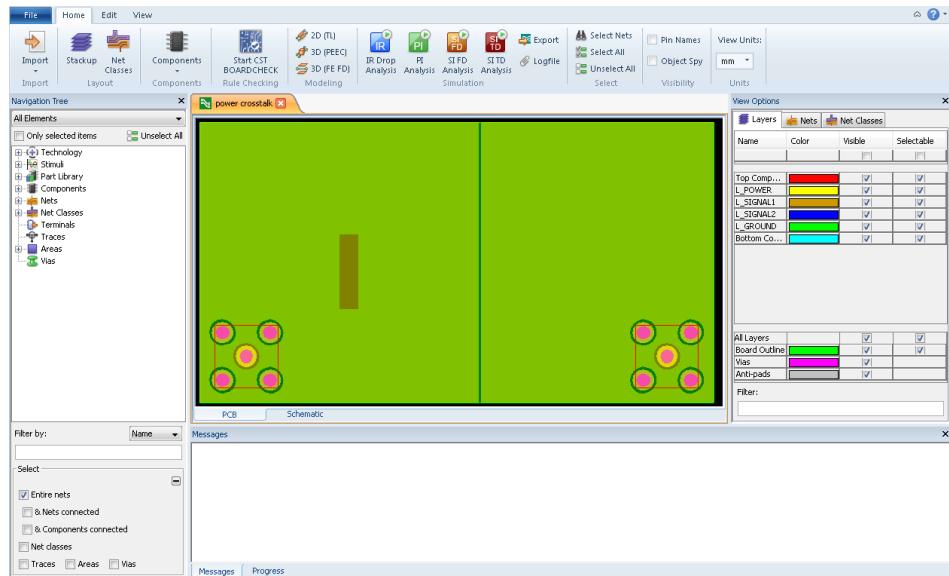
For many PCBs it is common practice to provide different power delivery systems for different applications, for example, it is common for the analog and digital systems on the board to be separated. A standard measure to prevent noise coupling from one power system to the other is to separate the power planes by introducing slots. In order to check the effectiveness of the slot in the higher frequency range, PEEC modeling can be used and this is demonstrated below.

The PCB Design

First we create a new project by importing an existing PCB design. In the corresponding import dialog box we check *Simlab PCBMod* as *Import type*.

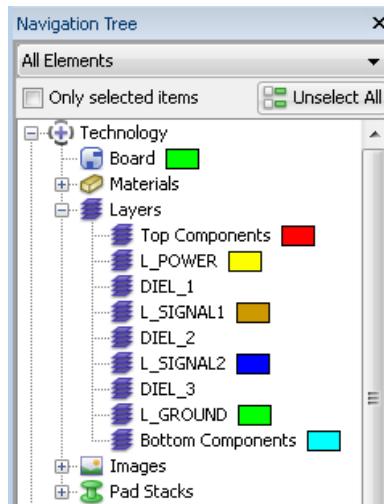


Next we use the file browser and navigate to the folder *Examples* of your *CST STUDIO SUITE* installation directory and select the file *split plane.dar* under the subfolder *PCBS/power crosstalk*. The following design will appear:

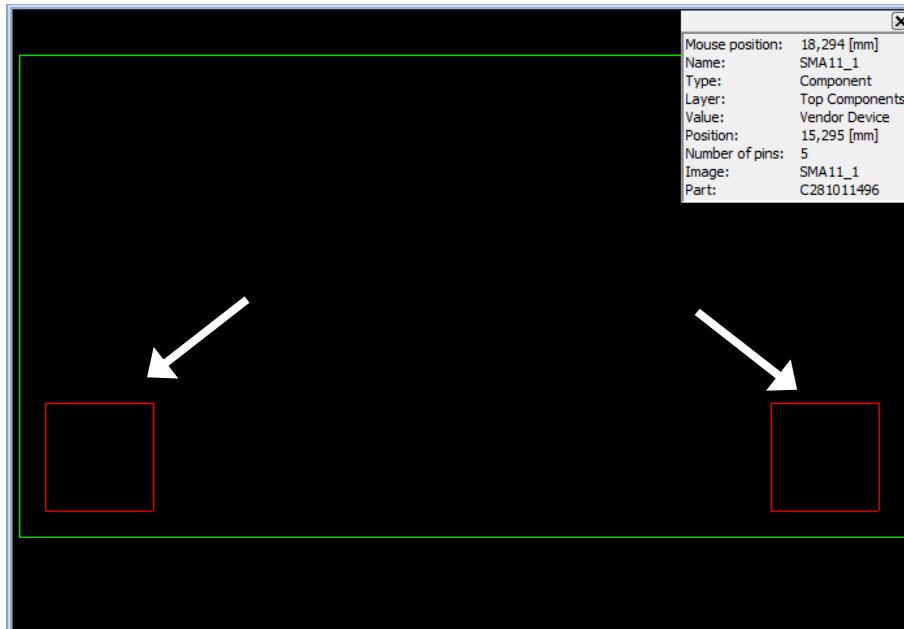


We save the project with name ‘**power crosstalk**’ and switch to the *Legacy viewer* to examine the design.

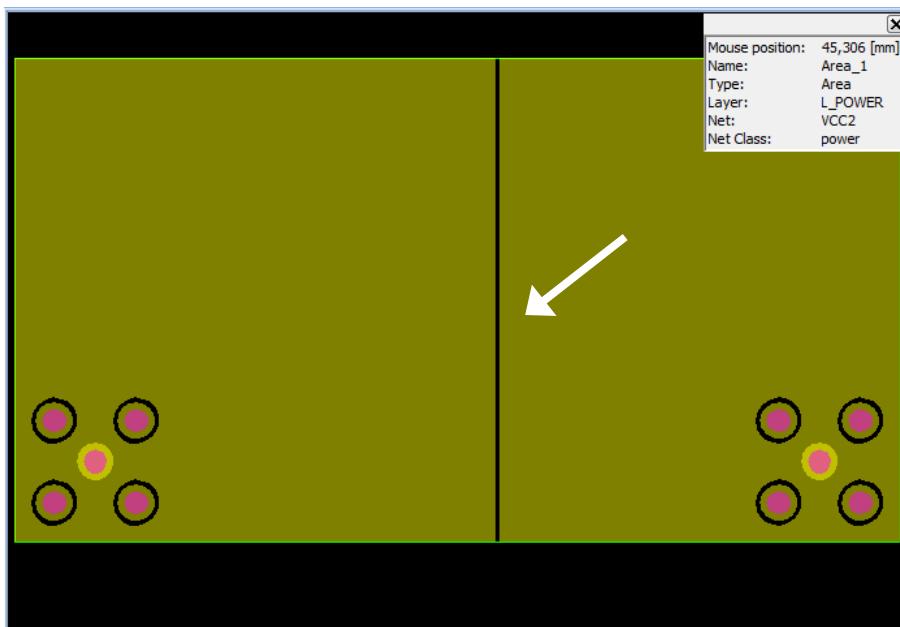
We start with having a look at the stack-up technology. Therefore, we expand the folder *Navigation Tree: Technology* \Rightarrow *Layers*. We notice there are four metallic layers *L_POWER*, *L_SIGNAL1*, *L_SIGNAL2*, *L_GROUND* and the corresponding dielectric layers in between.



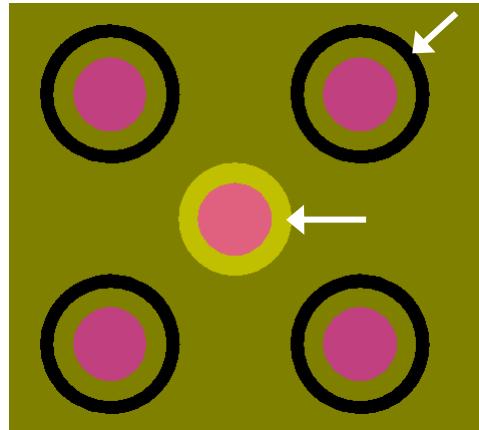
In order to investigate the layers, we go to the *View Options* window, select the *Layers* tab and then select the first layer *Top_Components*. Next we switch on the object spy (*View: Visibility \Rightarrow Object Spy*) and move the mouse cursor over one of the red marked frames on the lower side as shown in the figure below:



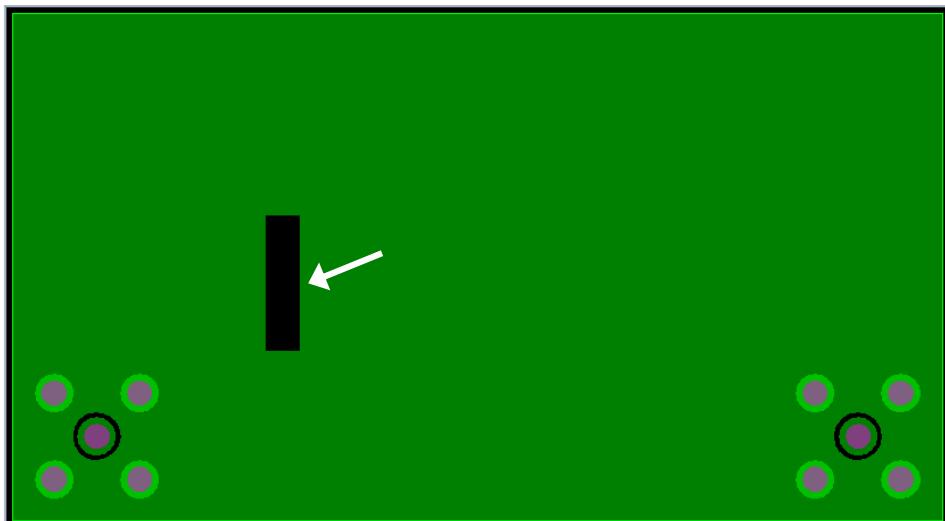
Next we select layer *L_Power* and see two different planes which are separated by a thin slot:



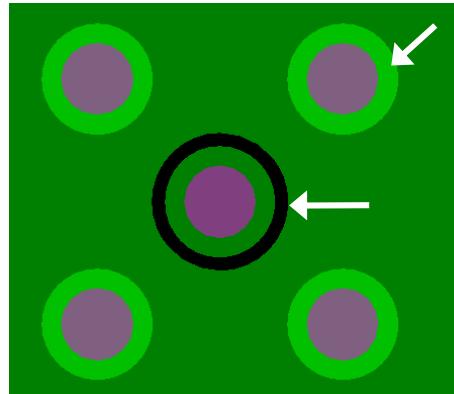
Besides the slot we see the characteristic via pattern of the SMA sockets. We switch off *Object Spy* and zoom into the region of the left socket:



It can be seen that the pad of the center via (in yellow color) is connected to the power plane whereas the pads of the four outer vias are separated by an insulation anti-pad (in black color). We again zoom out (by using right mouse click and selecting *Reset view to structure* from the drop down menu) and select the next layer *L_Signal1*. The layer is empty besides the small conductive pattern of the vias and their corresponding pads and this is also true for *L_Signal2*. Next we select *L_Ground*. We see a single plane with a cutout on the left side as shown in the figure below:

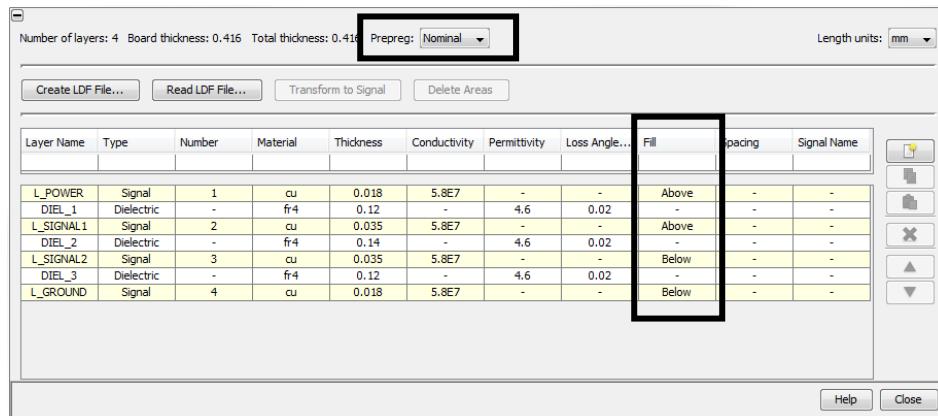


If we again zoom into the region of one of the sockets we now see the pads of the outer vias are connected to the plane and the pad of the center via is insulated:



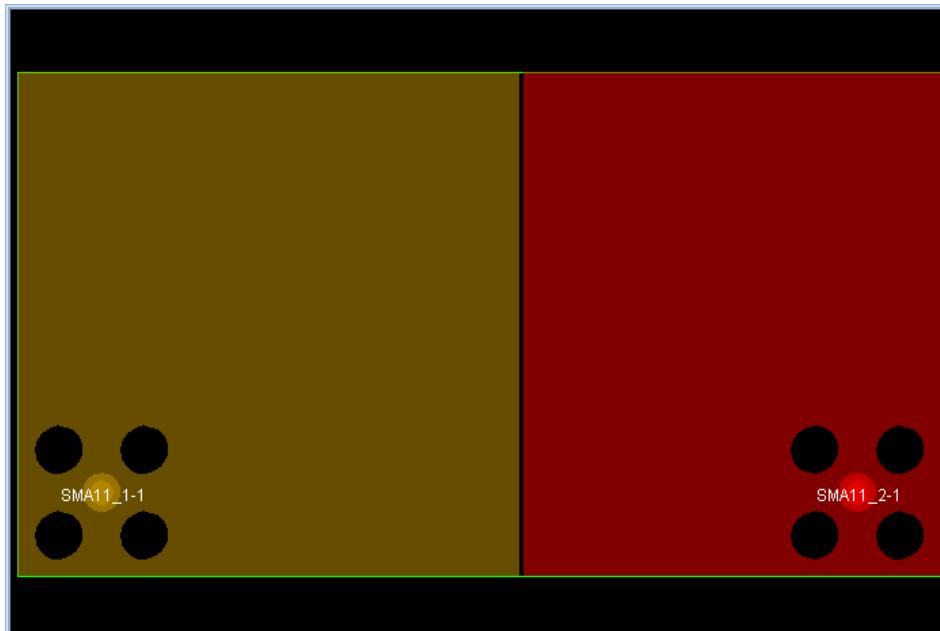
The layer *Bottom Components* is an empty layer and we don't have to consider it.

In order to investigate the layer stack-up technology we press *Home: Layout* \Rightarrow *Stackup*. First we look at the *Prepreg* parameter and see its value is assigned to *Effective*. We change the value to *Nominal*. We also see the two upper metallic layers are of type *Fill = Above*, whereas the two lower metallic layers are of *Fill = Below*. For a deeper insight of the Preprep- and Fill parameter we refer to the CST PCB STUDIO online help.



The upper and the lower dielectric layers have a thickness of 0.12 mm whereas the middle one has a thickness of 0.14 mm . The material for all dielectric layers is *fr4* and the overall thickness of the board is about 0.4 mm and this will determine the mesh size in the later *Meshing and Modeling* section.

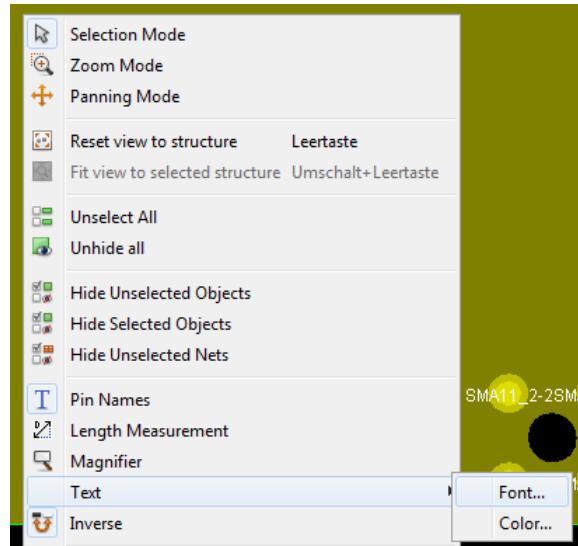
We continue our investigation by having a look at the available nets. We first select layer *L_Power* in the *Layers* tab of the *View Options* window. Then we select *View: Color* \Rightarrow *Color Mode* \Rightarrow *Nets* and once again change to the *View Options* window to select the *Nets* tab. Next we select *VCC1* and *VCC2* by using *Shift* + left mouse button. In order to see the pin names of the nets on these layers, we press *View: Visibility* \Rightarrow *Pin Names*. We should now have the following display:



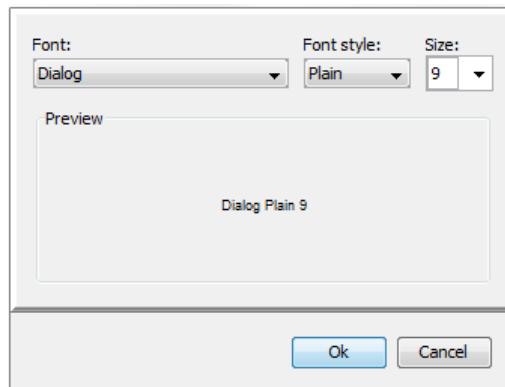
To see the *GND* net on the *L_Ground* layer first select net *GND* in the *Nets* tab (in the *View Options* window) and then change to tab *Layers* and select layer *L_Ground*. If you zoom into the lower region you will see each socket is connected to *GND* by four pins as shown in the figure below:



If the text size of the pin names doesn't fit, similar to the figure above, we can change it by right clicking in the *Main View* and selecting the *Text* item in the drop-down menu as shown in the figure below:



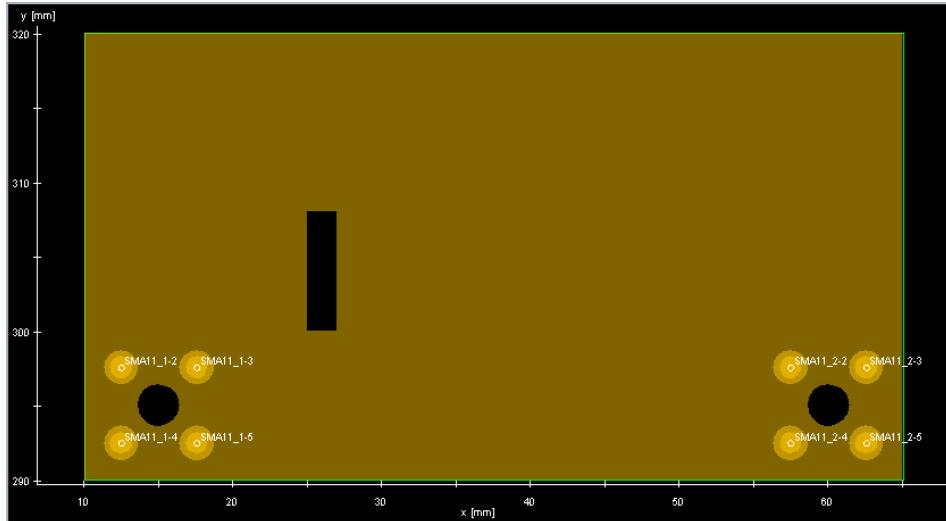
In the dialog box we choose a smaller font size as shown below:



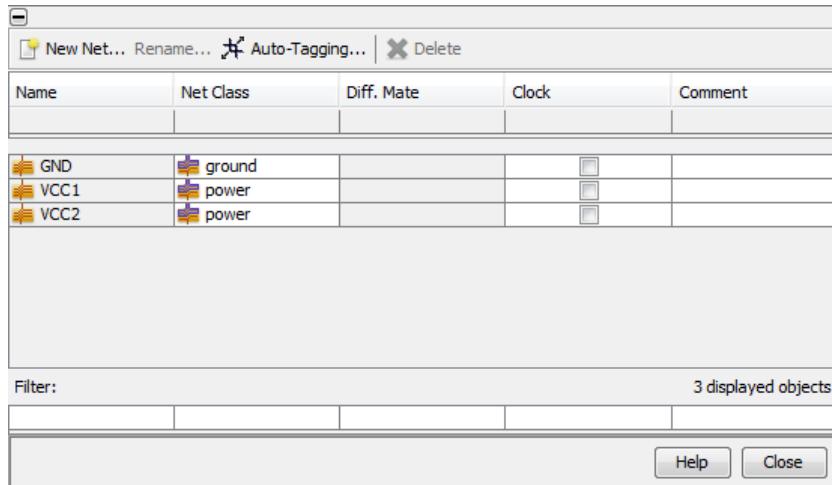
This helps to avoid overlapping pin names:



Next we zoom out again and switch on the axes via *View: Visibility \Rightarrow Axes*. Displaying the axes scaling helps to estimate the real dimensions of the PCB and this can give a good orientation on the mesh size to be chosen in the next section. The *Main View* now should look similar to the figure below:



Before we open the meshing dialog box we will finish this section by having a look at *Home: Layout \Rightarrow Net Editor*.



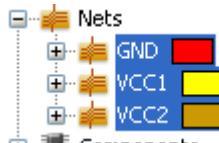
We see that net *GND* is assigned to net class *ground* and the two nets *VCC1* and *VCC2* are assigned to net class *power*. This is an important fact because any net assigned to net class *ground* or *power* can be treated as an ideal **reference conductor** during the PEEC modeling process. No separate inductive or capacitive elements will be generated for reference conductors. Their contribution is considered in the capacitive and inductive value of the remaining *signal* elements.

Assigning a net to net class *ground* and choosing net class *ground* as reference can speed up the modeling and simulation phase, but it is only effective if the assumption of an ideal reference conductor is sufficiently fulfilled. A conductor can be interpreted as an ideal reference conductor if it allows a sufficient current return path along the path in the vicinity of the corresponding *signal* conductor. This is, for instance, not true if the conductor has considerable slots or contractions. As a first step we will model the *GND* net as an ideal reference conductor and then change it to see the effect of the slot inside the conductor.

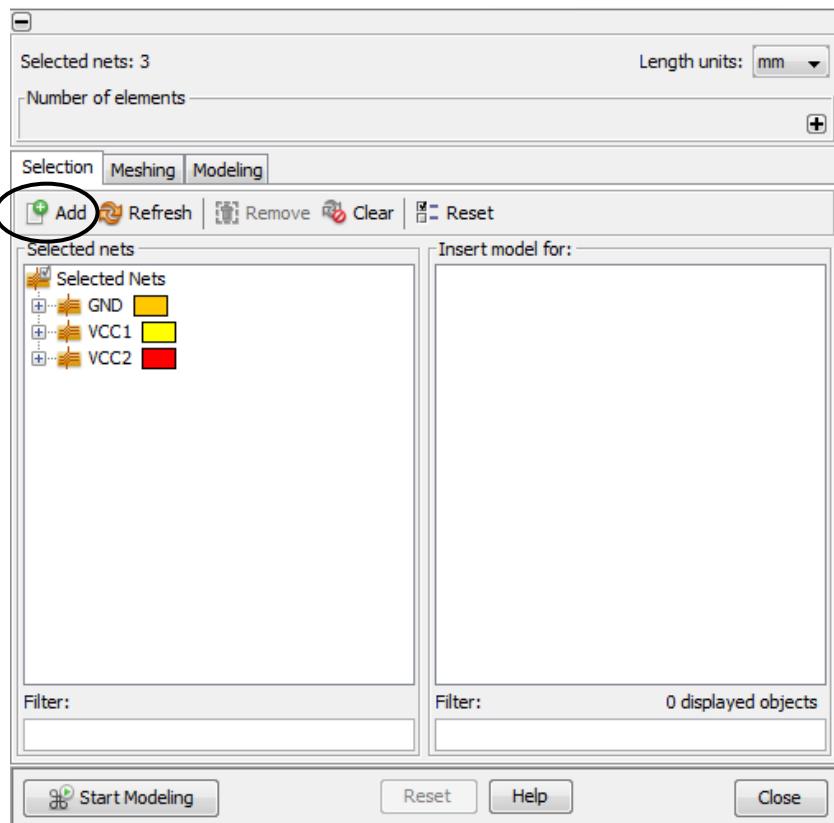
Meshing and Modeling

To start with meshing, we first turn off the legacy viewer, which means activating the default viewer (*View: Options* \Rightarrow *View Options*).

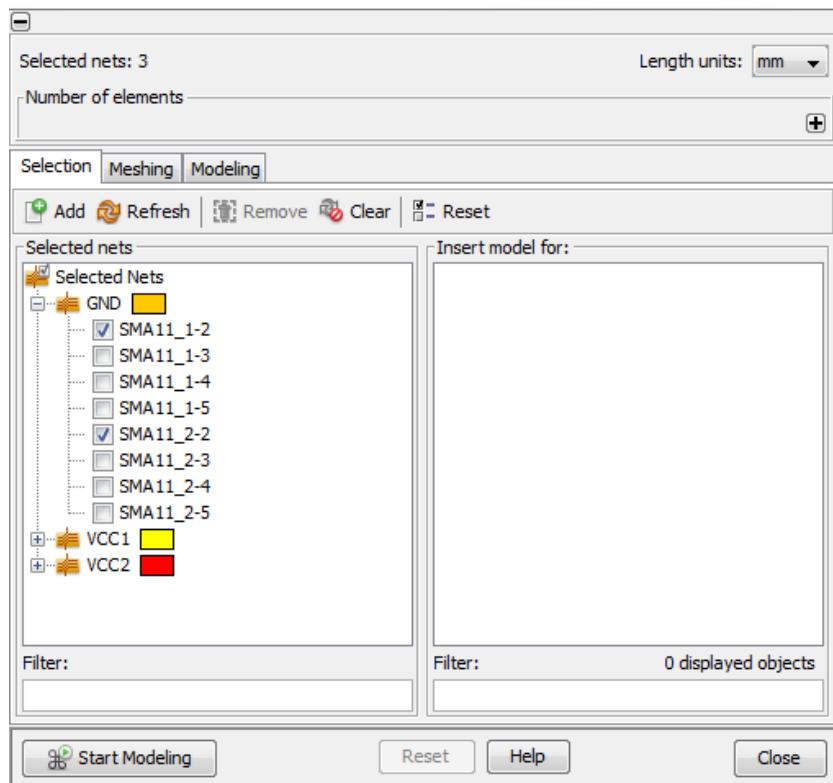
Next, we select the three nets in the *Navigation Tree* as shown in the figure below:



Next we select *Home: Modeling* \Rightarrow *3D (PEEC) Model*. In the dialog box we choose the *Selection* tab. Next we add the three selected nets by pressing the *Add* button:



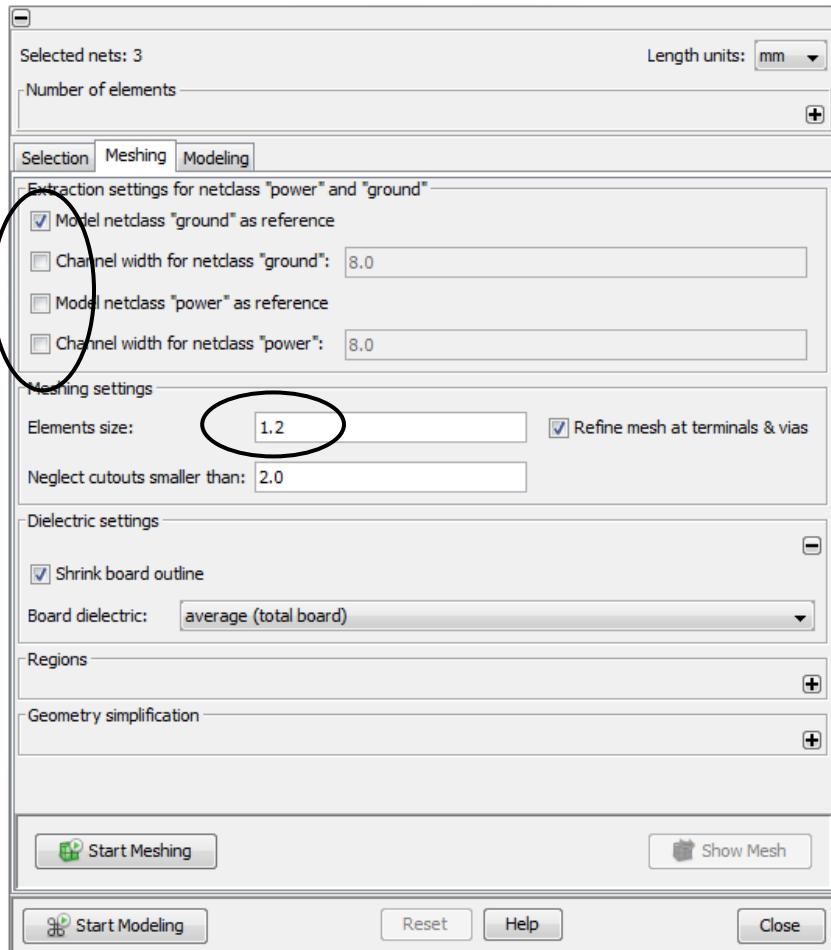
These three nets will be considered during the meshing and modeling phase. We now expand net *GND* in the list of *Selected nets*:



We see the list of all available pins on net *GND*. Every checked pin will appear as a terminal in the equivalent circuit, which will be generated later, provided that *GND* is not considered as a reference conductor. Although *GND* will be interpreted as a reference conductor in the first simulation, we will prepare the pin selection for later simulation set up.

The two pins of interest are: *SMA11_1-2* and *SMA11_2-2*. All other pins should be deselected by double-clicking on the corresponding check box. Expand net *VCC1* and *VCC2* and see the available pins are selected by default.

We keep these settings and move to the *Meshing* tab:

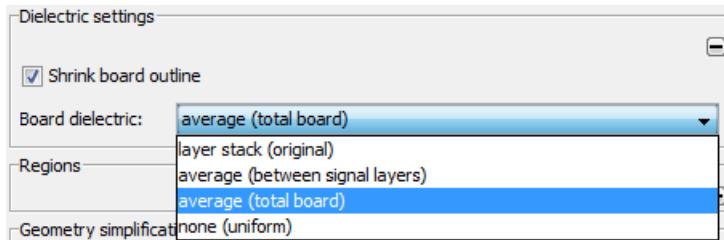


We now want to investigate the different available settings. The first frame, *Extraction settings for netclass "power" and "ground"*, determines whether net class *power* and *ground* should be modeled as a reference conductor or not.

In addition a *Channel width* can be assigned to both, net class *power* and *ground*. The channel width can significantly reduce the size of the overall structure to be calculated. This is a powerful feature when modeling transmission lines along or between reference conductors, because the whole reference conductor will not be considered but only parts within the specified channel width around the transmission line. In our example there is no transmission line, but rather there are power planes which are of similar size as the ground reference planes. Therefore, specifying a channel width does not make sense. We deselect the option for both netclass *ground* and netclass *power* (see figure above).

The next frame, *Meshing settings*, allows the specification of the mesh cell size for the PEEC mesh cell. We set the value to *1.2 mm* and keep the other parameters as their default values.

The next frame is *Dielectric Settings*. If we drop down the menu *Board Dielectric*, we see four choices of how to treat the dielectric layers during the modeling phase:



The first entry, *layer stack (original)*, means each dielectric layer will be considered during the capacitance calculation. This is the most costly but also most precise treatment of the dielectric layers. The second item *average (between signal layers)* performs an averaging of all dielectric layers between two adjacent metallic layers.

The third item, *average (total board)*, causes an averaging between all dielectric layers of the board. This approximation speeds up the capacitance calculation procedure but the user has to be aware of this simplification. In our case there are three dielectric layers consisting of the same material and therefore we will choose this option for our calculation without any loss of accuracy.

The last item, *none (uniform)*, ignores the presence of any dielectric and the user is able to define a *background* dielectric material. Choosing this function makes the capacitance calculation as fast as possible. It can be useful for a rough and quick estimation of the electromagnetic effects or in cases where the capacitive effects of the board are not dominant.

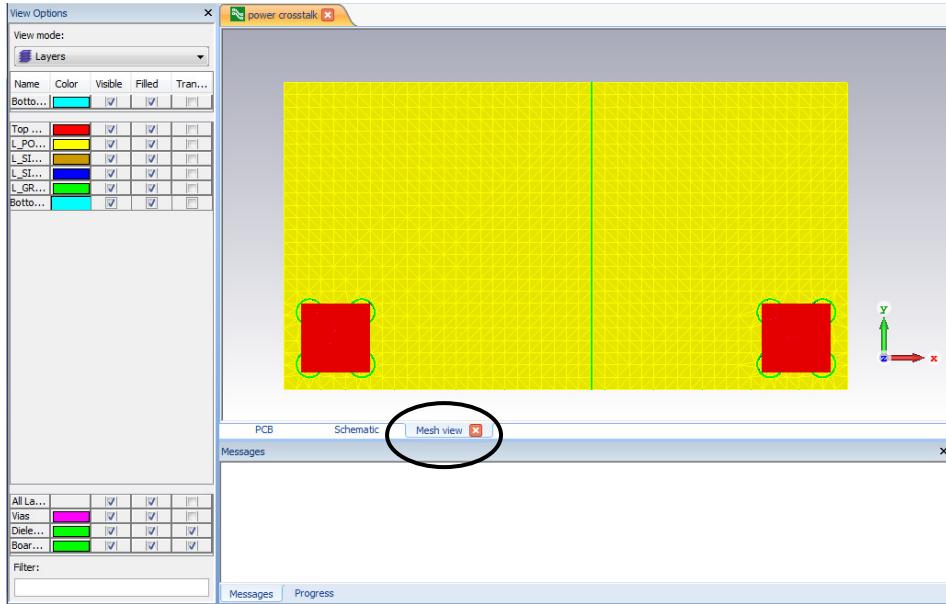
Checking the box *Shrink Board Outline* helps to shrink the overall board when only conductors in a small bounded region are selected. In this case the program avoids meshing the entire dielectric layer of the board but adapts the board outline to an adequate size around the selected conductors. In our case the selected conductors fill the whole board outline and therefore checking the box won't have any effect. We leave the *Shrink board outline* parameter activated.

The settings frame, *Regions*, allows the setting of a finer mesh for user defined regions on the board. We don't need this function right now and this is also true for the last settings frame, *Geometry Simplification*. It allows the setting of parameters controlling the abstraction of the board during the layout import. The parameters should only be changed by advanced users.

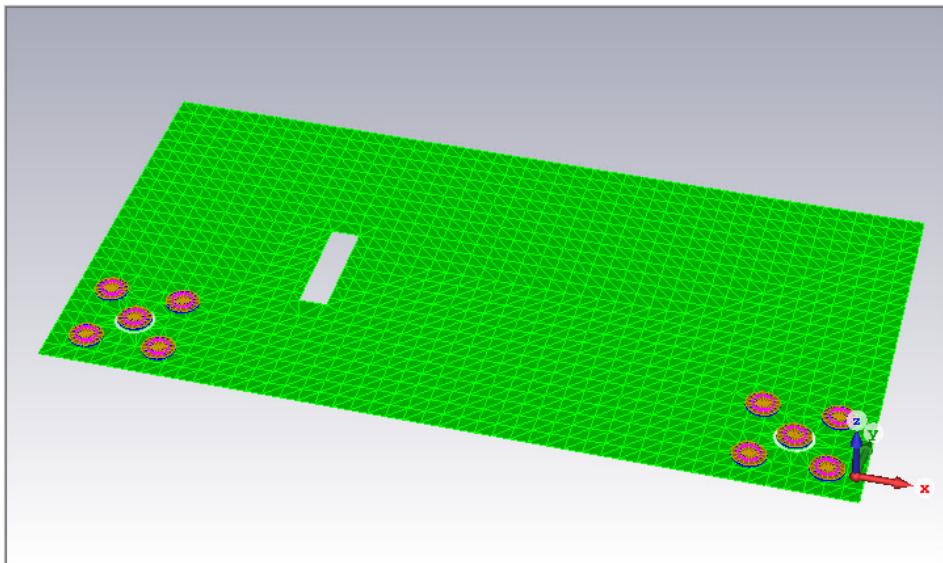
In order to start the meshing, press *Start Meshing* in the lower left corner of the tab. The meshing process will start showing some information in the *Message Window*. There will be a warning “*No DC connection found for SMA11_1_1 / SMA11_2_1*”. This means there is no further terminal for the corresponding nets *VCC1* and *VCC2* found and therefore, there will be no *DC* connection. But since we are interested in a crosstalk analysis between *VCC1* and *VCC2*, we can ignore this message.

The whole meshing process will be completed within a few seconds and the result can be displayed by pressing the *Show Mesh* button.

A *Mesh view* tab will be displayed showing the meshed layers:



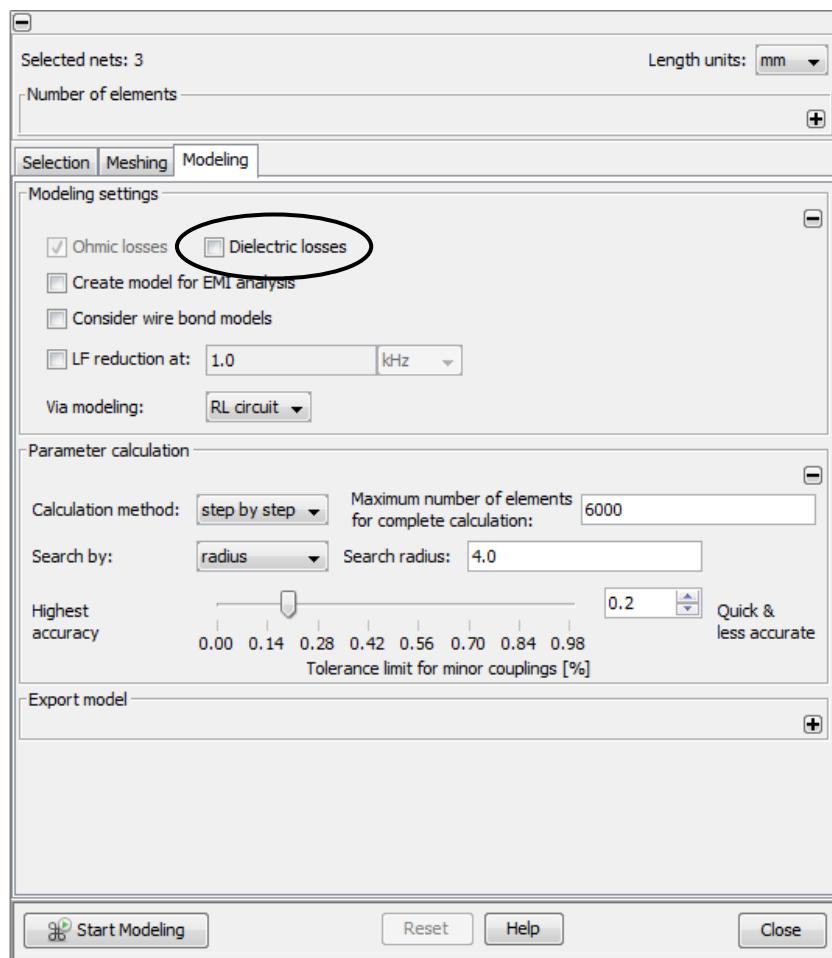
We go into the View Options window on the left side and deselect the first two layers (*Top_Comp...* and *L_POWER*). Next we click into the Main view and rotate the view in the 3D space using the rotate on the *Home tab* as shown in the figure below:



We finally reset the view by clicking space bar.

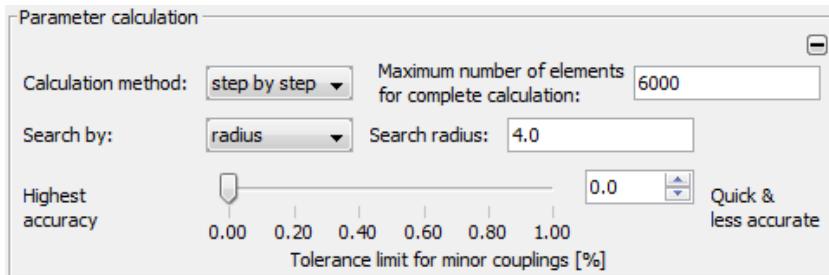
Note: The 3D mesh would be visualized in a different way if the *Legacy Viewer* was selected and the standard Viewer was chosen instead.

Next we move to the *Modeling* settings. The following dialog box will appear:



In the *Modeling Settings* frame we uncheck *Dielectric losses* in order to get a simpler model and let all other parameters by their default values.

Next we have a look at the *Parameter calculation* frame:



The settings apply for both inductance and capacitance calculations. In general there are two calculation methods: *complete* or *step by step*. The expression '*complete*' simply means that all mesh elements (*careas* and *isegs*) will be coupled with each other. This is the classical PEEC approach but it implies two problems:

First, the coupled capacitive areas, for example, are modeled by using a static capacitance and the longest distance between these areas limits the maximum allowed frequency range of the model. Therefore, in case of *complete* the maximum valid frequency is directly limited by the size of the board, ignoring all screening effects that can lead to a considerable de-coupling between different regions of the board.

Second, the calculation method *complete* in general leads to longer calculation times. The method is started by the program only if the *Maximum number of elements for complete calculation* is not exceeded. The method often leads to larger equivalent circuits that can only be avoided by using the *Tolerance limit for minor couplings*.

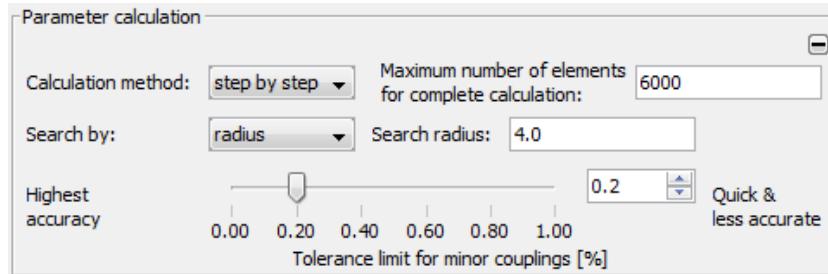
Calculation method *complete* should only be adapted when a PCB has only a few metallic structures and therefore fewer screening effects for decoupling certain regions can be expected. This is sometimes true for single-layer or double-layer PCBs.

In all other cases the calculation method *step by step* is recommended. With this method, the complete capacitance (or inductance) matrix is constructed using several calculations on different sub-regions. The size of these sub-regions is best chosen by setting the *radius* value in the *Search by* field. In general the *Search radius* should be about ten times the distance between the metallic layers or at least three times the mesh size to make sure the available conductors can lead to the expected screening effects. Screening only takes place inside an environment with considerable conductive materials.

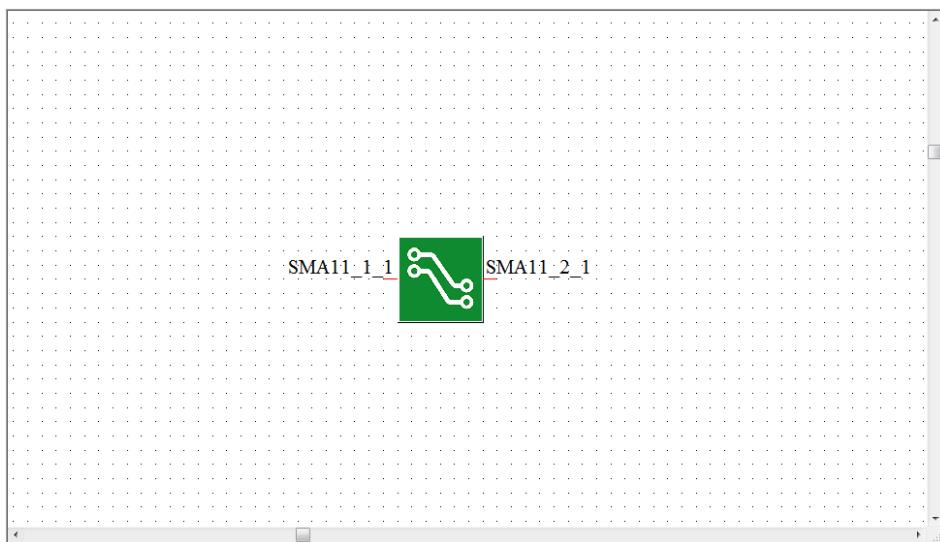
In our case there is a high presence of conductive materials on both layers allowing good screening. The mesh size was chosen to be *1.2 mm* and the distance between the layers is about *0.4 mm*, therefore we choose *4.0 mm* as *Search radius*.

Choosing value *factor* in the field *Search by* makes the program define an adequate radius on account of the existing distances between the conductors.

As a last step we change the *Tolerance limit for minor couplings* to 0.2 % as shown in the figure below. The program will delete all off-diagonal entries of the inductance- and capacitance matrix which are lower than 0.2 % of their corresponding main-diagonal values. This leads to a sparser PEEC model and to a faster simulation, especially if the *Calculation method* is set to *complete*.

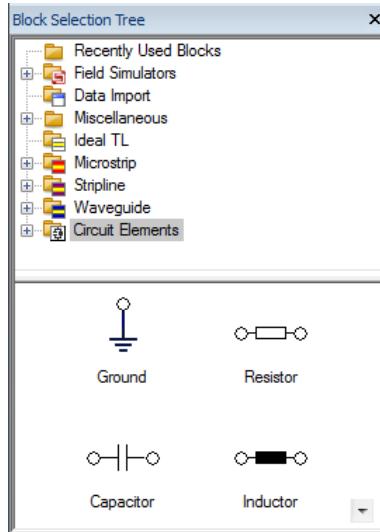


Now we press the button *Start Modeling*. The generation of the corresponding schematic symbol will take only a few seconds and we change to the *Schematic* tab:

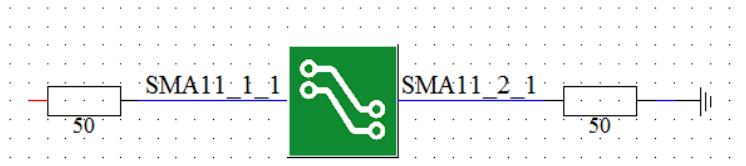


We see the two pins of net *VCC1* and *VCC2*. Because of the assumed ideal reference behavior of net *GND* there is no need for further pins and we can connect the loads between the pins and the ground reference symbol.

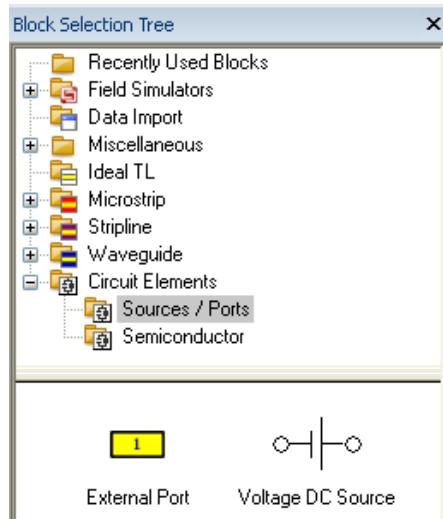
We start with putting a resistor of 50 Ohm on both terminals. In order to do this, we go into the *Block Selection Tree* and select *Circuit Elements*:



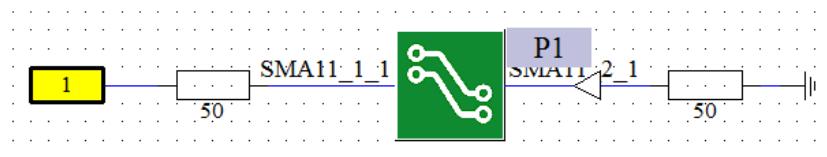
The available device symbols will appear and you can drag two resistors and a ground symbol into the *Main View* by simply drag-and-drop. The ground symbol can be rotated by using the right mouse button and should be connected to the resistor on the right terminal. The resistance value is 50 Ohm by default. The symbols can be connected by selecting *Home: Components* \Rightarrow *Connector*. For a deeper explanation how to use the schematic editor we refer to the *CST DESIGN STUDIO* manual. Our schematic should now look like in the figure below:



Next we have to complete the schematic by connecting an active port to the resistor on the left side. Therefore we go into the *Block Selection Tree*, expand *Circuit Elements* and scroll down the symbol list as shown in the figure below:

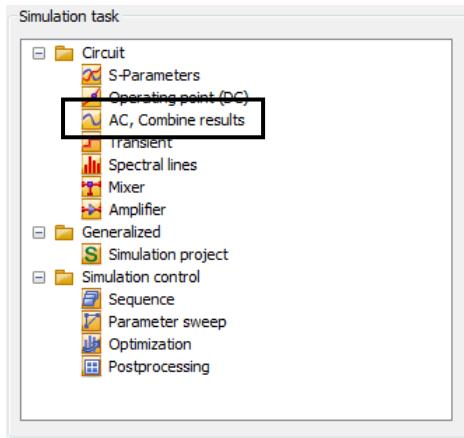


We select the yellow *External Port*, drag it on the *Main View* and connect it with the resistor. An additional *ground* symbol isn't necessary. To finish the loading, we drag a *Probe* symbol to the left side of the resistor on the right, (by selecting *Home: Components* \Rightarrow *Probe*) as shown below:

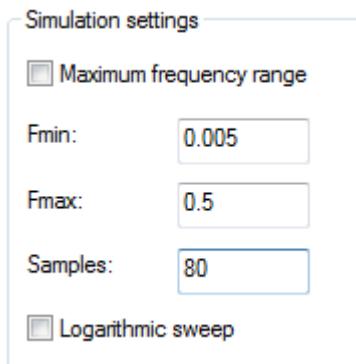


Note: the direction of the probe in your project can differ to the direction in the picture above. This is due to the fact the probe's direction depends on the direction of the connector where the probe is placed on. And the connector's direction is defined on how the connector was drawn, either from the left pin to the right pin or vice versa. But since we are interested in voltages and not currents, the probe's direction won't influence our results.

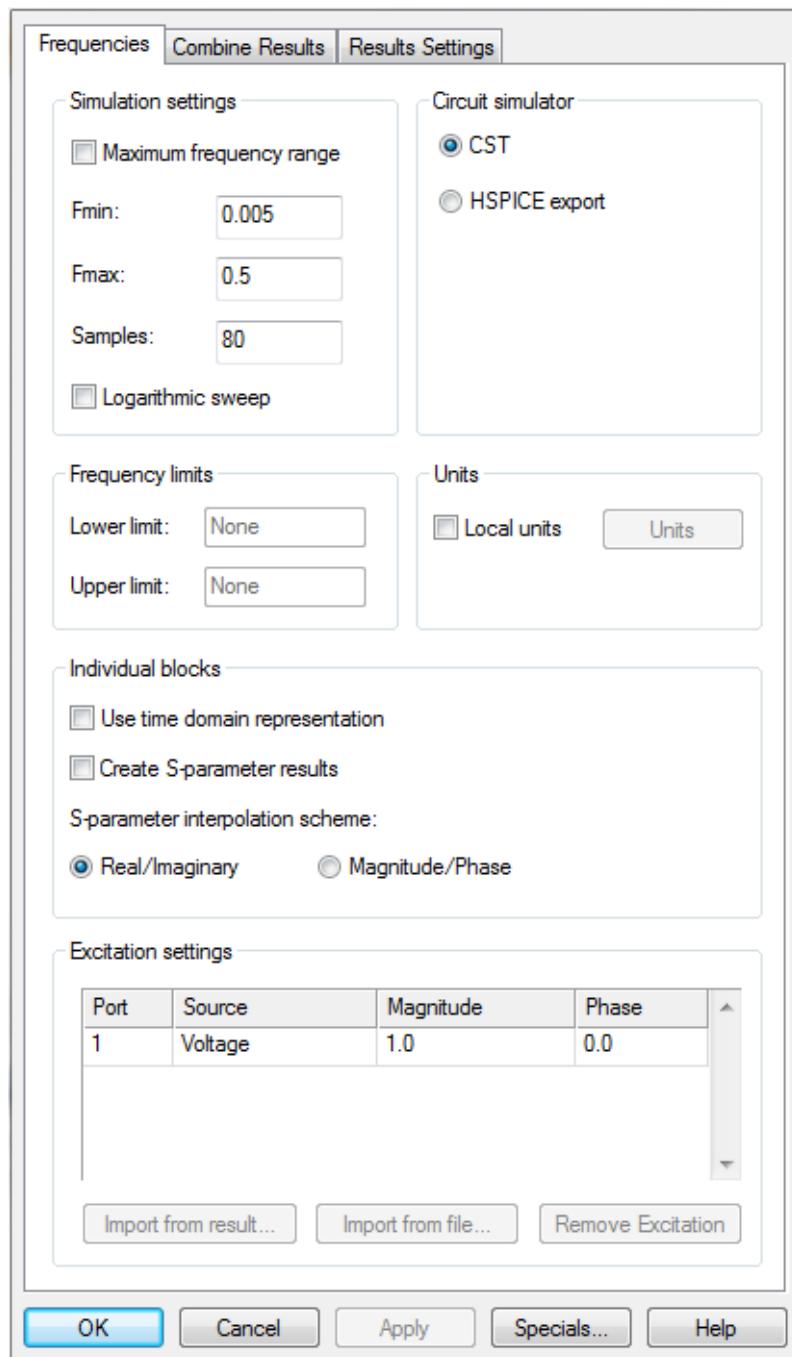
Next we have to define an AC-task by pressing *Home: Simulation* \Rightarrow *New Task*. A dialog box will appear where we select *AC/Combine results* as shown in the figure below:



After pressing *OK*, another dialog box will appear where we make the following settings inside the *Simulation settings* frame:



Before we can start the simulation we finally have to set an appropriate excitation. Therefore we click in column *Source* of Port 1 in the *Excitation settings* frame, select *Voltage* and leave the default values for *Magnitude* and *Phase*. The complete dialog box should now look like in the figure below:

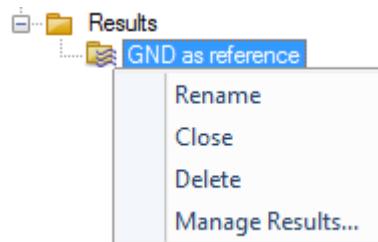


Now we select *Home: Simulation* \Rightarrow *Update* and start the simulation. First, the inductances and capacitances of the PEEC model will be calculated. In a second step, the actual circuit simulation will be started. The *Messages* window informs when the whole simulation task has been completed.

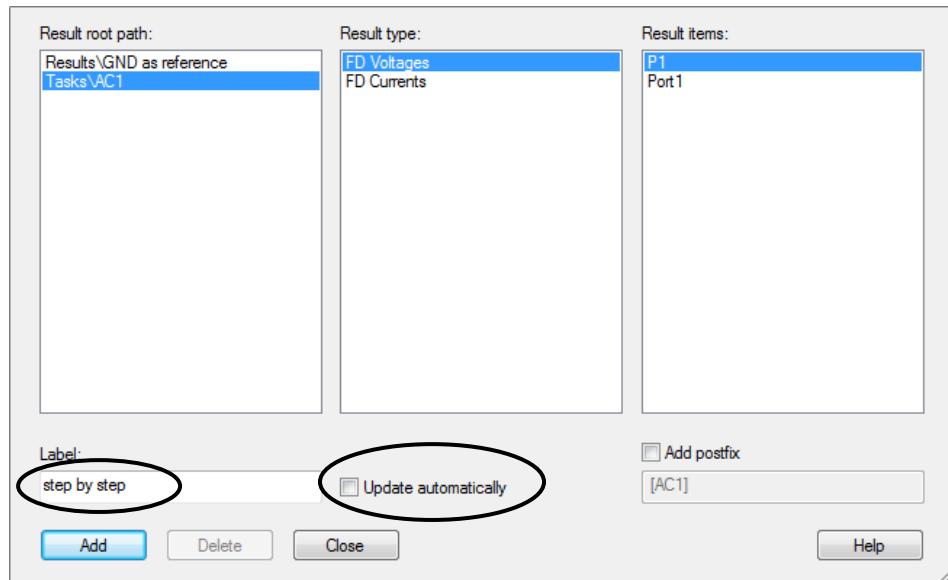
In order to display the result in an appropriate way, we go into the *Navigation Tree*, select folder *Results*, choose *Add Result Plot* (by using the right mouse button) and name the new result folder *GND as reference*:



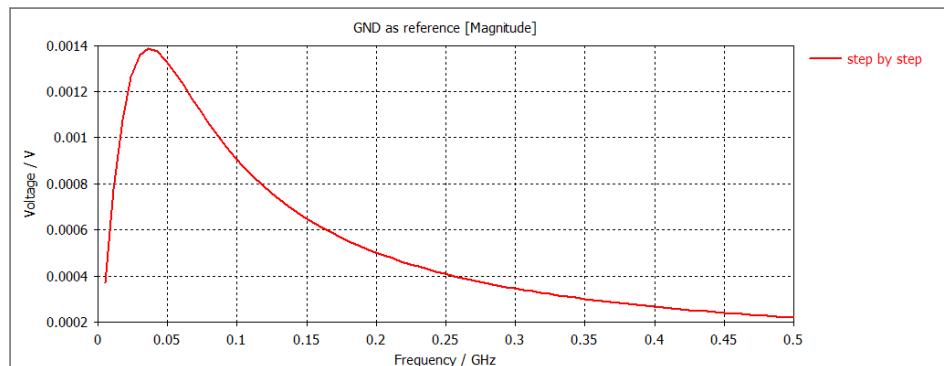
Next we select the folder and choose *Manage Results* (by using the right mouse button) as it can be seen in the figure below:



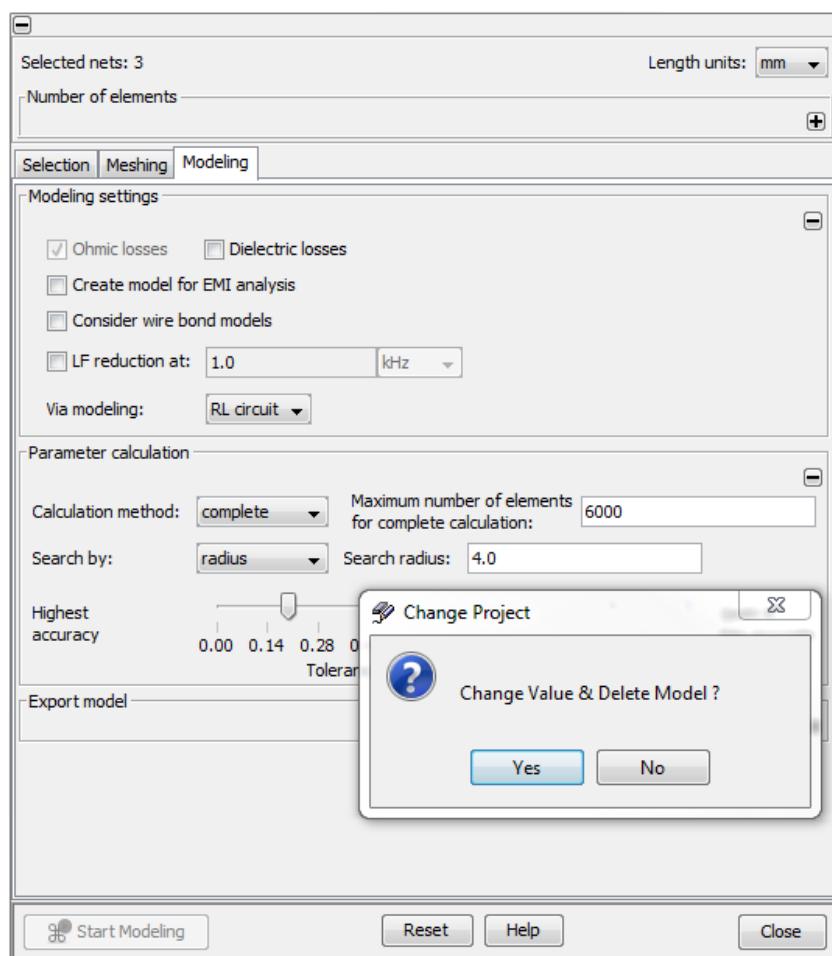
The following dialog box will appear. We enter name *step-by-step* in the field *Label* and uncheck the box *Update automatically*.



Then we press *Add*, close the dialog box and see the result in the separate tab:

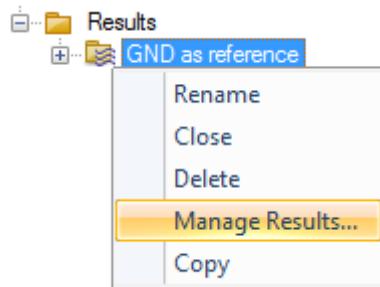


Now we generate another PEEC model using the calculation method *complete* instead of *step-by-step*. Therefore we change to the *PCB* tab and press *Home: Modeling* \Rightarrow *3D (PEEC)*:

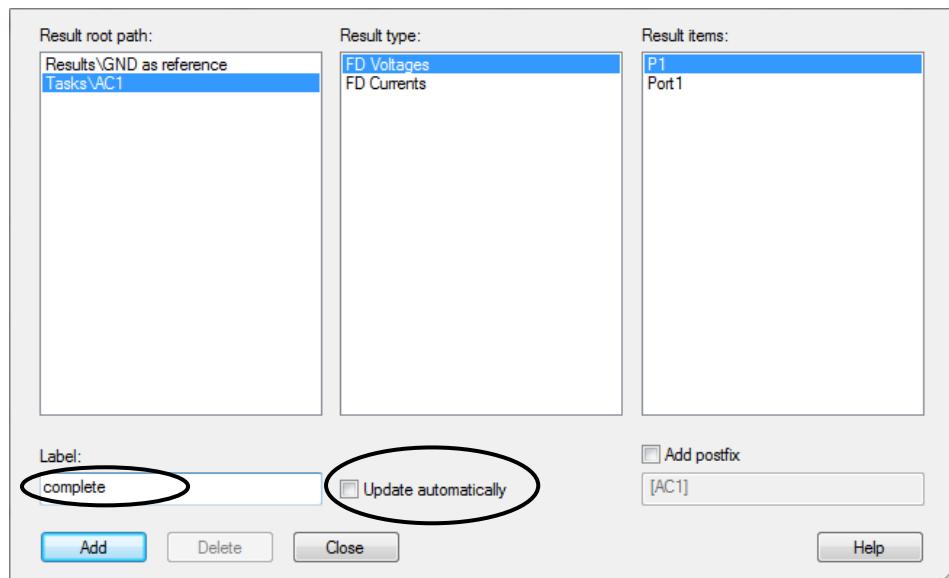


After we have selected *complete* as *Calculation Method* we are prompted to accept the value change and the fact that the old model will be deleted. We agree with Yes and afterwards press the *Start Modeling* button. The progress can be observed by looking at the information in the *Messages* window.

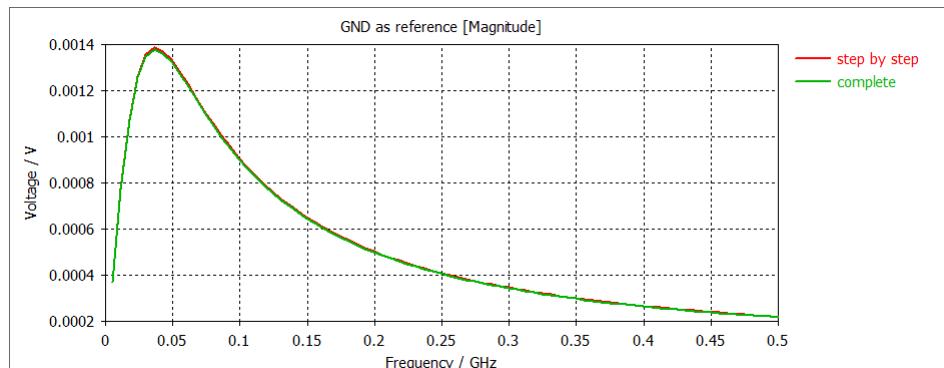
After completion we change to the *Schematic* tab and start the simulation again by simply pressing *Home: Simulation \Rightarrow Update*. The simulation will take just a few seconds longer than the previous one. In order to compare the new result with the existing, we select the Result folder *GND as reference* and choose *Manage Results* by using the right mouse button:



In the dialog box we enter the name *complete* in the *Label* field, uncheck the box *Update automatically*, press the button *Add* and finally click on *Close*:

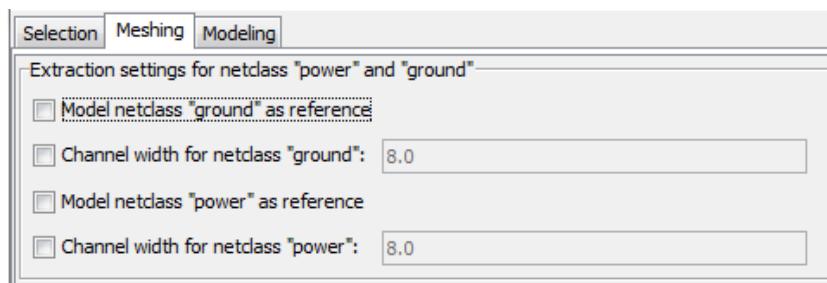


Now we see a second curve that is almost identical to the first:

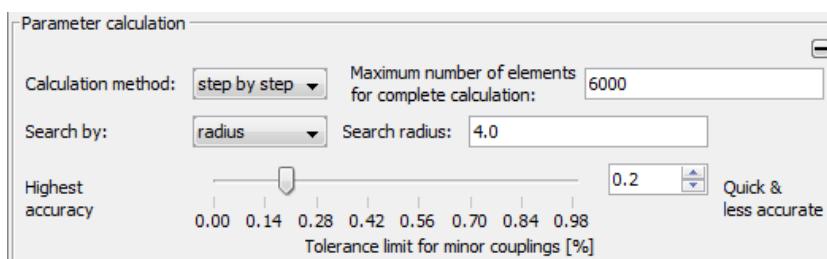


In order to see the effect of the cutout inside the net GND, we must consider the net GND as a normal net and not as a reference conductor. Therefore we change to the **PCB** tab and press *Home: Modeling* \Leftrightarrow **3D (PEEC)**.

Inside the dialog box we select the *Meshing* tab and uncheck the *Model netclass "ground" as reference* button. We will be prompted to accept the value change and we press Yes. The settings inside the *Extraction settings for netclass "power" and "ground"* frame should look like in the figure below:

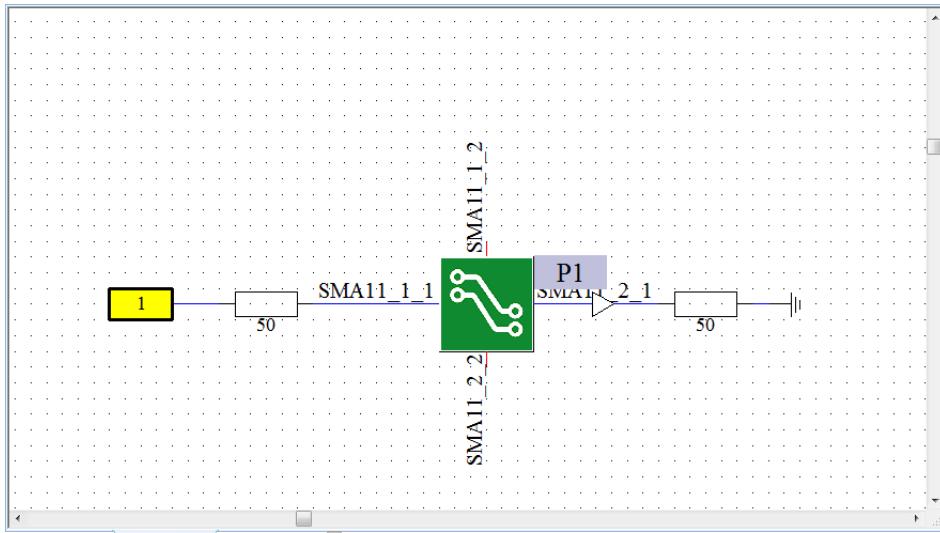


Next we select to the *Modeling* tab and change the *Calculation Method* back to *step-by-step* as shown in the figure below:



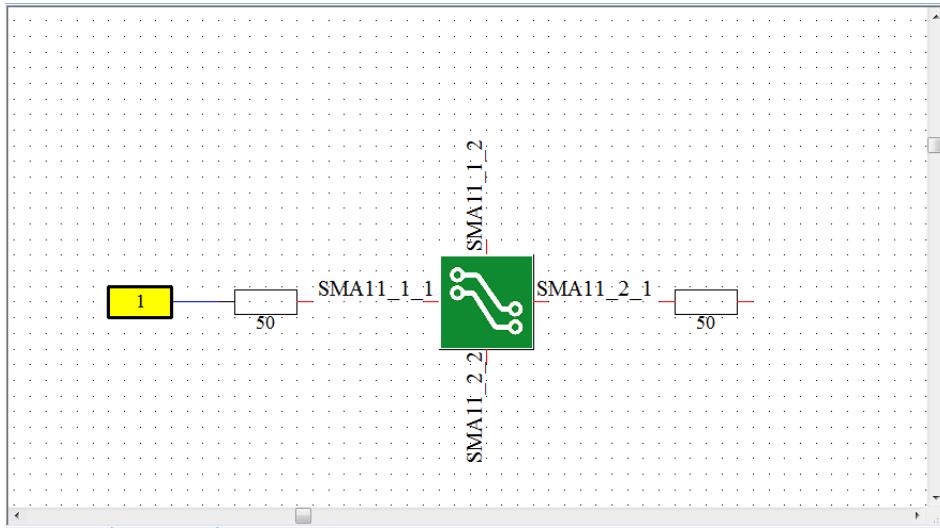
Again we press *Start Modeling* and see the information in the *Messages* window.

After changing to the Schematic tab we get an update of the PEEC model and it is obvious that this model consist of four pins – the two additional pins come from the *GND* net.

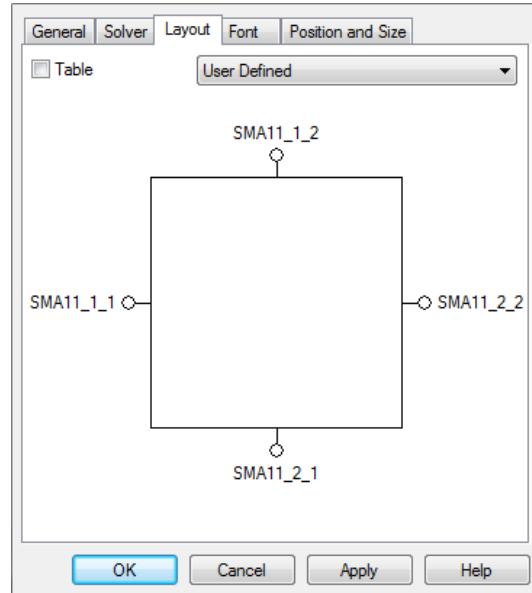


In order to load the PEEC model, we recommend removing the *ground symbols* and the electric connection lines from the schematic block by simply selecting them and choosing *Cut* (by using the right mouse button).

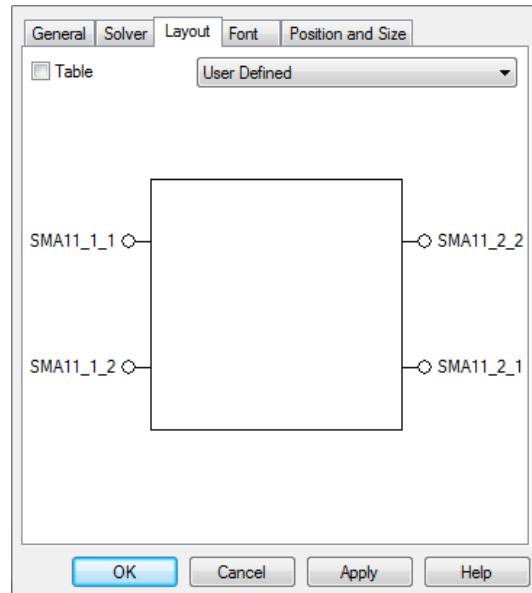
We start from the following schematic:



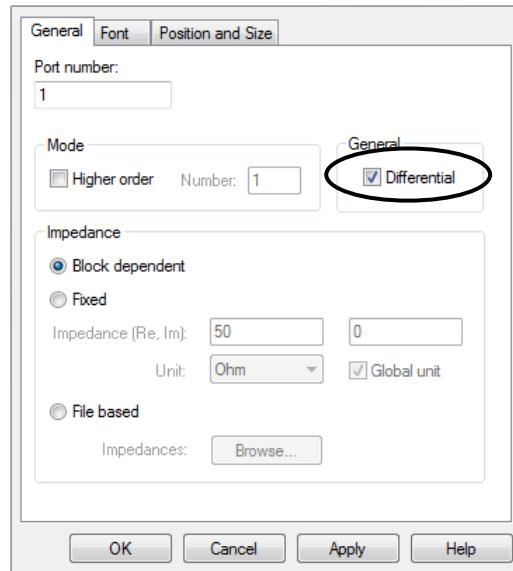
Next we re-arrange the pin positions. Therefore we double-click on the PEEC symbol and choose tab *Layout* in the dialog box:



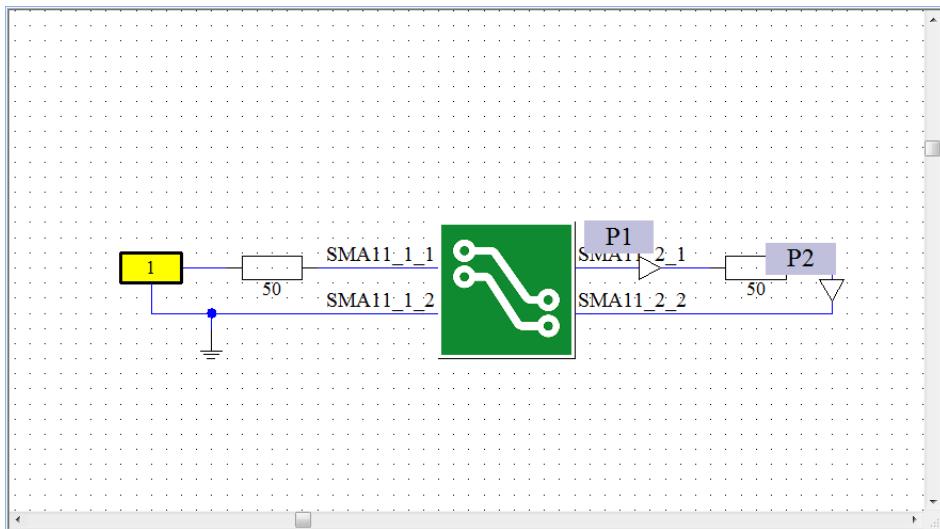
First we select pin *SMA11_2_2* and drag it from the bottom to the right side. Next we select pin *SMA11_1_2* and drag it from the top to the left side. The result is shown in the figure below:



After pressing *OK* we will have the re-arranged pin order on the PEEC symbol. Next we transform the port to a *differential* port. Therefore double-click on the port symbol. A dialog box will show up where we check *Differential* in the frame *General* as shown in the figure below:



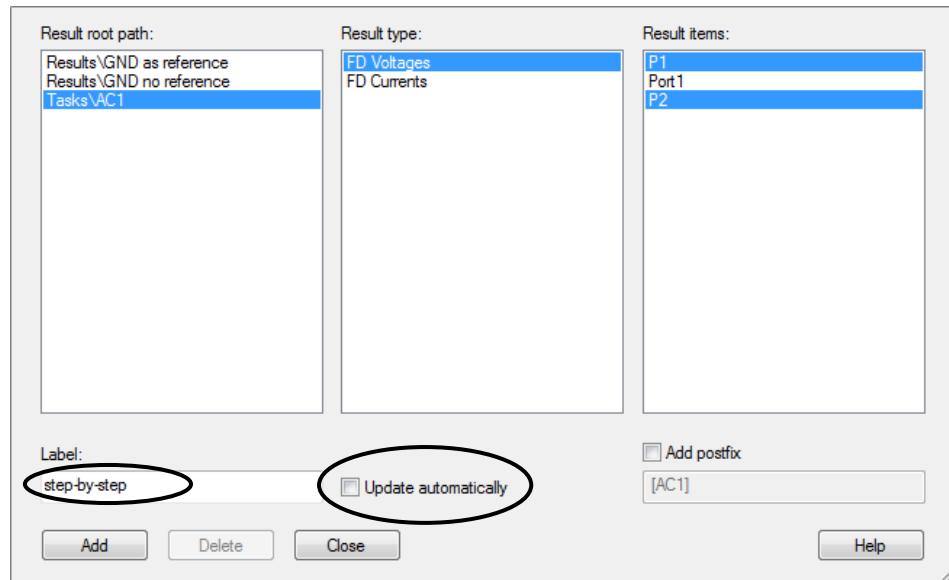
After pressing *OK* we will recognize an additional terminal on the yellow port and we are now able to complete the schematic as shown in the figure below:



Please do not forget to place the probes on both terminals on the right hand side as shown above.

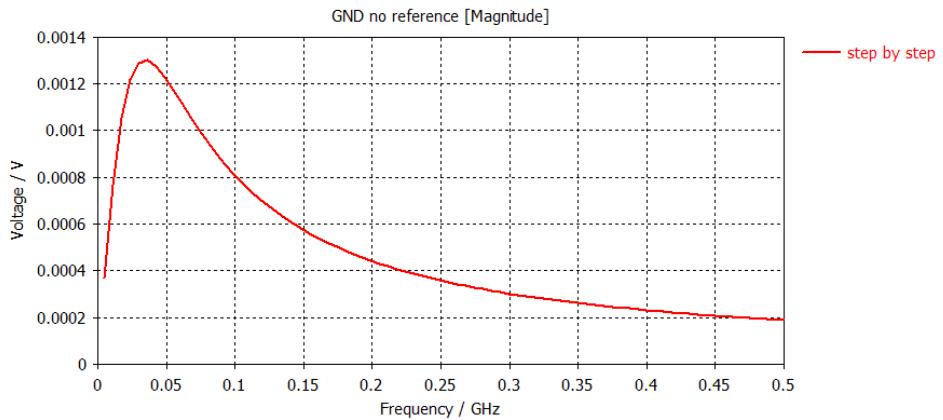
Next we run the simulation again by simply pressing *Home: Simulation* \Rightarrow *Update*. The simulation will take considerably longer than for the later ones.

In order to compare the new result to the existing results, we select the *Result* folder and choose *Add Result Plot* by clicking the right mouse button and name the new folder, *GND no reference*. Next we select this new folder and choose *Manage Results* by using the right mouse button. In the dialog box we first select the right result path in the left column, then enter the name *step-by-step* in the *Label* field and uncheck the box *Update automatically*:



Next we select both probes *P1* and *P2* (use *Ctrl*+left mouse button) in the right column, then press the *Add* button and finally *Close* the dialog box.

The following result will appear showing that the peak is a little bit smaller. In general, the result shows no significant influence from the cutout inside the net GND:



SI on a Multilayer using 2D Modeling

The purpose of this example is to acquaint you with the

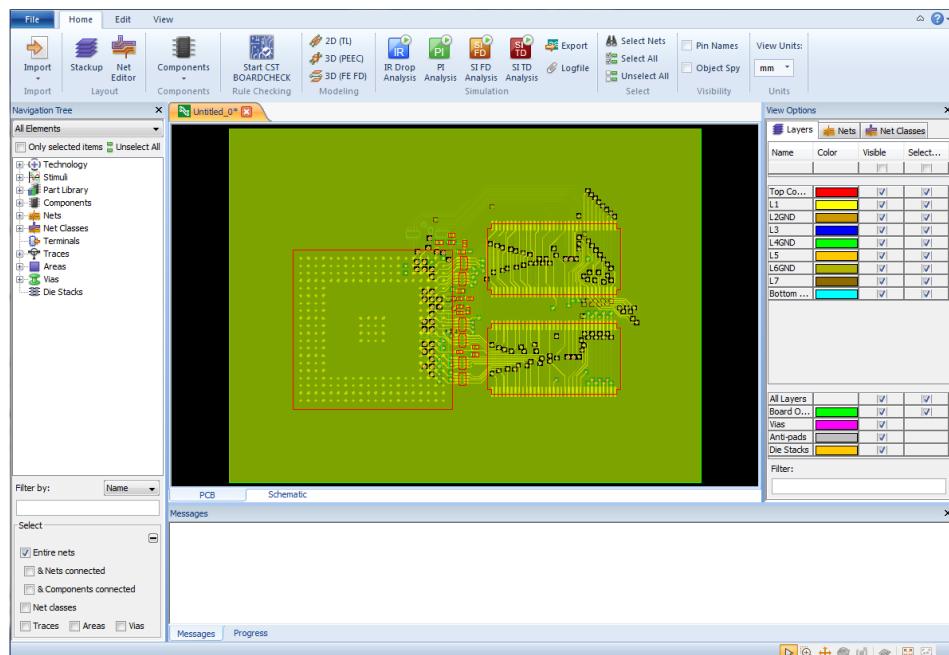
- Selection, Meshing and Modeling dialog for 2D Modeling.
- Component Library.
- Usage of the 2D model in the circuit simulator.
- Time domain analysis with focus on signal integrity.

Task Definition

In many high-speed PCB designs it is important to check the integrity of the signal paths. This means the whole system consisting of selected high-speed transmission lines, signal sources and loads has to be analyzed with respect to delay, over- and undershoot and crosstalk. For this kind of analysis the power delivery systems are normally regarded as ideal and the simulation is performed in the time domain. In this example we perform such an analysis on the basis of a single transmission line inside a PCB.

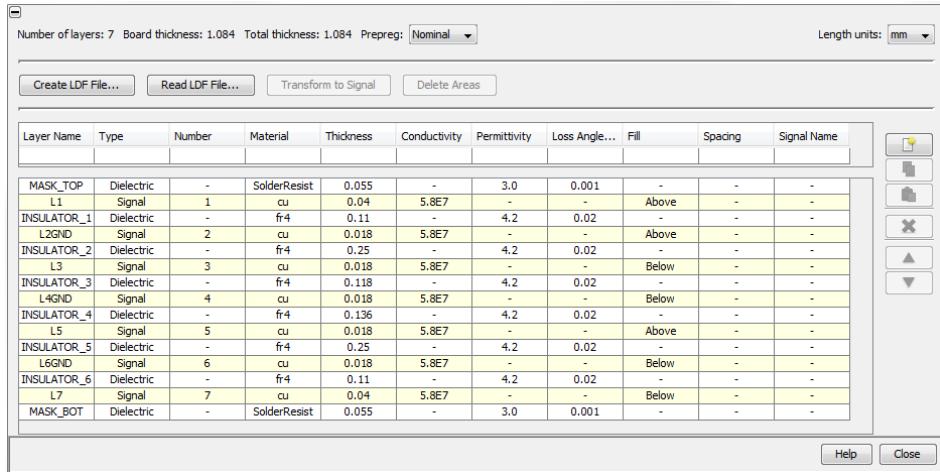
The PCB Design

First we create a new project by importing an existing PCB design. In the corresponding import dialog box we check *Simlab PCBMod* as *Import type* and navigate to the folder *Examples of the CST STUDIO SUITE installation directory* and select the file *high speed.dar* under the subfolder *PCBS/Signal Integrity*. The following design will appear:



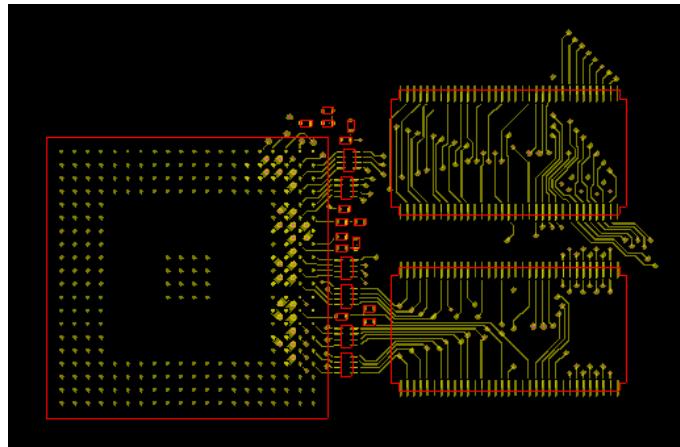
We save the project with name ‘signal integrity’.

Now we start to examine the design. We see a microcontroller on the left side that is connected with the two ASICS on the right side via an address bus. First we press *Home: Layout* \Rightarrow *Stackup* and change parameter *Prepreg* to value *Nominal*. We also note the particular sequence of *Above-* and *Below* values in the *Fill* column and refer to the CST PCB STUDIO online help for more details on the meaning of these parameters.

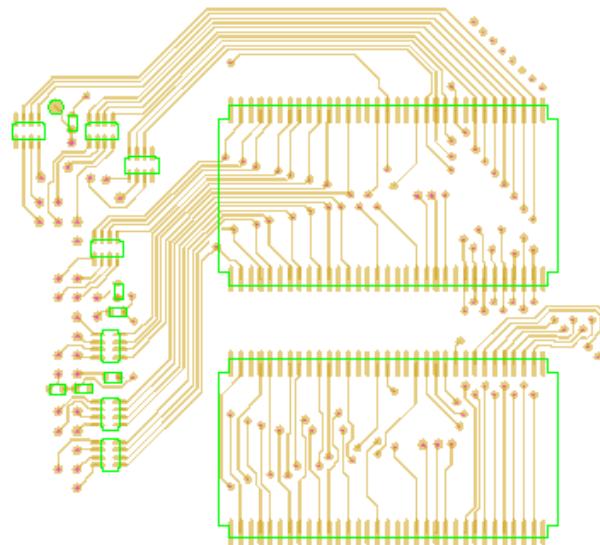


The board consists of seven metallic layers and has an overall thickness of about 1 mm. The material of the dielectric layers is *fr4* with a relative permittivity of 4.2.

Now let's have a closer look at the existing components of the board. We go to the *View Options* window and select the first two layers *Top Components* and *L1*. We see the microcontroller on the left side and two ASICS on the right side:

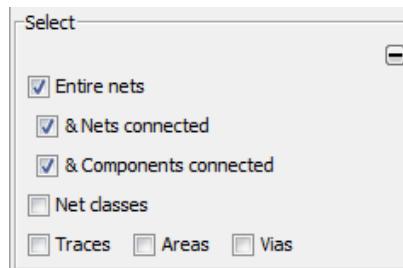


Now we select the last two layers *L7* and *Bottom Components*. We see another two ASICs on the bottom side. To make the nets better visible switch off the black background color by unchecking *View: Color \Rightarrow Black Background*:



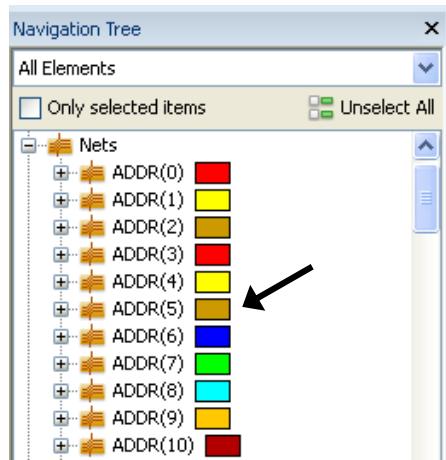
The address bus connects each signal from a pin of the microcontroller with the corresponding pins of the four ASICs.

We are interested in the transmission behavior of the net *ADDR(5)*. In order to select the net, we go into the *Navigation Tree*, expand the *Select* frame if need be and check the tree buttons: ‘*Entire Nets*’, ‘*& Nets Connected*’ and ‘*& Components Connected*’ as shown in the figure below:

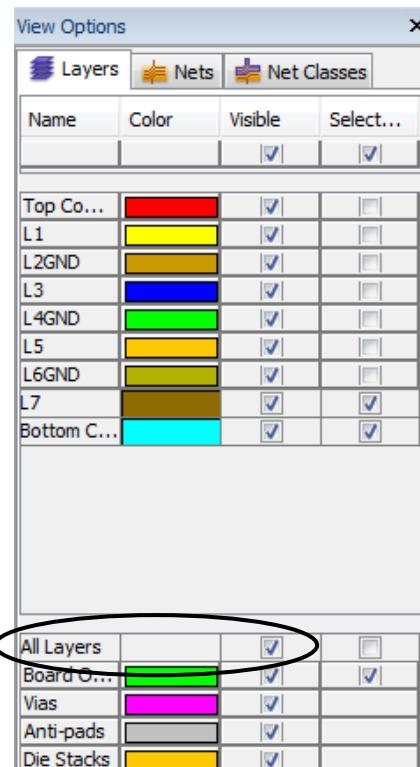


Checking the box ‘*&Nets Connected*’ means that all nets connected to a selected net (e.g. by a resistor) will be automatically selected, too. And checking the box ‘*& Components Connected*’ means that all components connected to any selected net (including the automatically selected nets) will be automatically selected. This is a powerful function as we will see now.

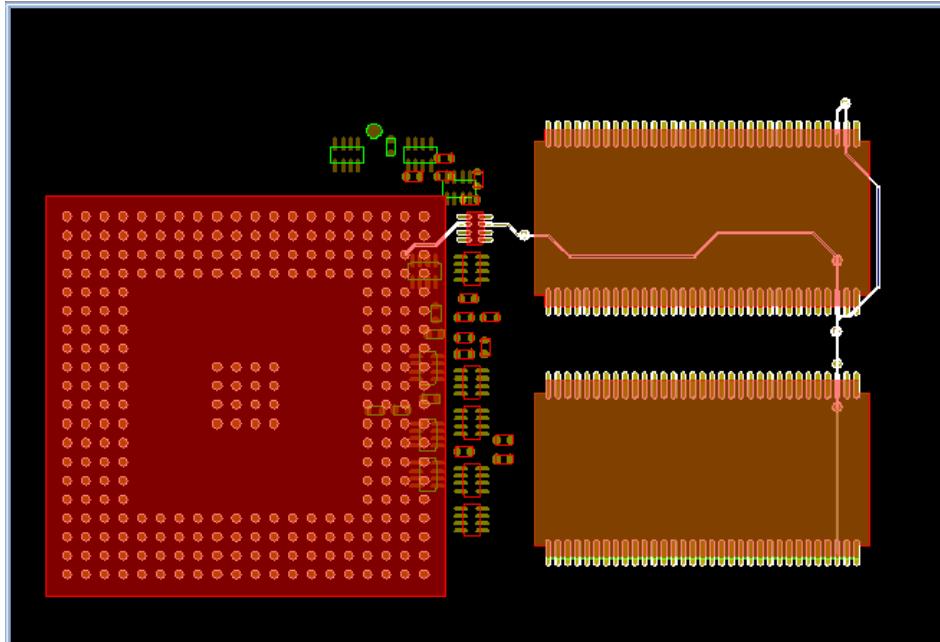
We go into the *Navigation Tree*, expand the *Nets* folder and scroll down until we see *ADDR(5)* as shown in the figure below:



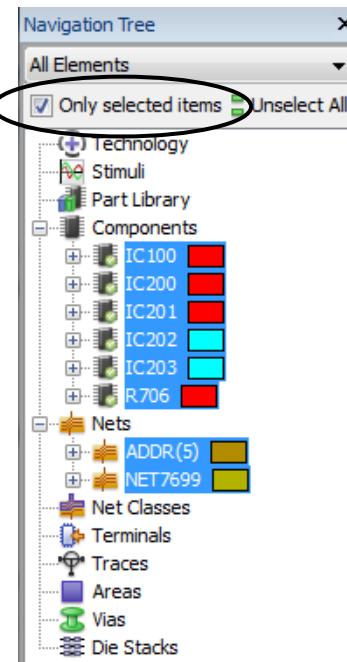
Now we select *ADDR(5)* and in addition, we press *View: Visibility \Rightarrow Hide Unselected Nets* to hide all unselected nets. Next we switch the black background color on again and go into the *View Options* window. Here, we select *All Layers* in order to make all layers visible as shown in the figure below:



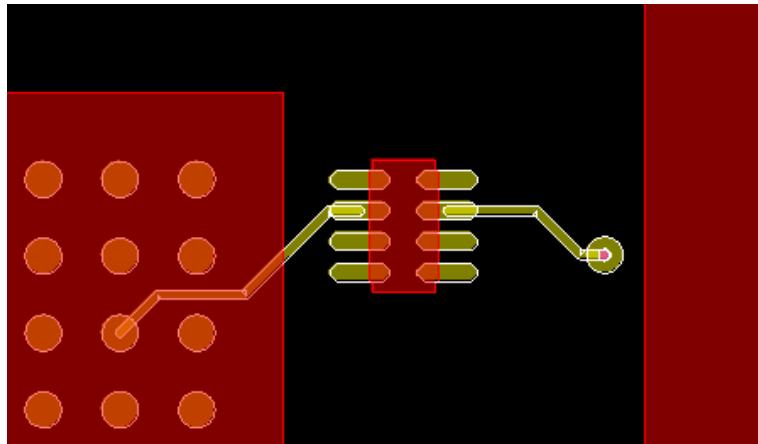
Afterwards we go into the Main View and zoom in a little bit. We should now have a view similar to the one shown in the figure below:



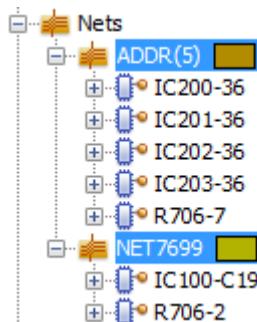
We see the selected net is highlighted with an additional net on the left side, both just separated by a resistor array. Go back into the *Navigation Tree* and check *Only Selected Items*. The two selected nets and the six components will be listed:



Next we go into the *View Options* window and select the two upper layers *Top Components* and L1 only. We zoom into the region of the resistor array and should have a similar view (the view can be slightly different depending on the chosen viewer, default or legacy):

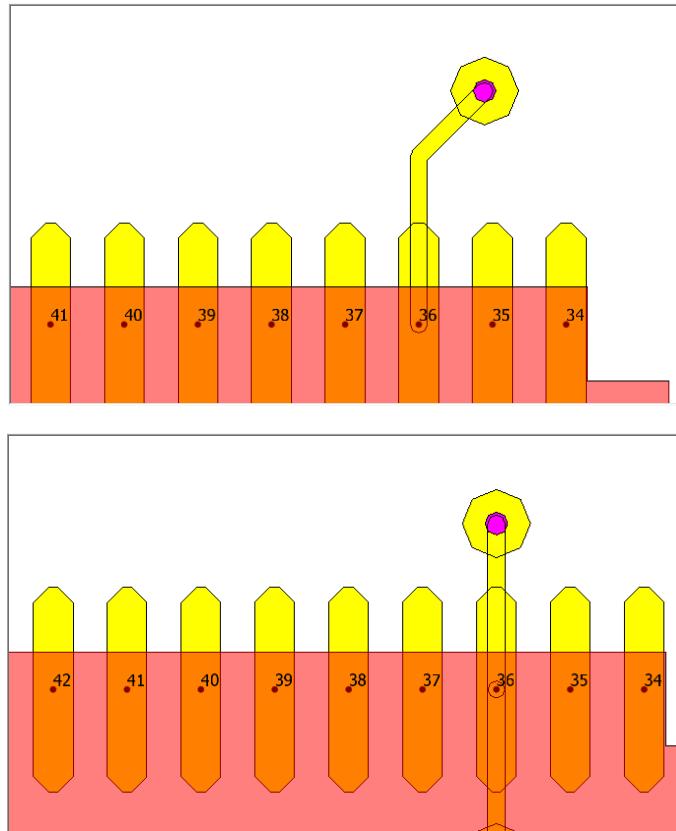


Next we take a closer look at the signal path of the selected nets. In order to do this, it is convenient to expand the selected nets inside the *Navigation Tree* as shown in the figure below:



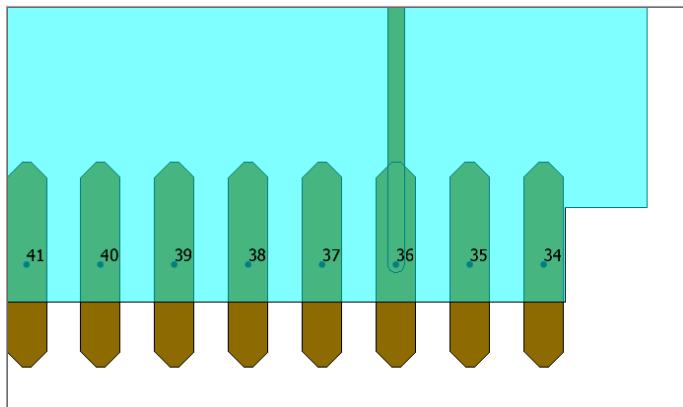
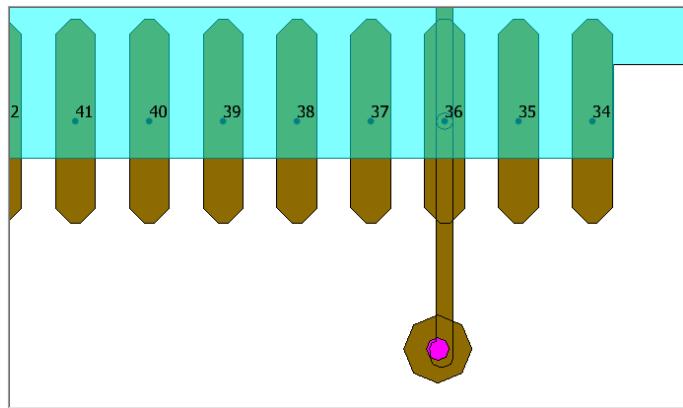
Now we can easily follow the signal path starting from pin *IC100-C19* of the microcontroller to pin *R706-2* of the resistor array. The resistor array includes 33 Ohm resistors and connects the signal to pin *R706-7*. From this pin the net *ADDR(5)* starts and connects the pins to the four ASICs.

To show the location of these pins we first zoom out again (by pressing *View: Change View* \Rightarrow *Reset View*). Then we zoom in on the ASICs on the right side and switch on the pin names (by pressing *View: Visibility* \Rightarrow *Pin Names*). The figures below show some pins of *IC201* and *IC200* in the inverse view (the view can be slightly different depending on the chosen viewer, default or legacy):



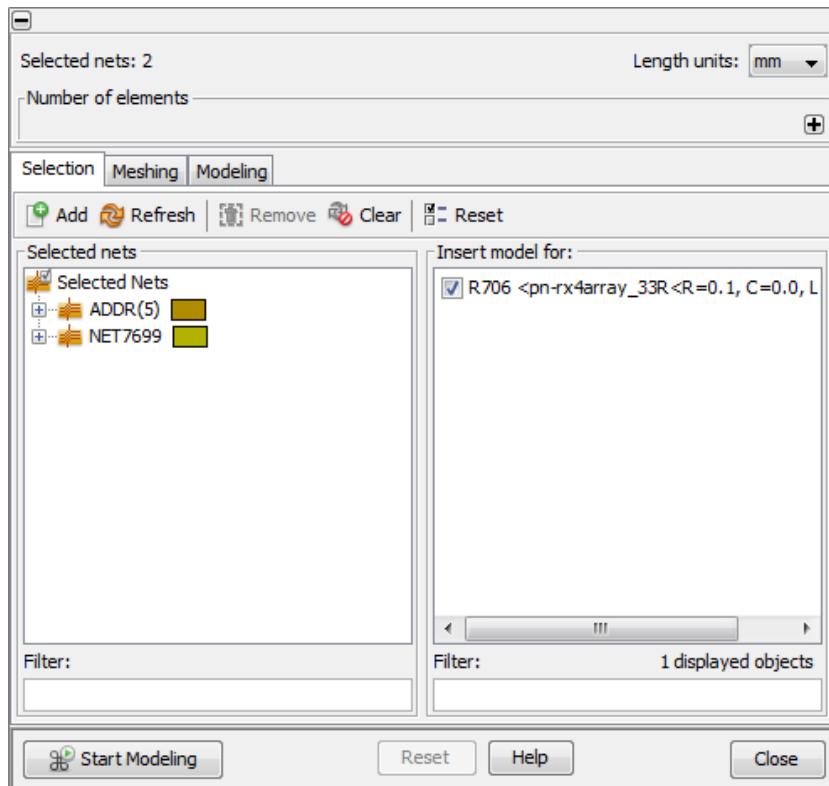
Again we change to the *View Options* window and select the two bottom layers *L7* and *Bottom Components*.

We zoom into the corresponding regions and recognize pin *IC203-36* and *IC202-36*:

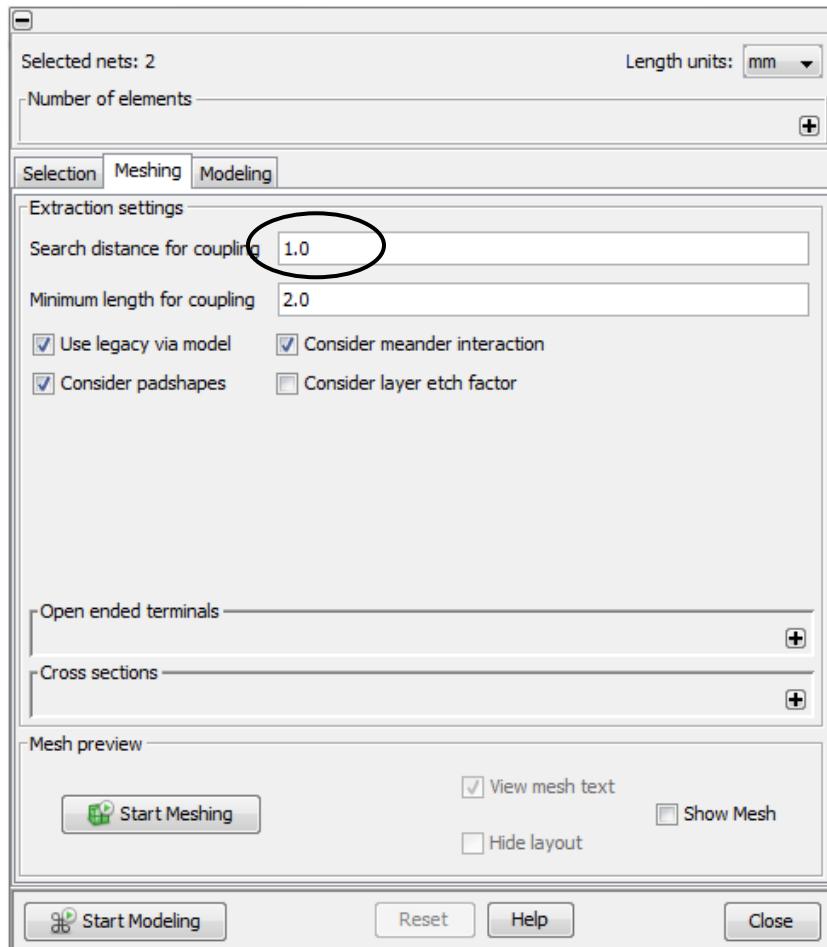


Meshing and Modeling

To start with meshing, we first uncheck *View: Visibility* \Rightarrow *Pin Names* to hide the pin names again. Then we press *Home: Modeling* \Rightarrow *2D (TL)*. In the following dialog we choose the *Selection* tab and press the *Add* button to include the selected nets:

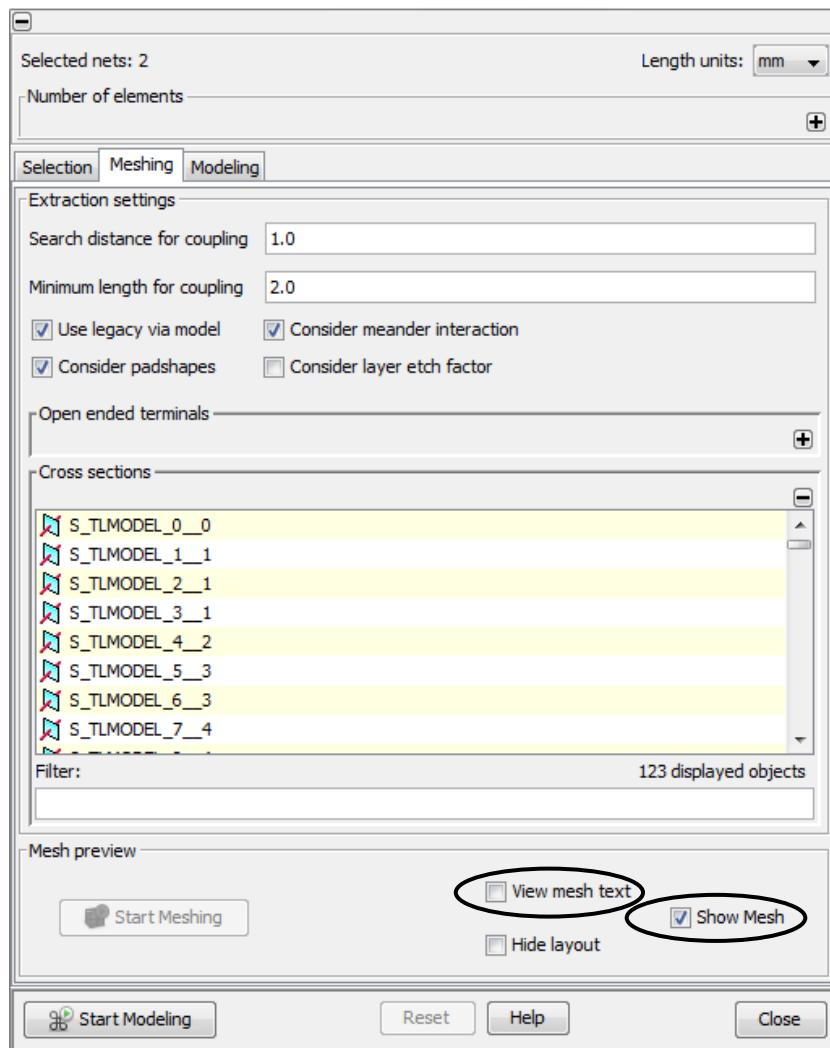


Next we change to the *Meshing* tab and see the following dialog box:



In the *Extraction Settings* frame we see two fields, namely *Search distance for coupling* and *Minimum length for coupling*. The first value controls how much space the meshing algorithm adds around the selected traces for the calculation of the transmission line parameters. In our case we want to have a short modeling phase and therefore we change the value to 1 mm. The second parameter defines a specific length: the traces in a cross-section will be only coupled (within the given range from the first parameter), if its length exceeds the *Minimum length for coupling*. Here we leave the default value.

We make sure that the parameter *Use legacy via model* is activated and press the *Start Meshing* button. Almost immediately the meshing will be completed as you can see in the *Messages* window. We go into the dialog box again and expand the *Cross sections* frame as shown in the figure below:

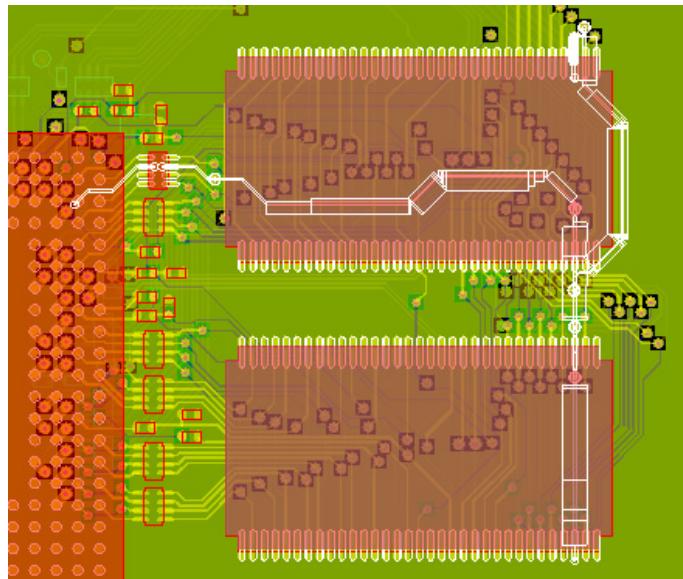


A list of cross-section segments appears. We uncheck the *View mesh text* box as shown in the figure above.

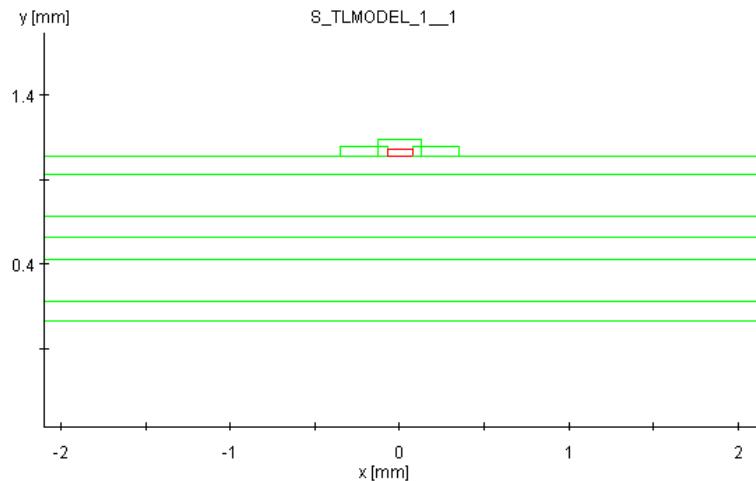
Note: the following feature is only available with the legacy viewer.

In order to display the generated cross-sections in the layout, the *Show Mesh* button has to be activated (see figure above). But before pressing the button, you are recommended to do the following steps: First, go into the *View Options* window and select *All Layers*. Second, uncheck *Hide Unselected Nets* (*View: Visibility* \Rightarrow *Hide Unselected Nets*) and confirm *Black Background* color (*View: Color* \Rightarrow *Black Background*). Lastly, uncheck *Only selected items* at the top of the Navigation Tree.

After appropriate view zooming we get the following view on the highlighted cross-section segments:

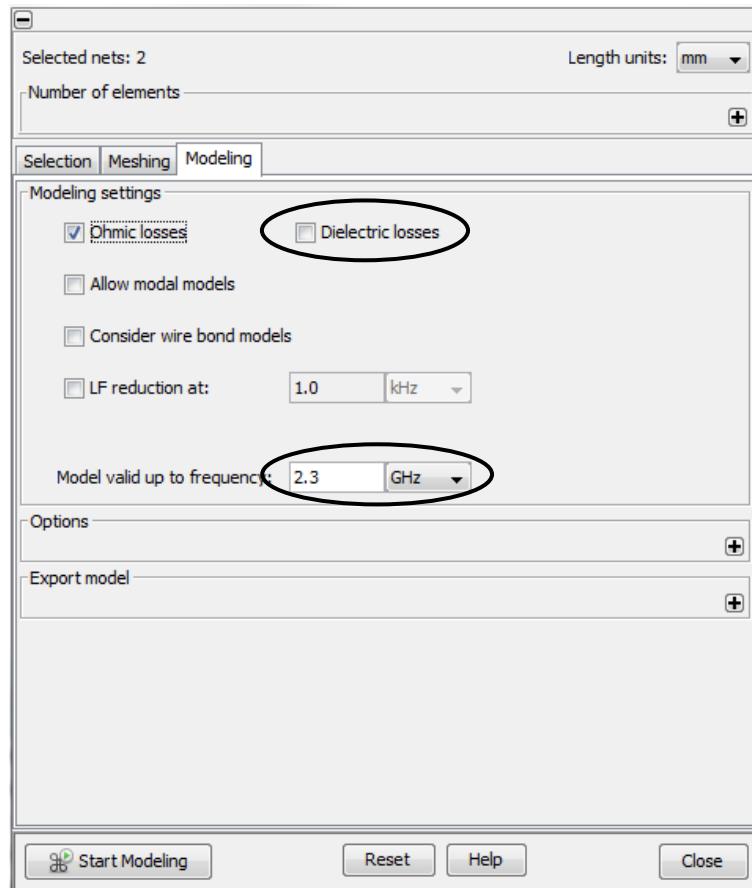


If we double-click on the second item “S_TLMODEL_1__1” in the cross-section list, a new window will appear showing the geometric dimensions of the corresponding cross-section:



Now we step through the cross-sections and watch both windows: the *Main View* and the separate *Cross Section View* window. We will notice that in both windows the corresponding segment is highlighted.

Next we change to *Modeling* tab where the following dialog box appears:

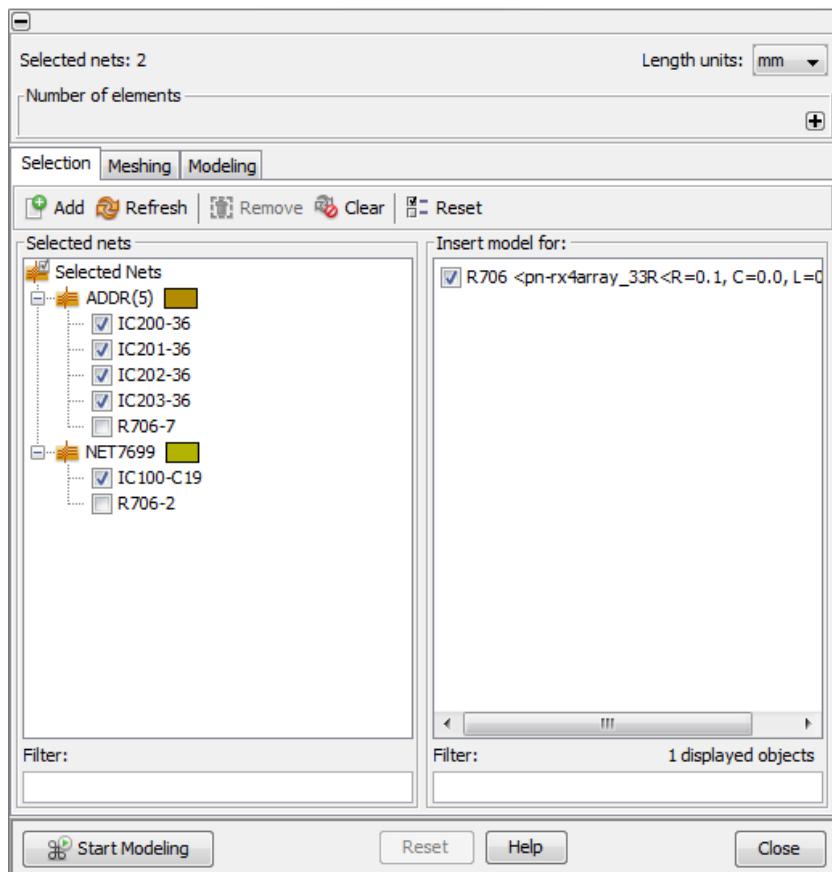


In the *Modeling settings* frame we leave the settings for *Ohmic losses* and deactivate the setting for *Dielectric losses*. *Allow modal models* is a special function useful for signal nets which are electrical long (a transmission line is electrical long when its length is several times over the minimal wave length of the signal that is transmitted on it). We uncheck this box.

An important setting is the maximum frequency up to which the model should be valid. We set the value of *Model valid up to frequency* to 2.3 GHz. Generally, we recommend setting the valid frequency range as high as it is needed for an application. This is due to two reasons. First, the maximum frequency range affects the complexity of the equivalent circuit - the higher the frequency the more complex the circuit is.

Secondly, every configuration has its own natural frequency limit and above this limit a model can't be produced because of the modeling method. The limiting factor is the cross sectional size – the bigger the size, the lower the maximum possible frequency range. After the modeling the program reports the maximum achievable frequency.

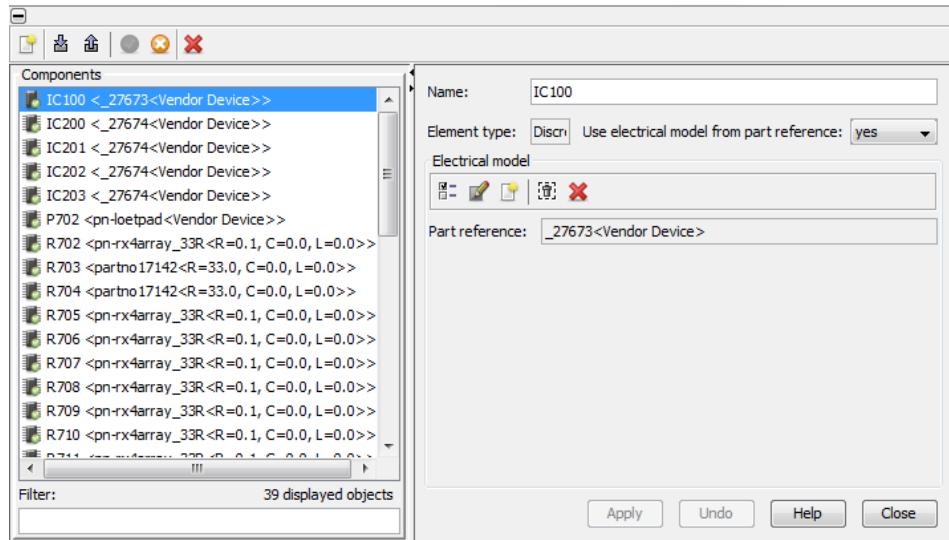
By default, the program will insert behavior models of those components which separate different nets listed inside the *Selection* tab. In addition, the pins of those components do not appear on the schematic block by default. In order to see these settings we change back to the *Selection* tab:



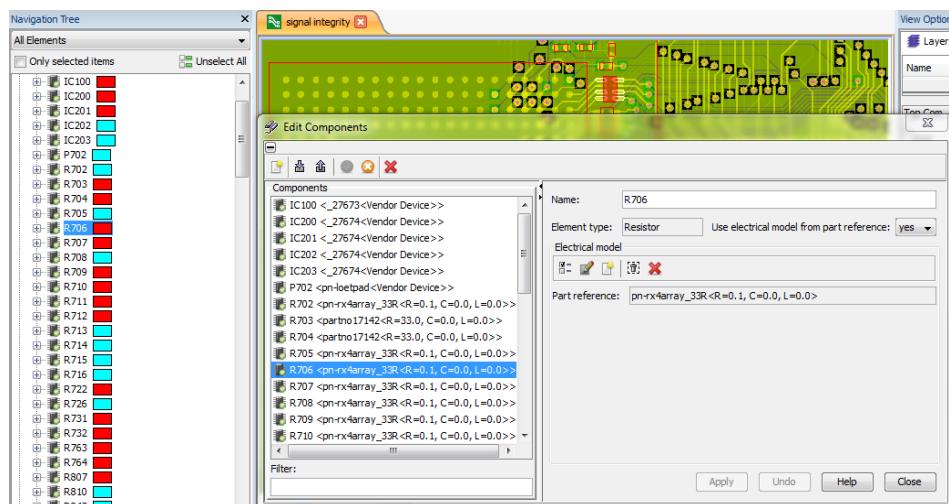
In the right column we see the checked component *R706*. It is the resistor array that connects the two nets *ADDR(5)* and *NET7699* which are listed in the left column. The two pins *R706-7* and *R706-2* are unchecked by default, since the program won't display these pins on the schematic block. This is a powerful feature and prevents the schematic block from having more terminals than is necessary.

In order to enable the insertion of the “inner” components, the right behavior models have to be assigned first. Therefore we close the current dialog box and have a look at how components are handled by selecting *Home: Components* \Rightarrow *Components*.

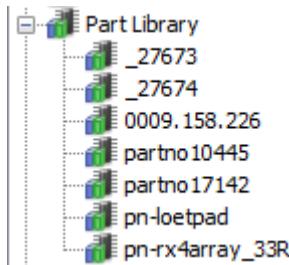
The following dialog box will arise presenting the *Component Library*:



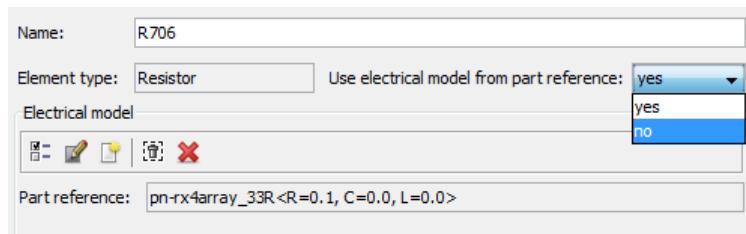
In the left column we see a list of all components placed on the PCB. The first five components are the ICs we already know. The rest are single resistors or resistor arrays. We select R706 and see that the component is highlighted in both, the *Navigation Tree* and the *Main View*:



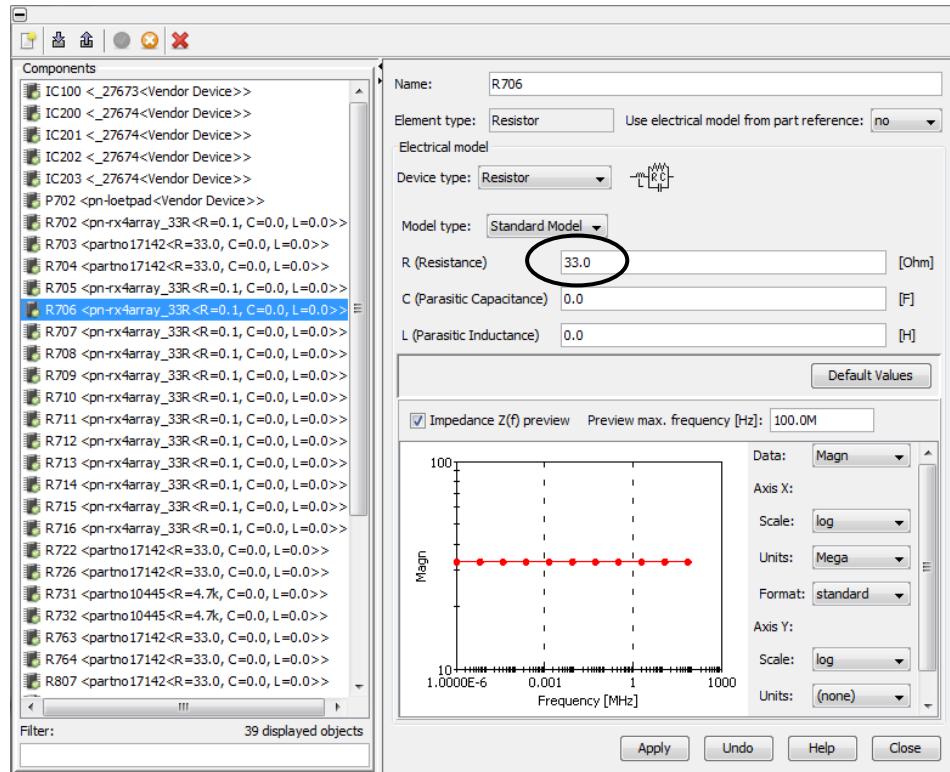
On the right side of the dialog box we see that *R706* references the part *pn-rsx4array_33R* which is stored inside the *Part Library* (see the last item in the figure below):



We don't want to use the behavior model from this part reference and decide to define a separate, local model to *R706*. Therefore we change the *Use electrical model from part reference* to 'no' as shown in the figure below:



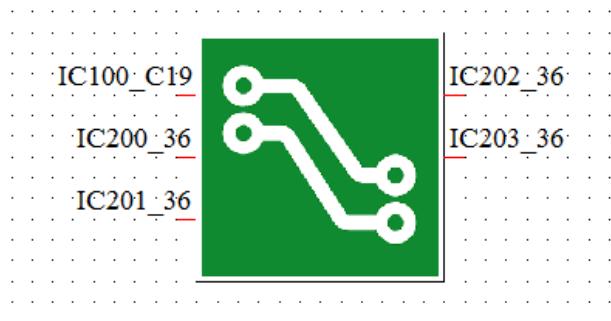
The right column of the dialog box changes and we see the standard model type of a resistor with a resistance of 0.1 Ohm and no parasitic capacitance and inductance:



Right beside the field *Device type* the corresponding general circuit topology is shown. We change the resistor value to 33 Ohm , press *<Return>* and then *Apply*.

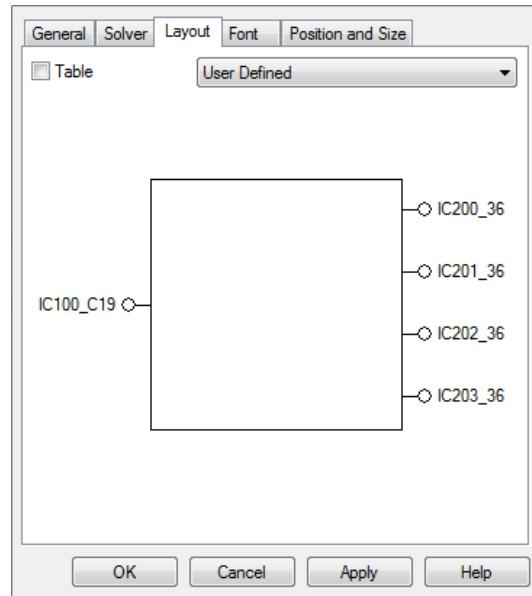
Now the right model of the resistor is assigned and we can continue with the example. Therefore we change back to the *2D (TL) Modeling* dialog, press the *Start Modeling* button and watch the information in the *Messages* window. The whole Modeling process will take a few seconds.

After the Modeling process has finished, we close the *2D (TL) Modeling* dialog box and change to the *Schematic* tab:

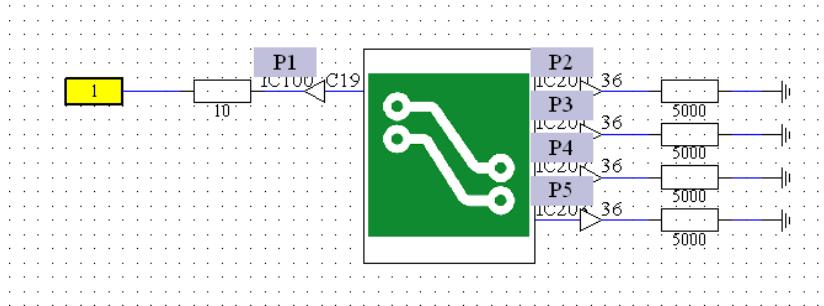


We see the end-terminals of the ICs but no additional pins from the internal component *R706*. Obviously the corresponding resistor model has been built into the circuit automatically.

We now start with a re-arrangement of the pins in order to have the pins of the four ASICS at the right hand side of the schematic block as shown in the figure below:

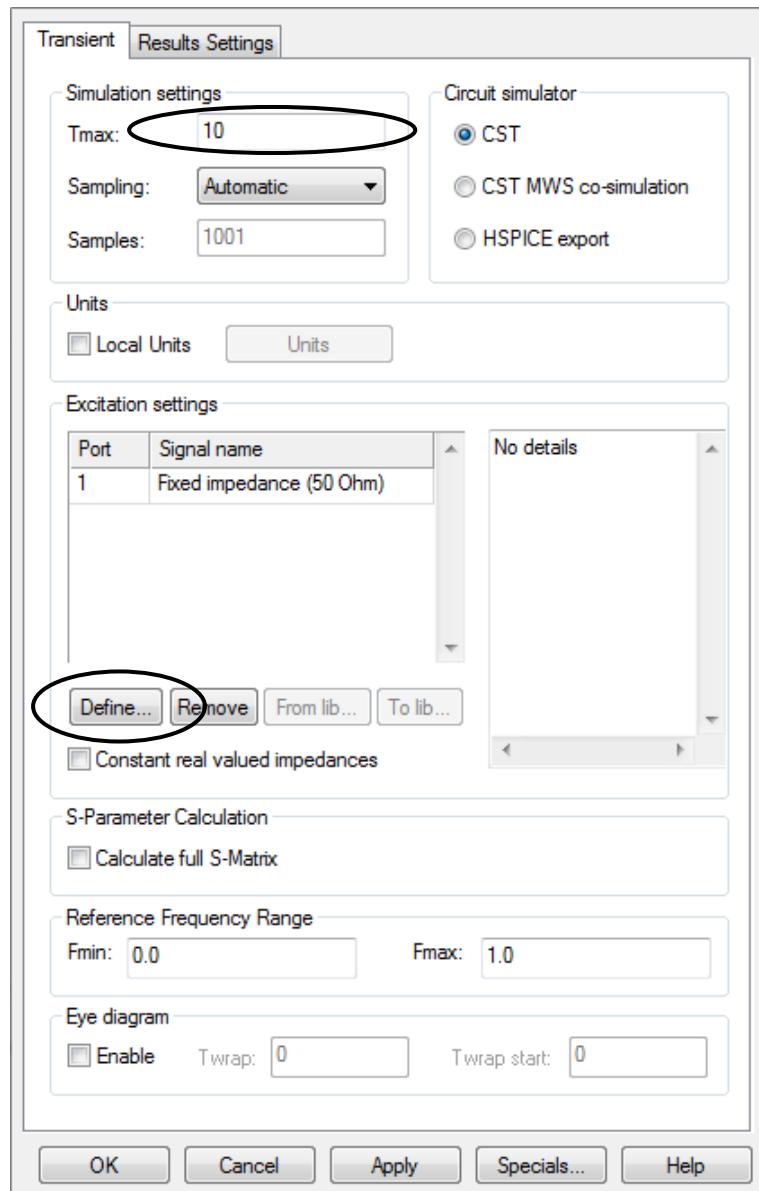


We press **OK** and load the schematic block as it is shown in the figure below:



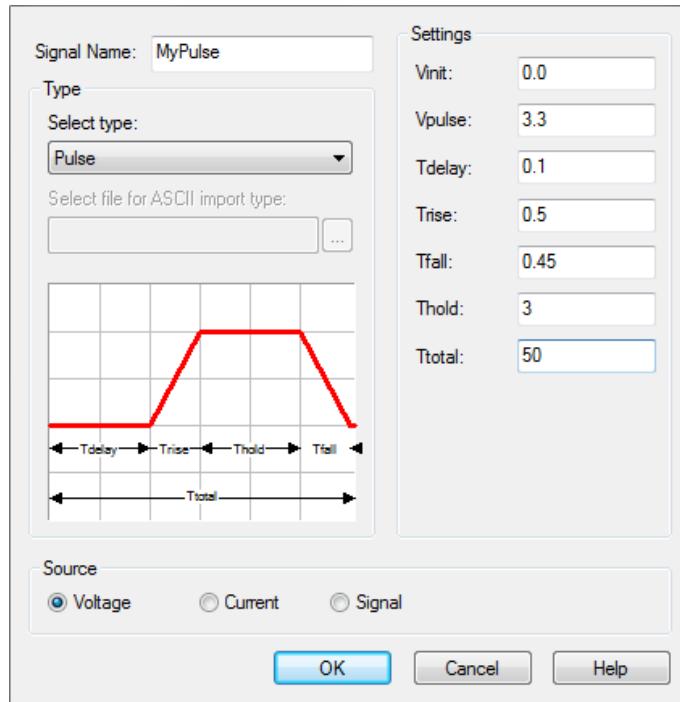
Note: Don't forget to place the probes!

Next we define a new transient task by opening the corresponding dialog box via *Home: Simulation \Rightarrow New Task \Rightarrow Transient Task*:

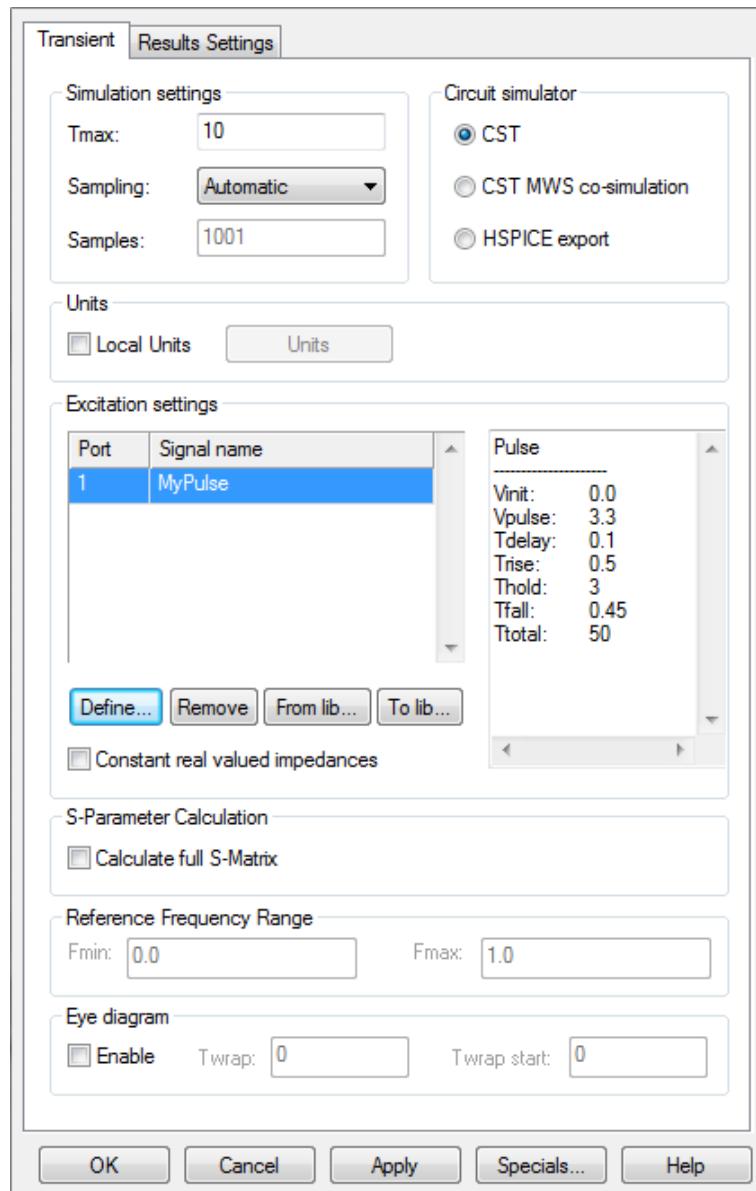


We first enter 10 (ns) in the *Tmax* field. Next we select *Port 1* in the *Excitation settings* frame and press *Define*.

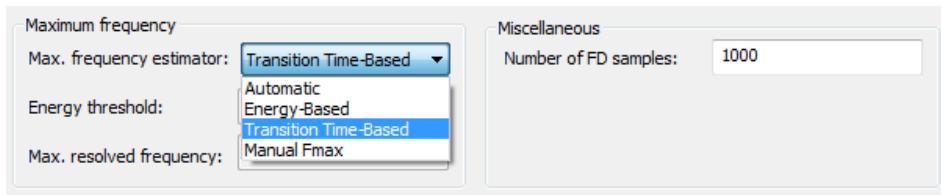
A new dialog box will appear where we set the parameters according to the figure below:



After pressing *OK* the dialog box for the transient task should now look like in the next figure:

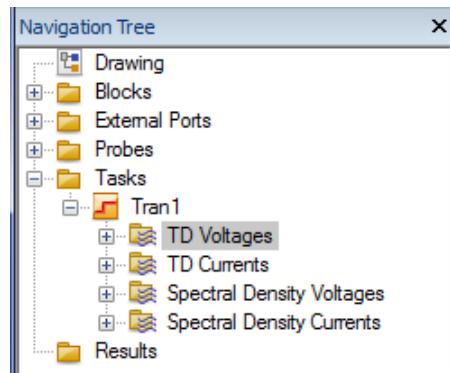


Lastly we press the **Specials** button at the bottom of the dialog box and change the value of the *Maximum frequency estimator* to *Transition Time-Based* as shown in the figure below:

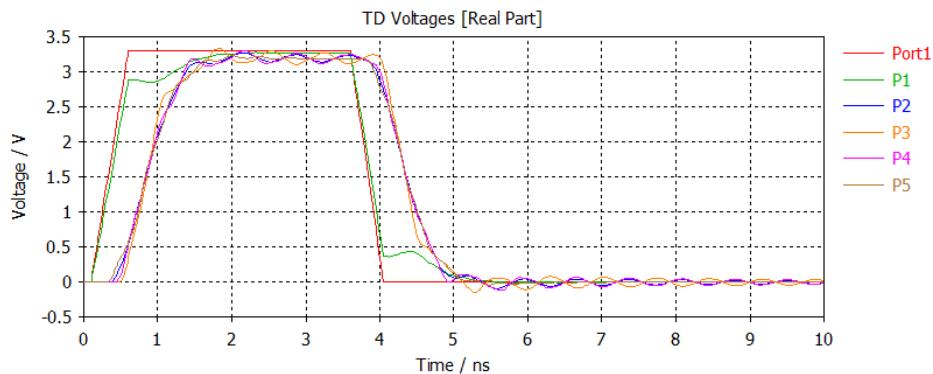


Now we press *OK* and start the simulation by pressing *Home: Simulation \Rightarrow Update*. First the transmission line parameter of the structure will be calculated by the 2D field solver and this will take some time. Afterwards the transient simulation will be started automatically.

To see all results, we go into the *Navigation Tree* and select *TD Voltages* inside the *Tran1* folder as shown in the figure below:



The results should look like in the figure below:



Now we have finished the signal integrity analysis of a simple net. If you now added a second net, e.g. net *ADDR(6)*, you could also check the crosstalk effects from one net to the other. You are recommended trying this additional step by yourself.

Note: for further explanations how to use CST PCB STUDIO for more complex *signal integrity (SI)* tasks please refer to the online documentation of CST PCB STUDIO.

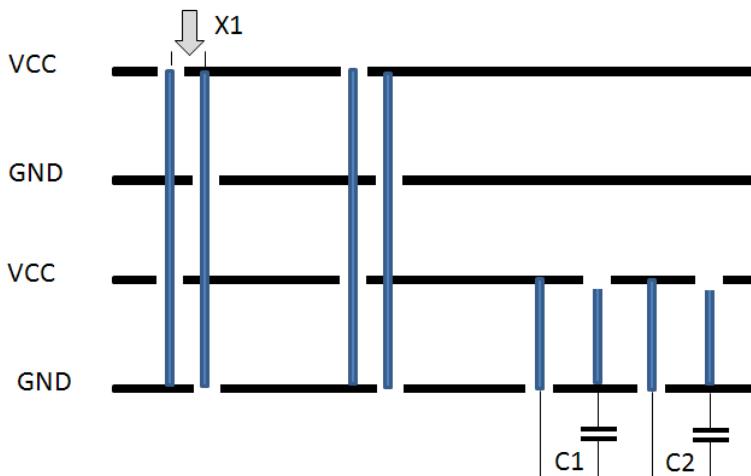
PI Analysis using the FE/FD-solver

The purpose of this example is to acquaint you with the

- Component Library
- Selection, and Modeling dialog for the 3DFEFD solver
- Impedance analysis with focus on power integrity

Task Definition

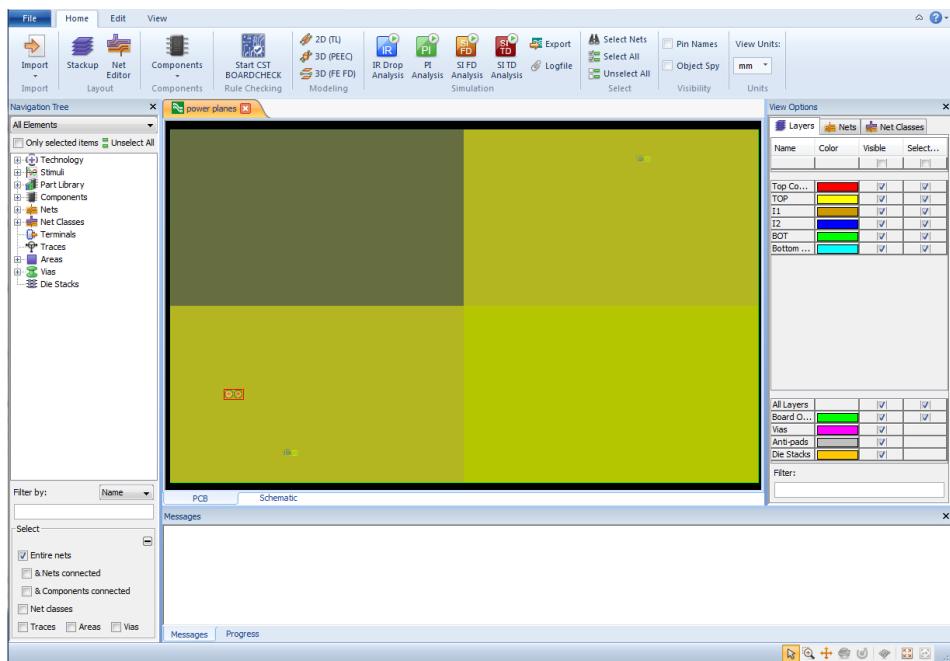
In this chapter we want to investigate the impedance of a power delivery network (PDN). It consists of four metallic layers (two GND, two VCC). The GND layers are connected to each other through vias, and similarly, the VCC layers are connected to each other through vias as shown in the figure below:



The lower VCC- and GND-layers are loaded with two decoupling capacitors C_1 and C_2 , which are placed at the bottom side of the board. In addition, the top side of the left via pair is loaded at X_1 , drawing power from both the VCC- and GND layers. We are interested in the impedance that is seen from X_1 .

The PCB Structure

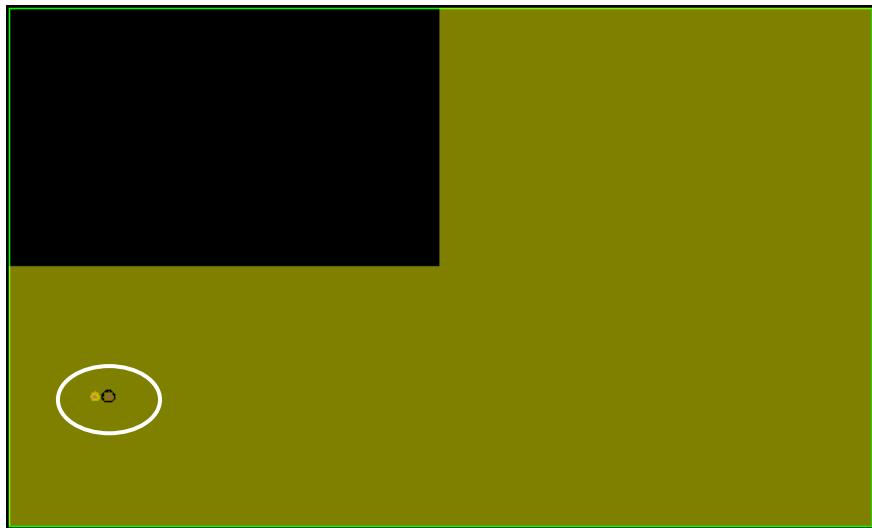
First we create a new project by importing an existing PCB design. In the corresponding import dialog box we check *Simlab PCBMod* as *Import type* and use the file browser to navigate to the folder *Examples* of your *CST STUDIO SUITE* installation directory and select the file *power delivery system.dar* under the subfolder *PCBS/Power Integrity*. The following design will appear:



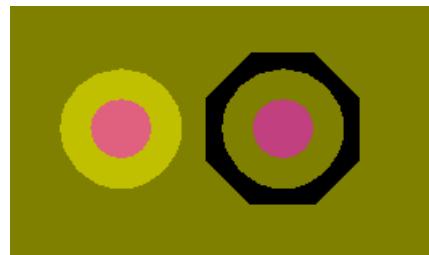
We save the project with name '**power planes**' and then start to examine the design.

On the left lower side of the PCB we see the red image of component *X1*. It provides the port where we want to analyze the impedance. We go inside the *View Options* window and select layer *TOP*.

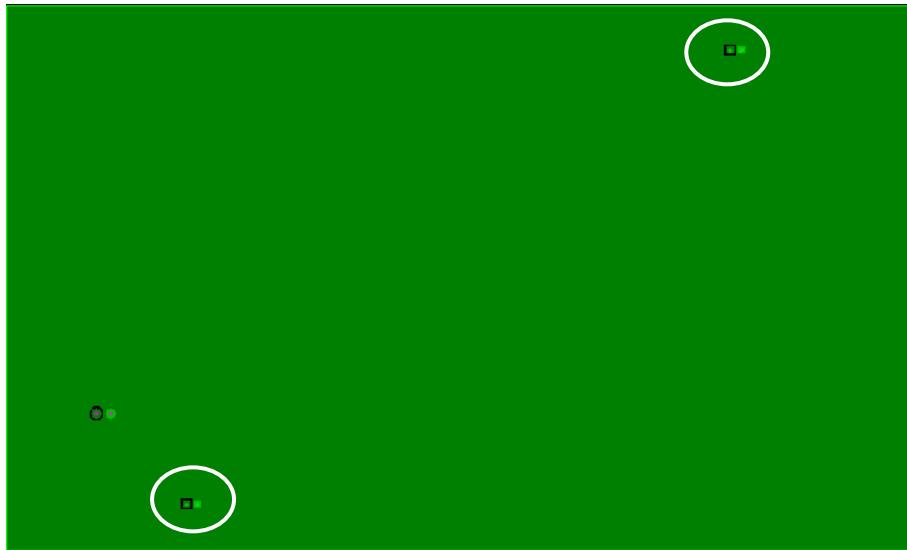
We now see the two drills connecting *X1* to *VCC* (on this layer) and to *GND* (on the layer below):



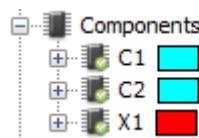
We zoom into the region around the drills to see there is a connection between the conductor on the layer and the left drill, and no connection between the layer and the right drill because of an anti-pad:



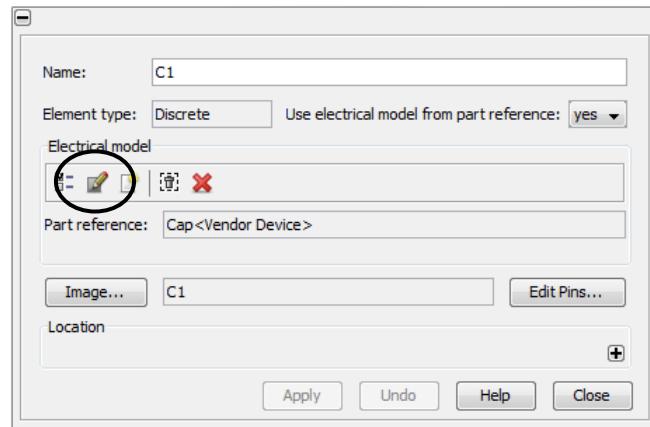
Now we zoom out again and change to layer *BOT* to see the drills and the connections for the two decoupling capacitors (see figure below) and finally select layer *Bottom Components* to see the capacitor components.



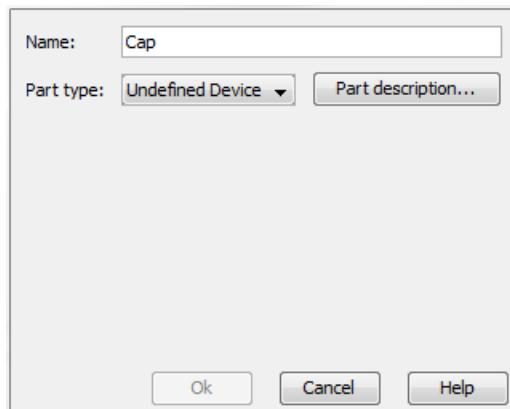
In order to have a deeper look at the capacitors' electric models we first go to the *Navigation Tree* and expand folder *Components* as shown in the figure below:



Now we select C1 and choose *Edit* by using the right mouse button. The following dialog will appear:

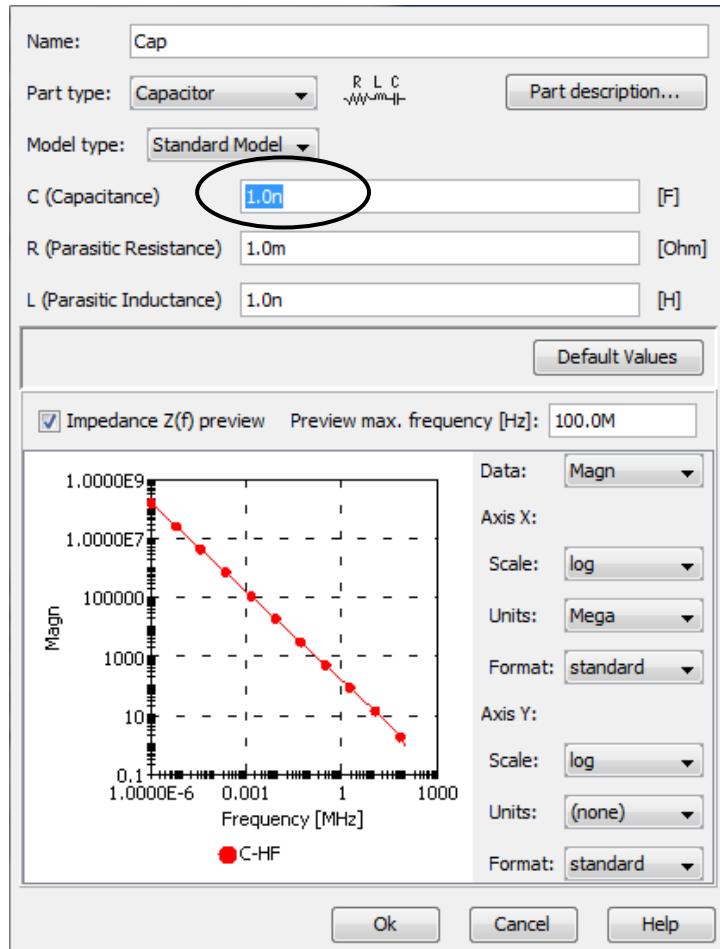


We see C1 refers to a model definition inside a part with name *Cap*. In order to edit this part, we press the marked symbol (see figure above). A dialog box appears telling that only an *Undefined Device* is assigned to this part.

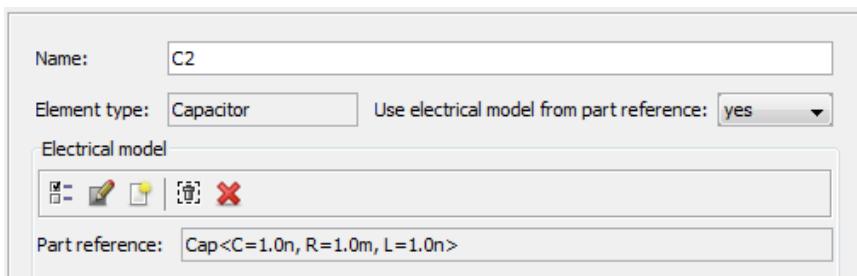


In order to assign a capacitor model to this part, we click on the field *Part type* and select *Capacitor* from the pull-down menu.

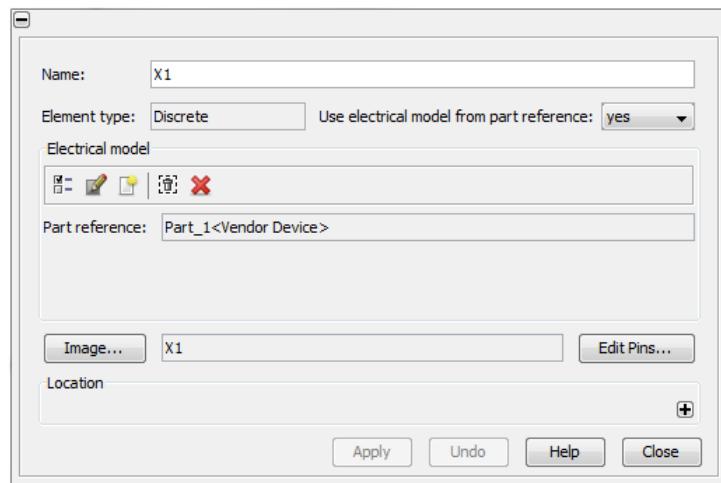
A new dialog box appears where we can set the corresponding capacitor model for the part Cap:



We change the capacitance value to 1.0 nF , leave the values for the parasitic resistance and parasitic inductance and finally press *Ok*. For the second capacitor C2, we don't have to make any further settings, since C2 also refers to the same part Cap. This can be seen by double-clicking on the component in the *Navigation Tree*:

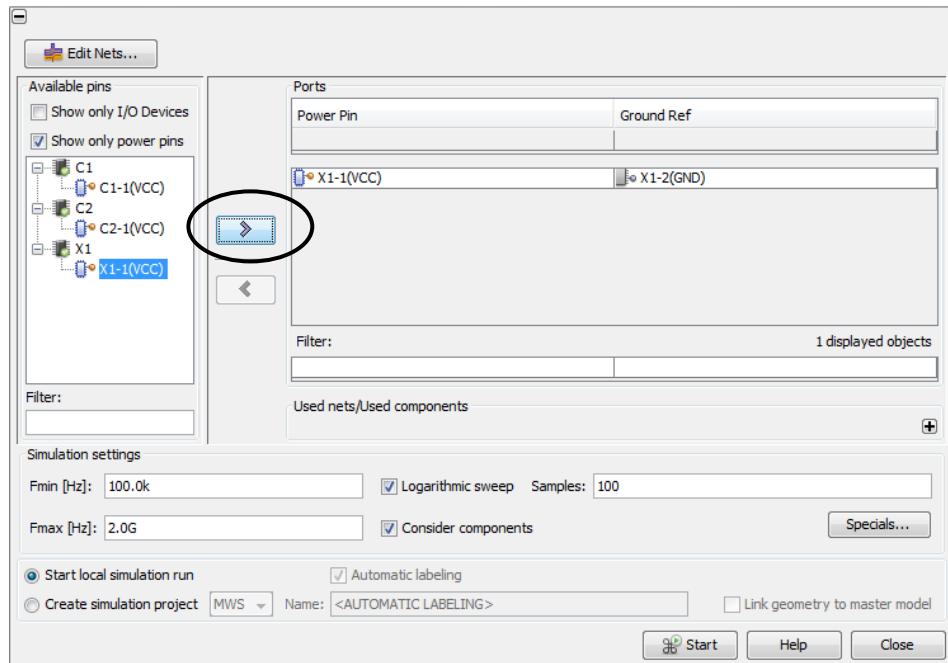


Before starting with the simulation setup we briefly explore the component X1:



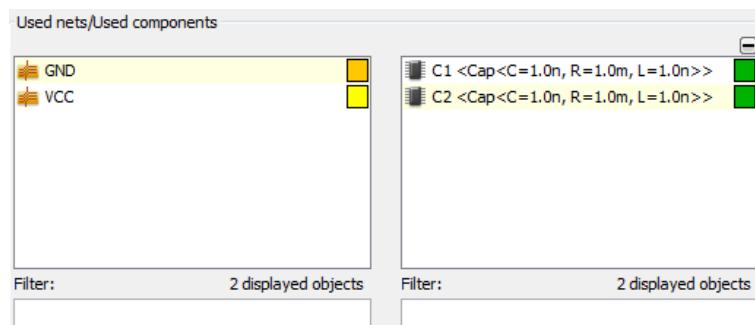
We see that the *Element type* of X1 is a general *Discrete* type and its electrical model is in the *Parts Library*. We don't need a further examination of this component since X1 will only be used to define a port in the following impedance analysis.

We set up the simulation task by pressing *Home: Simulation* \Rightarrow *PI Analysis*. The following dialog box will appear:

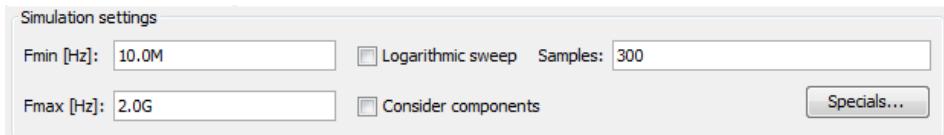


We see that only pins on *power nets* are listed in the *Available power pins* frame. This is because for *PI-analysis* only power pins and their related ground reference pins are of interest. We want to calculate the impedance between the *VCC*- and *GND* pin of *X1*. We select the pin *X1-1(VCC)* and click on the marked arrow in the middle of the dialog as it is shown in the figure above. On the right side, we see a port consisting of the selected power pin and its corresponding ground reference pin.

If we expand the *Used nets/Used components* frame we see that the two capacitors *C1* and *C2*, which both are connected between net *VCC* and net *GND*, are recognized and can be used within the simulation.

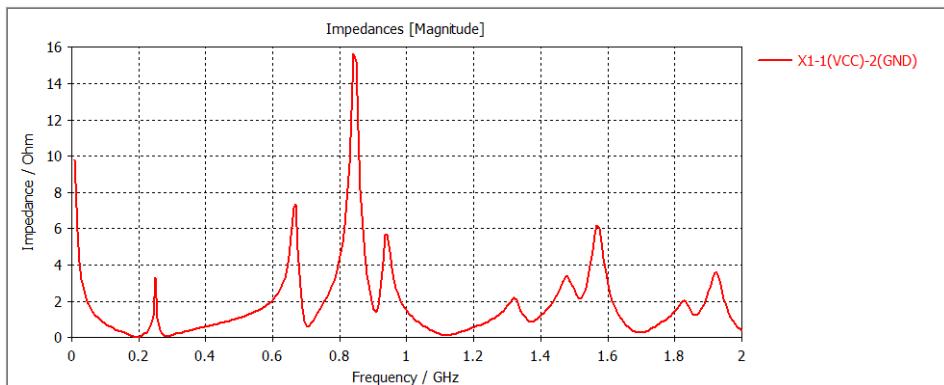


Next we set the *Simulation settings* as follows:

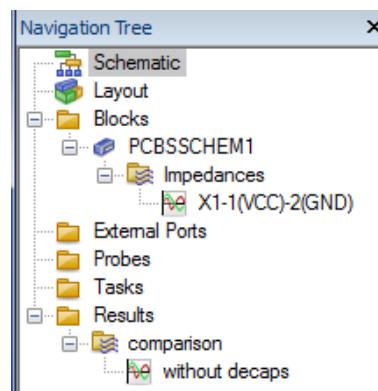


With the button *Consider components* we can control whether the linear two-pin components (resistors, inductors, capacitors), which are listed inside the *Used nets/Used components frame*, should be considered during the simulation or not. For the first simulation we uncheck the button and press *Start*.

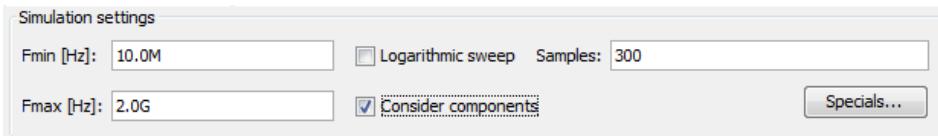
After a few seconds the result will appear automatically as shown in the figure below:



In order to store the curve for a comparison afterwards we generate a folder with name *comparison* below the *Results* folder and copy the result curve from the *Impedances* folder into the *comparison* folder under the name *without decaps* as shown in the figure below:

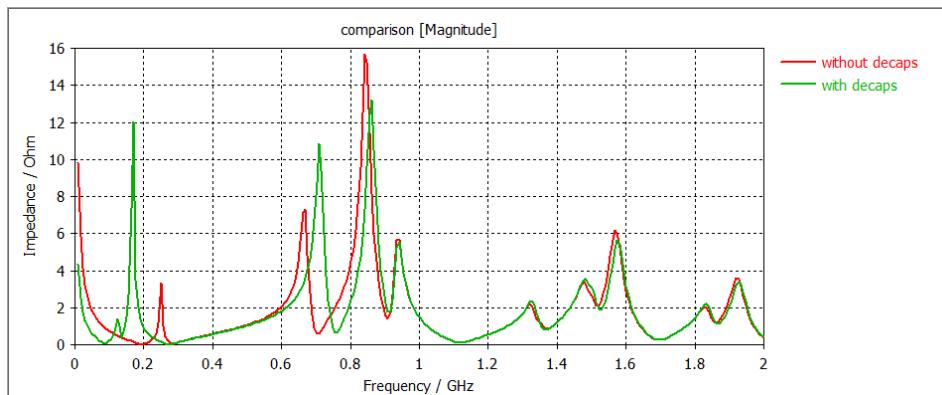


Now we change back to the *Solver Settings* tab and set the value of *Consider components* to *true*:

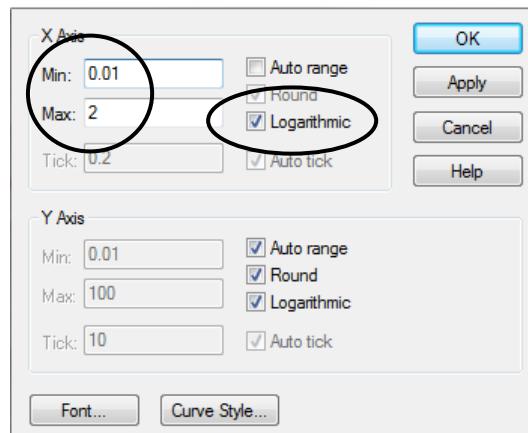


We accept the '*Change value & Delete model*' prompt and press the *Start* button once again. After another few seconds the new curve will appear. The curve now includes the effect of the decoupling capacitors.

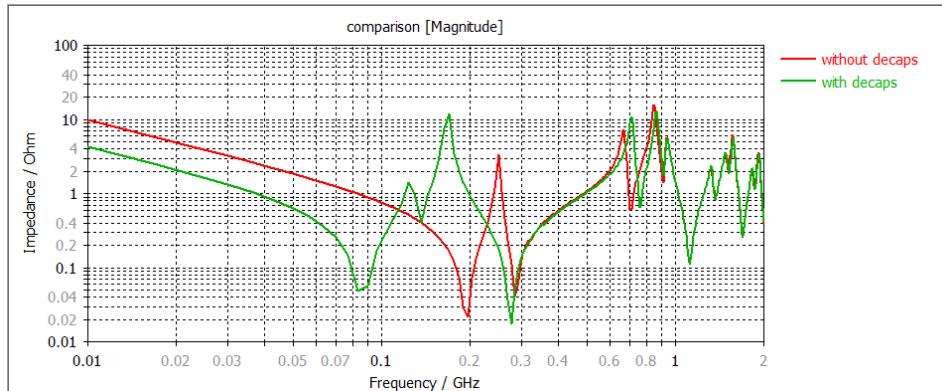
We copy this curve under the name *with decaps* in the *comparison* folder and compare two plots as shown in the figure below:



In order to get a logarithmic scaling of the curves we right mouse click in the *Main View* and select *Plot Properties* from the drop-down menu. In the arising dialog box we uncheck *Auto range* for the X Axis and adjust the *Min* and *Max* values first. Then we check *Logarithmic* for both axes:



Next we press *OK* and the displayed curves should look like in the figure below:



Chapter 4 — General Methodology

CST PCB STUDIO is designed to be easy to use. However, to work with the tool in the most efficient way the user should know the principal methods behind it. The main purpose of this chapter is to explain the theoretical concepts.

3D (PEEC) Modeling

The Partial Element Equivalent Circuit (PEEC) method divides a selected 3D structure (including conductors and dielectrics) into a mesh of short conductive segments and small conductive and dielectric areas. Constant currents inside the segments and constant charges on the areas are assumed.

There are different types of PEEC methods that differ in the way they treat retardation effects and in the way they handle dielectrics. The common feature of all types of PEEC methods is the transformation of the electromagnetic field problem into an electric network that can be simulated with a network simulator in time and frequency domain. Because of the electric connection of the conductive segments inside the network simulator, the models work for low frequency and DC.

CST PCB STUDIO uses a quasi-static PEEC approach. The magnetic coupling between the conductive segments is done by inductive coupling devices and the electric coupling between the conductive areas is done by capacitors, which takes into account the impact of the dielectric areas. The size of the circuit can be reduced by the amount of the dielectric areas and this is a big advantage of this approach but also the reason for limitations on the maximum allowed frequency. The longest distance between two coupled elements (segments or areas) limits the maximum frequency range of the whole circuit. The maximum valid frequency is evaluated by the program automatically.

There are many applications of the PEEC method and CST PCB STUDIO features additional approximation tools in order to enable the usage for complex PCBs. But the most appropriate applications for this method are boards with a small number of layers and no reference plane with clearly defined characteristic impedances present. This means the 3DPEEC method is most suitable in the case that the conductors cannot be modeled as microstrips or striplines due to the absence of a ground, from which the characteristic impedance could be determined.

2D (TL) Modeling

The Transmission Line Modeling method parses a single trace or a group of traces and divides them into a finite number of straight segments. For each segment the program checks for any conductive areas surrounding the traces which may serve as reference conductors. All traces in a segment, in combination with additional reference areas, define its cross-section. The primary transmission line parameter per unit length (R' , L' , C' , G') will be calculated by a static 2D field solver.

In a following step all segments will be transformed into an equivalent circuit. The procedure even considers vias and creates related equivalent circuits as well. Finally all circuits will be connected together into one single electrical model representing the whole trace or group of traces.

The procedure implies that only *TEM* propagation modes can be considered and this causes two limitations. First, the model is only valid inside a frequency range from DC to a maximum frequency. This is due to the fact that the primary transmission line parameters are static parameters and only valid when the geometric dimensions behind the calculation are significantly smaller than the shortest wavelength of the propagating wave. A second limitation is that additional effects on typical discontinuities like bends, deviations or open ends are not considered.

The method is best used in the classical SI analysis where wave propagation effects on signal lines into high-speed multi-layer boards have to be analyzed. The method assumes ideal power delivery systems and does not take into account any effects like ground bouncing.

3D (FE/FD) Modeling

The 3D (FE FD) solver is based on the frequency-domain Finite-Element method, combined with a domain-decomposition approach. Problem-adapted basis functions are used to improve simulation performance by exploiting the structural characteristics of the PCB.

In order to explain the underlying idea, we first note that multi-layer PCBs, despite their first-sight high complexity, exhibit strong internal structuring, such as the layer-based geometry, solid power/ground planes, highly repetitive local via domains, and signal traces which follow strong design constraints, like bounding to reference planes and 45-degree routing, just to name a few. It is clear that exploiting these characteristics within a numerical method leads to tremendous performance improvements when compared to a general but monolithic approach (like standard Finite Elements).

Thus, as an essential first step, the present solver algorithm identifies the partial volumes (called *specific domains*) of the whole PCB volume that allows a specialized and efficient numerical description, due to the above-mentioned structural elements. In the current version, these are: (i) domains sandwiched between copper areas/planes, possibly containing intermediate signal layers, (ii) vias and their local surroundings, (iii) domains containing microstrip lines. Ideally, the specific domains cover all relevant aspects of the PDN.

Method approximations

CST PCB STUDIO specializes in the fast and accurate simulation of electromagnetic transmission effects of PCBs. This specialization brings some limitations which are summarized below:

- The PEEC modeling method is based on a *quasi-static* 3D approach where all selected conductors are divided into a number of elements and transferred into an equivalent circuit consisting of resistors, inductors and capacitors. The capacitor and inductor representing the longest distance between two mesh elements limit the maximum frequency range of the whole circuit. The maximum valid frequency is evaluated by the program automatically.
- The 2D modeling method is based on classical transmission line theory where all selected transmission lines are divided in a finite number of straight segments with constant cross-sections and is used for **signal-integrity applications** (SITD Analysis and SIFD Analysis). For each segment the primary transmission line

parameters (R' , L' , C' , G') will be calculated via a 2D static field calculation. This means the maximum frequency range is limited by the largest dimension of the cross-section inside a segment. The maximum valid frequency is evaluated by the program automatically.

- The 3D (FE FD) method has been developed with the focus **on power-integrity applications** (PI Analysis). As described above, the current implementation accurately models the full-wave electromagnetic effects for the typical building blocks of power-distribution networks (PDN) of multi-layer PCBs. These are, (i) domains sandwiched between PDN copper areas/planes, (ii) vias and their local surroundings, (iii) domains containing microstrip lines. The solver should therefore be used for analyzing PDNs having distributed capacitance (power/ground plane pairs). In turn, if this precondition is not met, other modeling techniques are recommended (e.g. PEEC).

Chapter 5 – Finding Further Information

After carefully reading this manual, you will have a basic understanding of how to use CST PCB STUDIO efficiently. However, when you are creating your own designs many questions will arise. In this chapter we will give you a quick overview of the available documentation.

Other Printed Documents

A more detailed introduction into the circuit simulator can be found in the 'CST DESIGN STUDIO - Workflow' document. You will find it in the same directory as this document.

Online Reference Documentation

You can access the CST STUDIO SUITE online help system's overview page at any time by choosing *File: Help ⇨ CST STUDIO SUITE-Help*.

Please refer to the CST STUDIO SUITE *Getting Started* manual for more information about how to use the online help system.

Examples

The installation directory of CST STUDIO SUITE contains an examples subdirectory containing some of typical application examples. A quick overview of the existing examples can be obtained by browsing through the descriptions of the examples inside the online help system. These examples may contain helpful hints that can be transferred to your particular application.

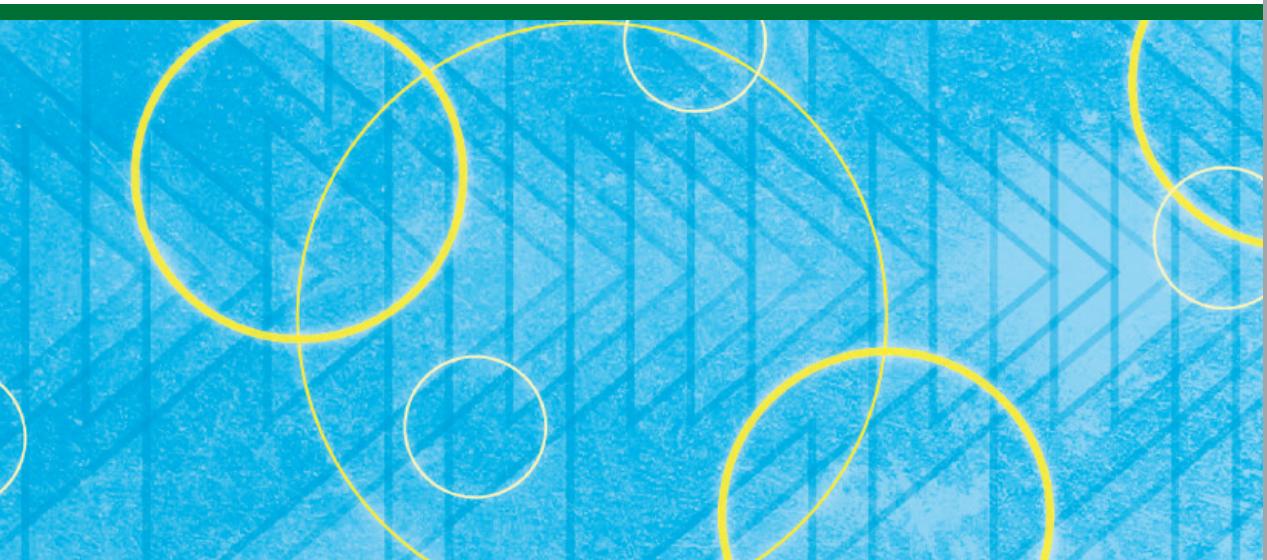
Access Technical Support

After you have solved your first model with CST PCB STUDIO, you may send the project file (with the extension 'cst') to the technical support team. Even after your model has been successfully run, further investigation of the set up may lead to better and faster results.

The support area on our homepage (www.cst.com) contains a lot of useful and frequently updated information. A simplified access to this area is provided by choosing *Help ⇨ Online Support*. You only need to enter your user name and password once. Afterward, the support area will be opened automatically whenever you choose this menu command.

History of Changes

The history of changes between software releases of the program is available via the online help system. Since there are many new features in each new version, you should browse through the list even if you are familiar with one of the previous releases.



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