Introduction to MEMS and Micromachining Technology

Short Course, Xiamen University 2003

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About Me

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- M.S., 1999, Dept. of EECS, Case Western Reserve University, Cleveland, OH, USA
  - Advisor: Prof. Mehran Mehregany
  - Thesis Title: “Metal contacts and hydrocarbon gas sensors based on 3C-SiC film grown on silicon”

- Ph.D., 2002, Dept. of EECS, Case Western Reserve University, Cleveland, OH, USA
  - Advisor: Prof. Mehran Mehregany
  - Dissertation Title: “Fabrication and applications of 3C-silicon carbide on insulator by the grow-a-substrate method”

Outline

- Introduction
- Photolithography
- Surface Micromachining
- Bulk Micromachining
- Packaging

The material for this short course can be found at: http://www.kuos.org/mems.htm

What is MEMS?

- MEMS is standing for **M**icro**e**lectro**m**echanical **S**ystems(微機電), which are integrated micro devices or systems combining electrical and mechanical components.

- "MEMS fabrication uses integrated circuit (IC) batch processing techniques and can range in size from micrometers to millimeters. These systems can sense, control and actuate on the micro scale, and function individually or in arrays to generate effects on the macro scale."
  - Adapt from MEMSCap "all about MEMS"

Why MEMS?

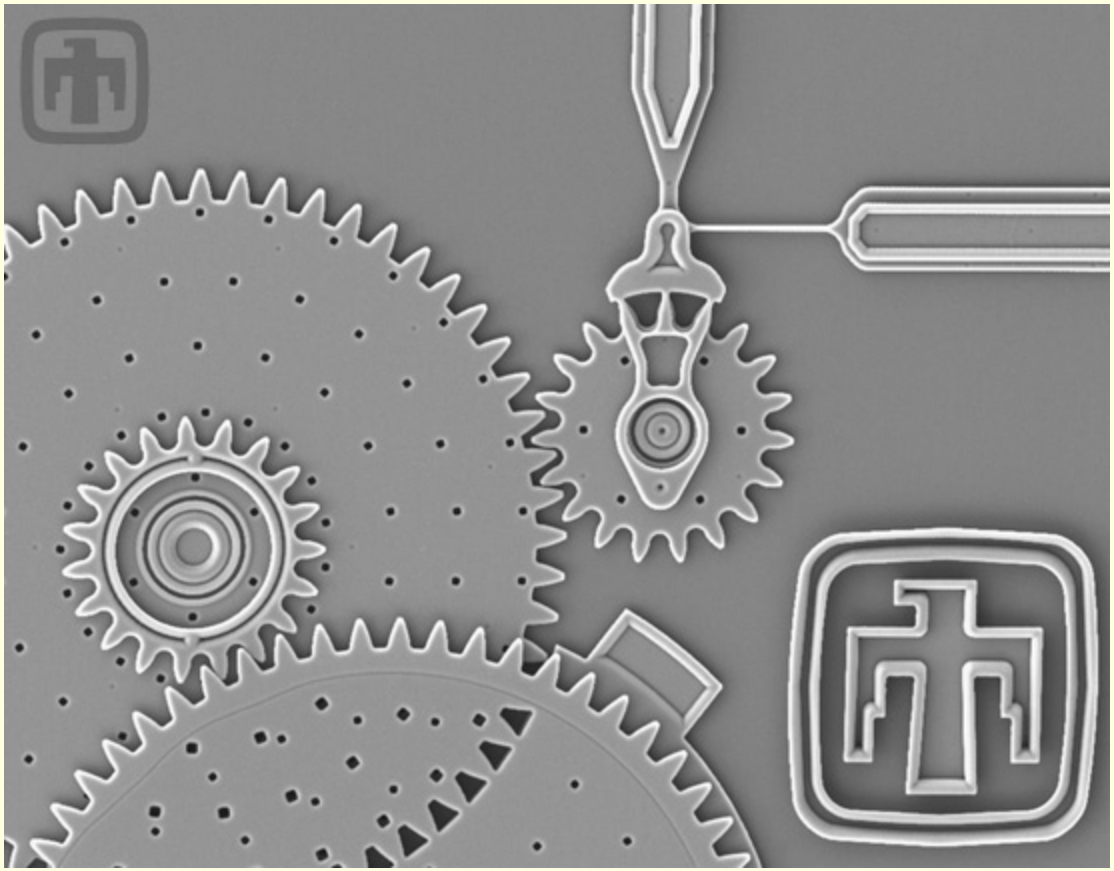
- Price Reduction
  - Adapt IC Fabrication Process $\Rightarrow$ Mass Fabrication
  - Adapt used or existing IC Fabrication Tools $\Rightarrow$ Cheaper capital investment
  - Size reduction (cm to μm, nm)$\Rightarrow$ More devices on a wafer
- Increase Value
  - System integration in a chip
  - Performance enhancement
- Versatile
  - BIO MEMS, Optical MEMS, RF MEMS, Lab-on-Chip, Chemical and Physical Sensors, etc.

Analysis and Forecast of US MEMS Markets (in Millions of US Dollars)

Year	Automotive	Medical	Information Technology & Industrial	Military & Aerospace	Total
1994	255.7	129.5	438.3	49.1	872.5
1995	298.0	146.1	459.0	54.8	957.9
1996	355.0	164.4	492.8	62.2	1,074.3
1997	419.0	187.0	527.0	71.6	1,204.6
1998	491.5	216.7	575.3	79.6	1,363.1
1999	562.0	245.7	645.9	95.8	1,549.4
2000	645.7	291.3	733.3	110.7	1,781.0
2001	758.5	354.8	836.0	133.3	2,082.5
2002	879.6	444.7	995.1	156.9	2,476.3
2003	1,019	562.9	1,222	176.7	2,980.4
2004	1,172	716.0	1,514	202.7	3,604.5

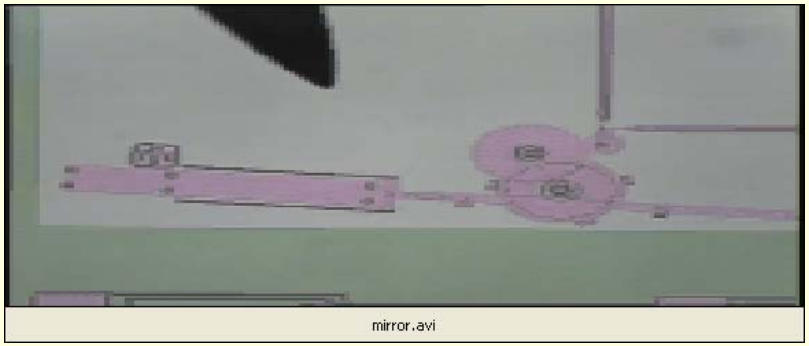
Source: Maluf, “An Introduction to Microelectromechanical Systems Engineering”; Based on the research data on www.frost.com

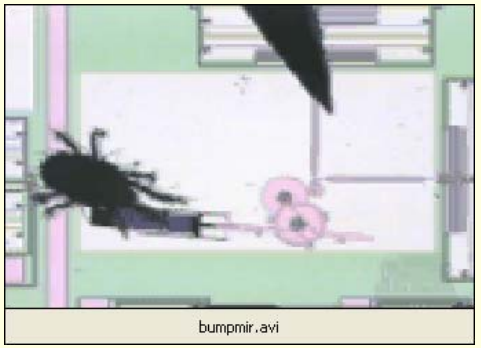
Sandia: Multiple Gear Speed Reduction Unit



Source: Sandia National Labatories; mems.sandia.gov

Micromirror from Sandia National Laboratory

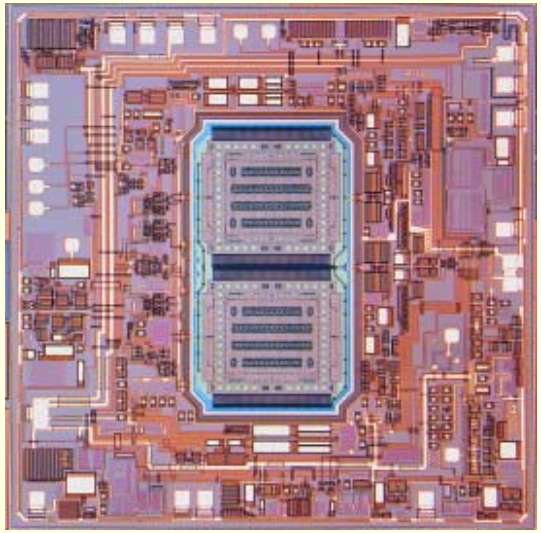




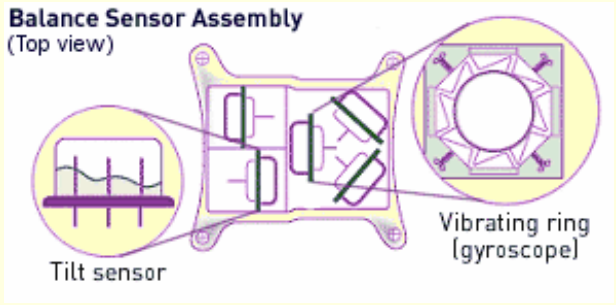
Pop-up Silicon Mirror
Force provided by a comb drive actuator moves a linear rack, which drives a hinged sheet of silicon back and forth. A HeNe optical-band (red) laser is focused at an angle such that as the mirror is elevated, the coherent light is reflected into the microscope's camera.
Source: Sandia National Laboratory

Spider Mite Test
This micromirror continues to be operational even after being tested by the spider mite
Source: Sandia National Laboratory

Analog Device: Gyroscope

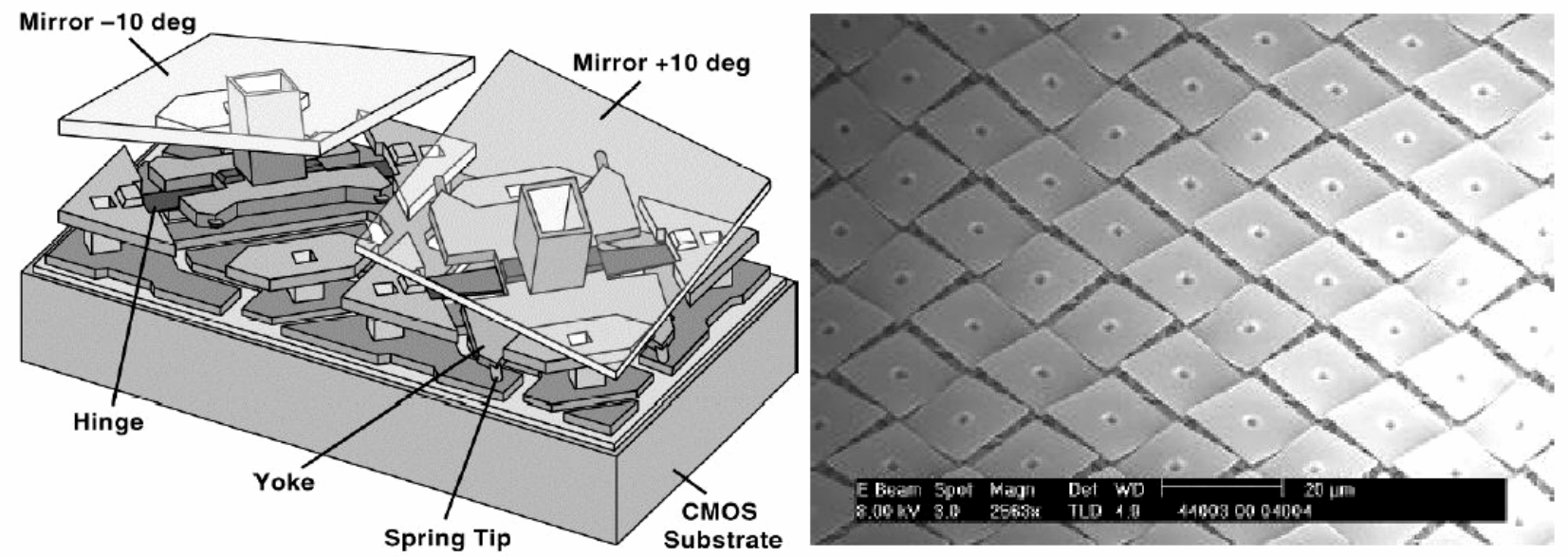


Integrated Gyroscope, Courtesy of Analog Device

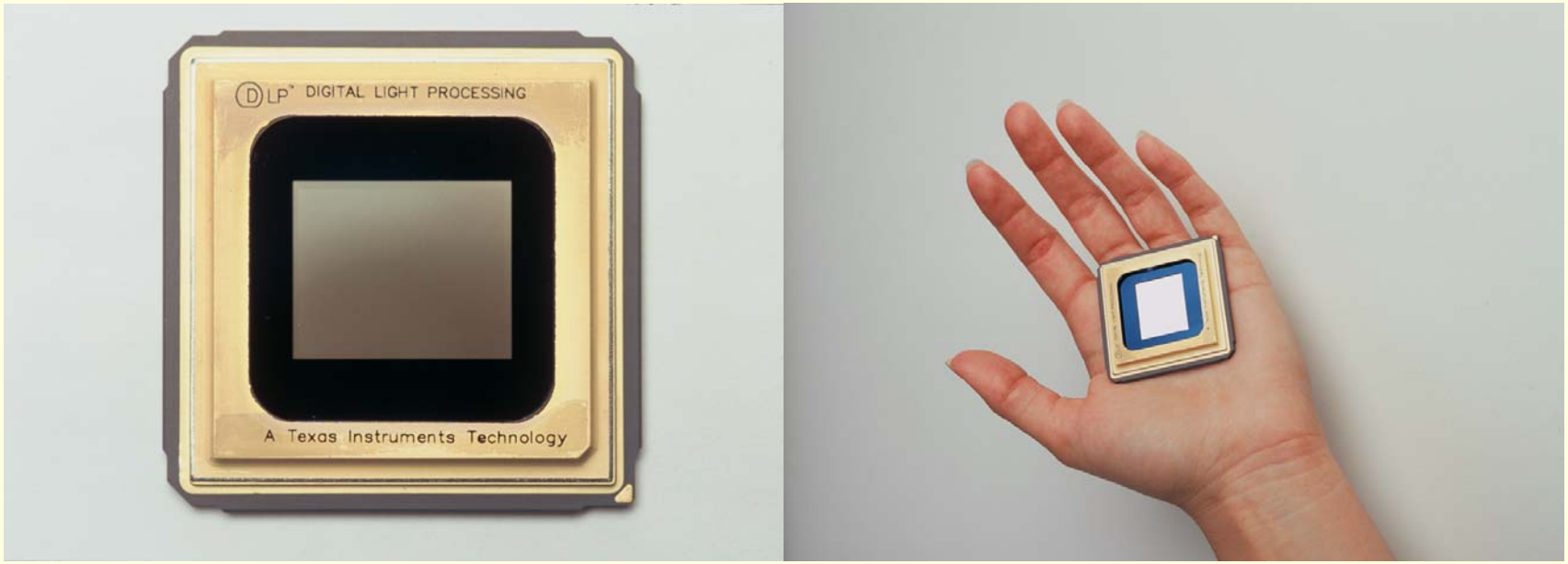


Segway™ HT

Texas Instrument: DMD™ (Digital Micromirror Devices)



Texas Instrument: DMD™ (Digital Micromirror Devices)

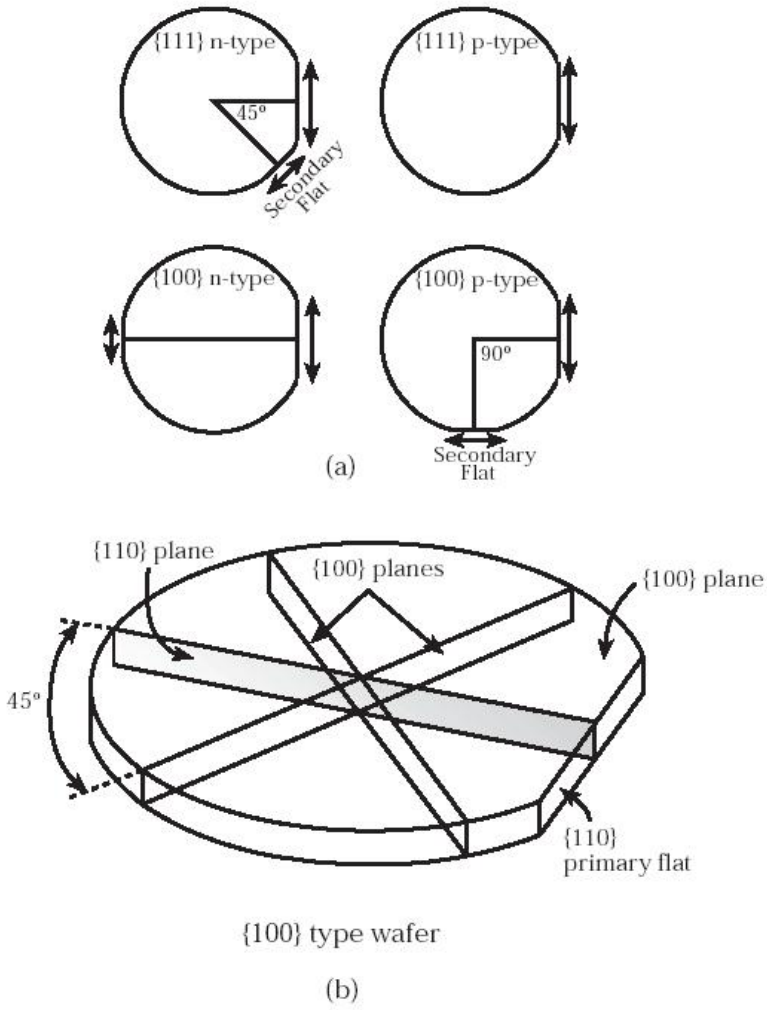


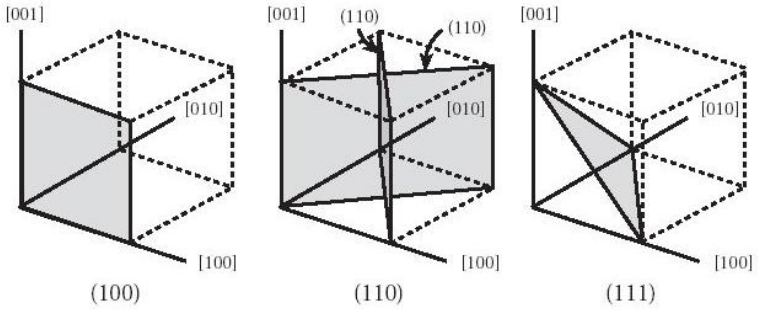
- **SXGA DMD:** SXGA device with black aperture: 1280x1024; 1,310,720 mirrors

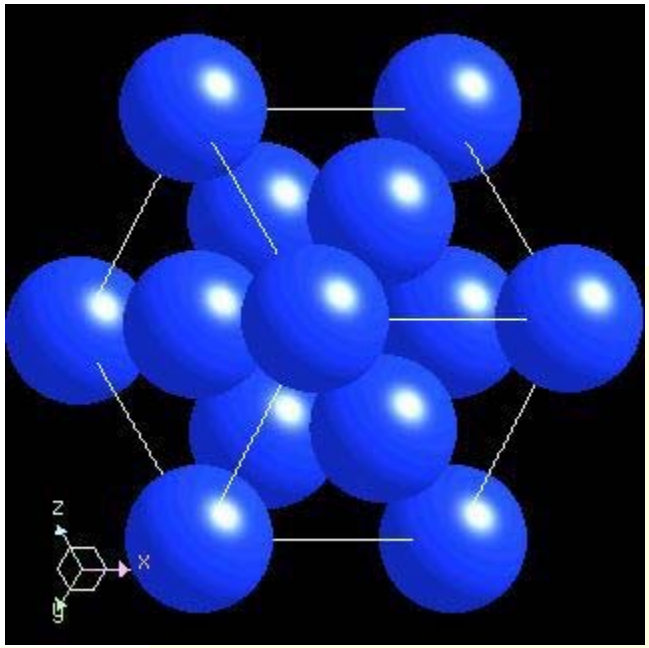
Properties of Silicon

	Si	SiO_2	Si_3N_4	SiC	Stainless Steel
Yield Strength (GPa)	7	8.4	14	21	2.1
Young's Modulus (GPa)	160	73	323	450	70
Poission's Ratio	0.22	0.17	0.17	0.14	0.3
Density (g/cm^3)	2.4	2.3	3.1	3.2	7.9
Thermal Conductivity (W/cm·K)	1.57	0.014	0.19	5	0.329
Thermal Expansion Coeff. (10^6/K)	2.6	0.55	2.8	4.2	17.3

Orientation of Silicon







Source: Maluf, "An Introduction to MEMS Engineering" Artech House (2000)

Source: www.webelements.com

Wafer Cleaning Process

- **Piranha**
  - When to use?
    - After wafers bring into cleanroom
    - Strip photoresist
  - To remove organic contamination
  - $H_2SO_4 : H_2O_2 = 4 : 1$ (20~30 min)
- **RCA (Developed by Kern and Puotinen in RCA, 1970)**
  - When to use?
    - Before bring processed wafers into cleanroom
    - Before any furnace process
  - RCA 1 (15 min)
    - To remove residual organic contamination
    - $H_2O_2 : NH_4OH$: DI water (1:1:5) in 75~80 °C
  - HF Dip (30 sec)
    - To remove native oxide on surface
    - HF (49%) : DI Water (1:10)
  - RCA 2 (15 min)
    - Desorption of remaining atomic and ionic contaminates
    - H_2O_2 : HCl : DI water (1:1:5) in 75~80 °C

Wafer Cleaning Process

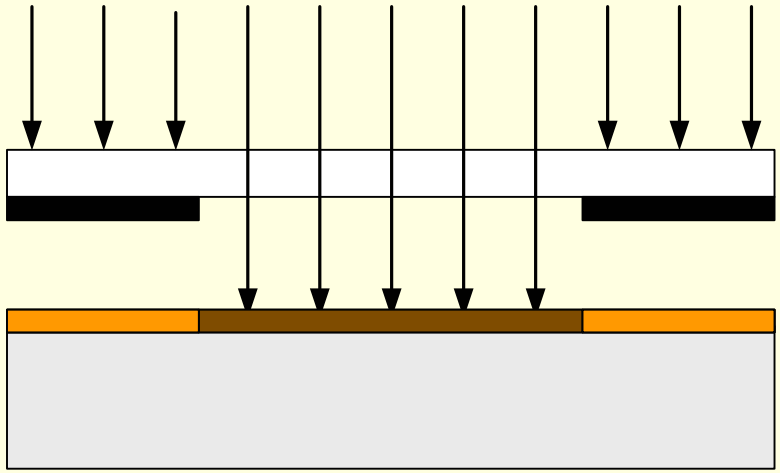
- DI Water
  - Facts:
    - 1500 gallons of city water produce 1000 gallons DI water
    - Production one 200mm wafer requires 200 gallons DI water
  - Requires constantly monitor water's resistivity (>17 MOhm) to ensure water quality
- Rinse
  - To remove chemical from previous process, usually done by spraying DI water to wafer for 3 times
- Spin-Rinse-Dryer (SRD)
  - Remove excess water from wafer's surface

Fabrication Process

- Photolithography
- Additive Process (Surface Micromachining)
- Substrate Process (Bulk Micromachining)
- Packaging

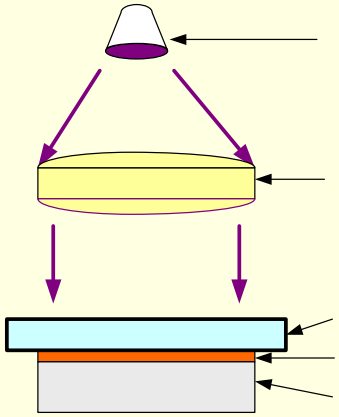
Photolithography Process

- Start with silicon wafer
- HMDS prime
- Spin photoresist
- Softbake
- UV Exposure Through mask
- Develop

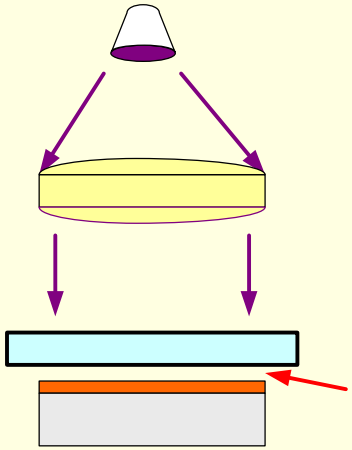


Methods of Transferring Patterns

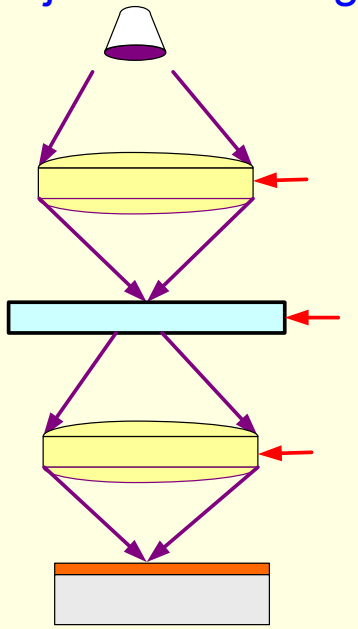
Contact Printing



Proximity Printing



Projection Printing



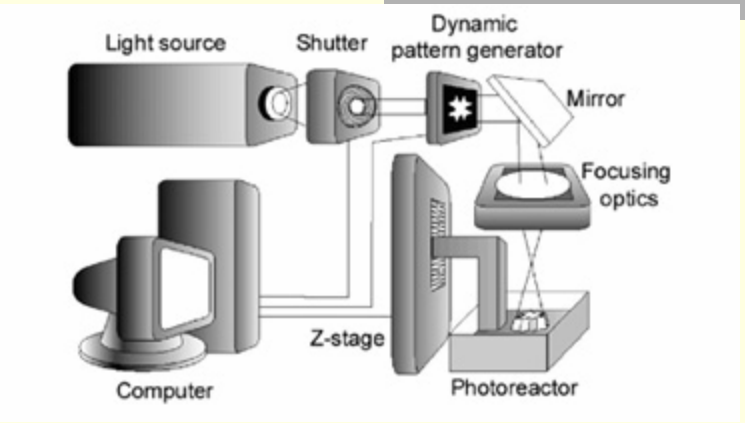
- Contact Printing
  - Best resolution
  - Defects and contamination on mask may occur
- Proximity Printing
  - Does not make contact
  - Less mask damage
  - ~10μm resolution
- Projection Printing
  - Does not make contact
  - High resolution lens projects an image of mask onto the PR-covered wafer
  - Good resolution

Other Lithography Methods I

- Electron Beam Lithography
  - Use focus beam instead of light source
  - Pro:
    - Nanoscale resolution without using mask
    - Lower defect density
    - Diffraction is negligible
  - Con:
    - Very slow
- X-ray Lithography
  - Pro:
    - Flood exposure $\Rightarrow$ fast
    - Making molds for LIGA
  - Con:
    - Requires x-ray source and x-ray mask
- "Soft Lithography" (Whitesides, Harvard Univ.)
  - Using PDMS as physical mold to "print" on structures

Other Lithography Methods II

- Microstereolithography
  - Fabricated by using photo-induced polymerization of a liquid resin (SU-8)
  - Polymerize one layer at a time
  - The good
    - Capable of 3D and high aspect ratio microstructures
    - Works with different materials
    - No photo mask required
    - Fast prototyping, allows desktop microfabrication
  - The bad
    - Low resolution (3~5 μm)
    - Slow



Source: Arnaud Bertsch, http://lmis4.epfl.ch/~abertsch/

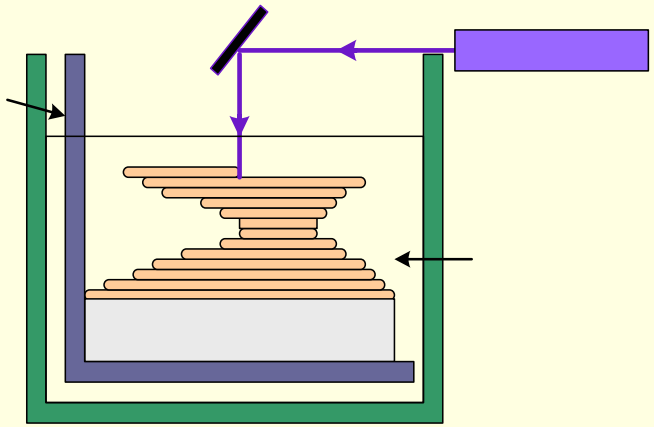
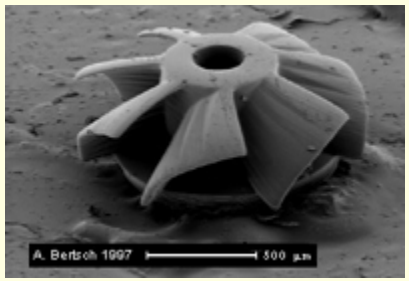
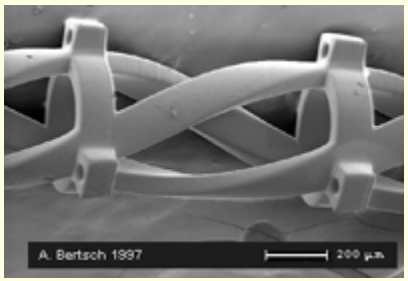


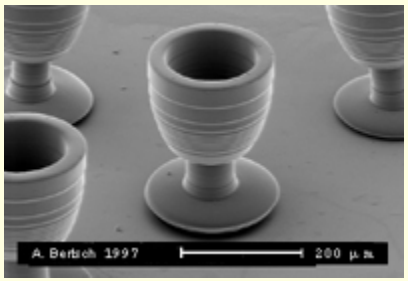
Image Gallery for Microstereolithography



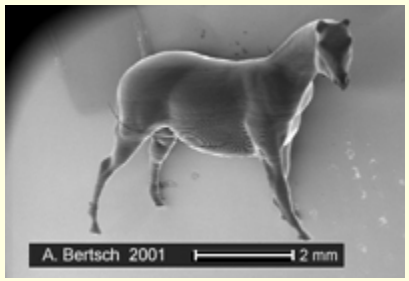
Turbine



Small spring

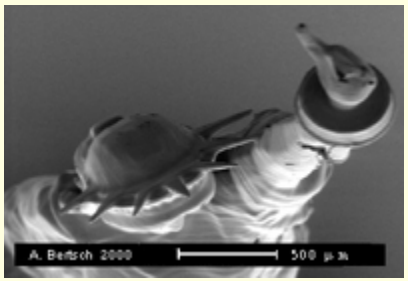


Small cup



Small horse

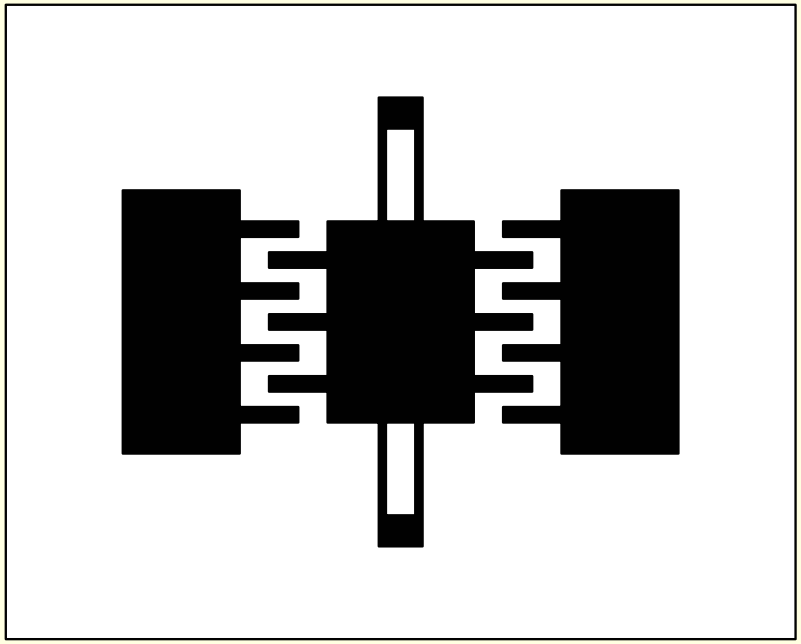
Miniature Porsche



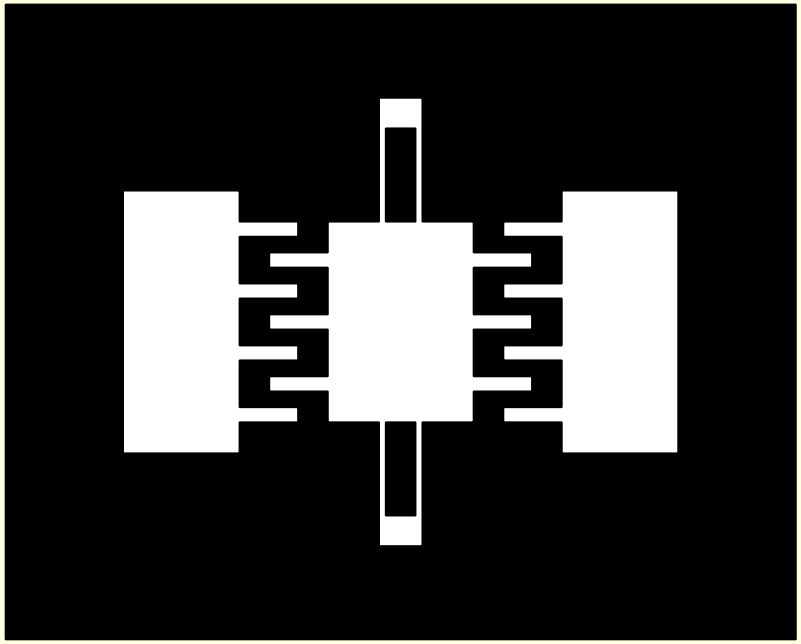
Miniature statue of liberity

Source: Arnaud Bertsch, http://lmis4.epfl.ch/~abertsch/

Photo Mask

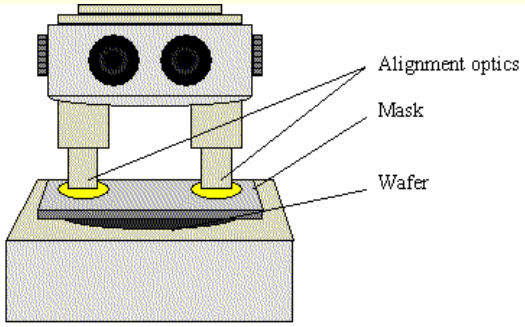


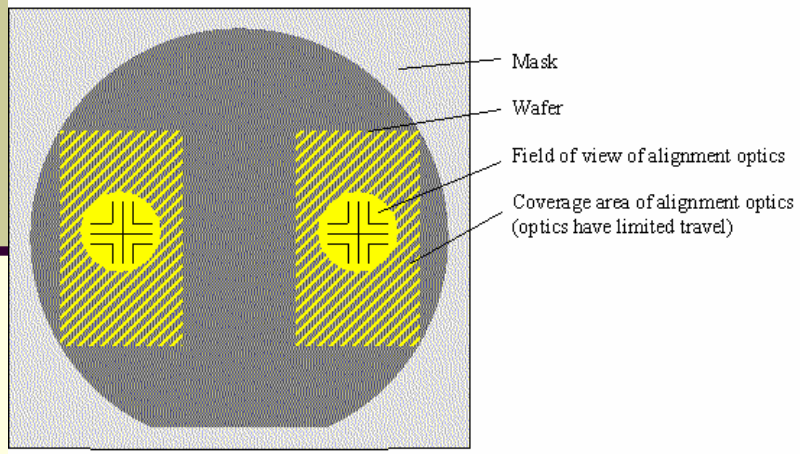
Clear Field

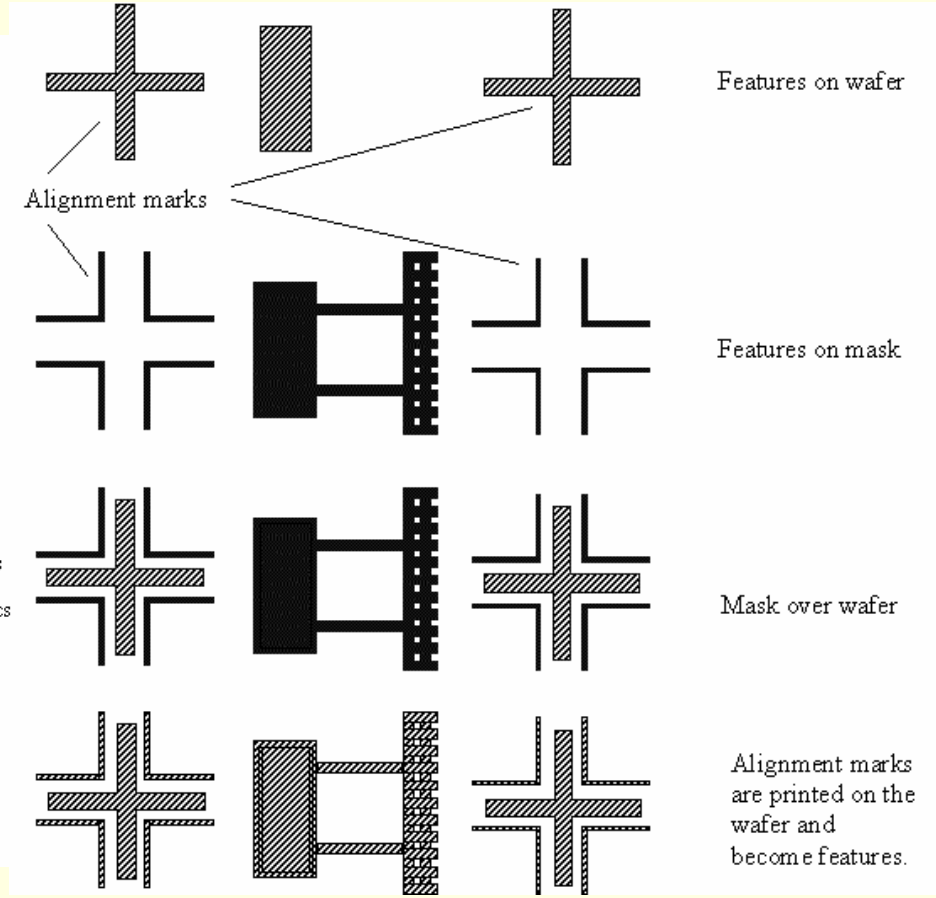


Dark Field

Alignment







From www.memsnet.org

Photoresist Stripping

- Completely removal photoresist without damaging devices under construction
- Wet Stripping
  - Acetone: Can be used if post bake was not too long or not too high in temperature
  - Piranha: Can be used if no metallic layer underneath
- Dry Stripping (Ashing)
  - Reactive plasma stripping: with oxygen $\Rightarrow$ reactive O atom will convert PR into gaseous product
  - Gaseous chemical reactants: ozone $\Rightarrow$ ozone will attack PR in atmospheric pressure
  - Radiation combination: UV/ozone $\Rightarrow$ UV assist breaking bond in PR, more efficient for ozone to attack

Additive Process (Surface Micromachining)

- Oxidation
- Physical Vapor Deposition (PVD)
- Chemical Vapor Deposition (CVD)

Additive Process

- **Oxidation**
- Physical Vapor Deposition (PVD)
- Chemical Vapor Deposition (CVD)

Thermal Oxidation

- Dry Oxidation

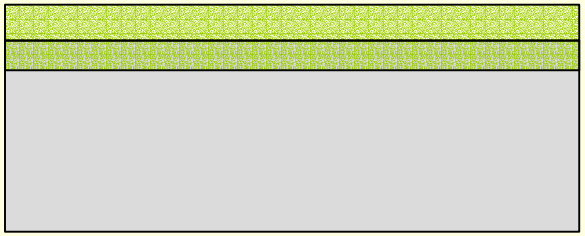
  Si (solid) + O_2 (vapor) $\rightarrow$ SiO_2 (solid)

- Wet Oxidation

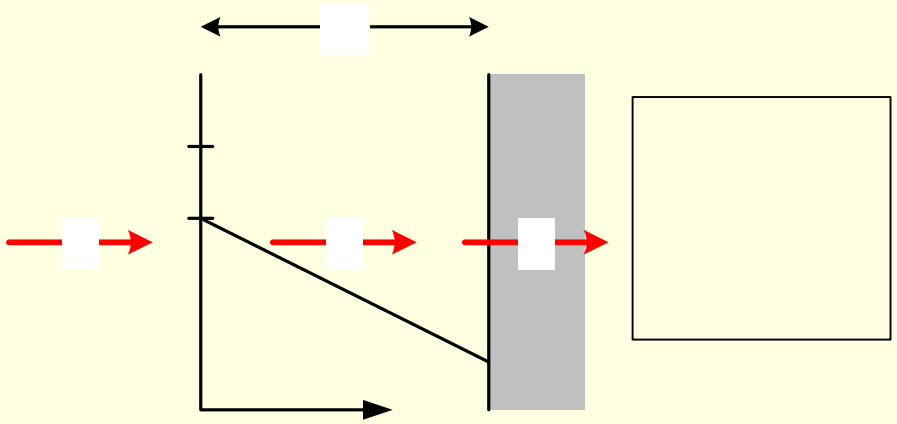
  Si (solid) + $2H_2O$ (vapor) $\rightarrow$ SiO_2 (solid) + $2H_2$

- The ratio of Si thickness converted, X_{Si} to resulting oxide thickness, X_{ox}, is

$$\frac{X_{Si}}{X_{ox}} = 0.46$$



Oxidation Kinetics



- **F_1:** Gas phase transport to the surface
- **F_2:** Diffusion to the existing oxide
- **F_3:** Oxidation reaction

h: gas phase mass-transfer coefficient
k_s: Si oxidation rate constant
C*: equilibrium oxidant concentration in the oxide = $H \cdot P_G$
H: Henry's law constant
P_G: Partial pressure of oxidant in the gas phase

Gas Oxide

Oxidation Rate

- Oxide growth rate:

$$\frac{dX_{ox}}{dt} = \frac{C_i k_s}{N}$$

  - Solution for the equation

$$X_{ox}(t) = \frac{A}{2}\left\{\left[1 + \frac{(t+\tau)}{A^2}4B\right]^{\frac{1}{2}} - 1\right\}$$

X_{ox}: oxide thickness
k_s: Si oxidation rate constant
D: oxidant diffusivity
C_i: Concentration of oxidant at the interface of oxide/silicon
N: number for the molecules of oxidant per unit volume of oxide ($2.2\times10^{22}cm^{-3}$ for dry oxygen)

Where **A**=$2D(1/k_s+1/h)$
B=$2DC^*/N$
$\tau=(X_i2+AX_i)/B$
h: gas phase mass transport coefficient
C*: equilibrium oxidant concentration in the oxide=HP_G
H: Henry's law constant
P_G: Partial pressure of oxidant in the gas phase
X_i: initial oxide thickness

- **For Thin Oxide, $(t+\tau)>>A^2/4B$**

$$X_{ox} = \frac{B}{A}(t+\tau)$$

- **For Thick Oxide, $t>>\tau$ and $t>>A^2/4B$**

$$X_{ox}^2 = B(1+\tau)$$

Oxidation Rate (cont.)

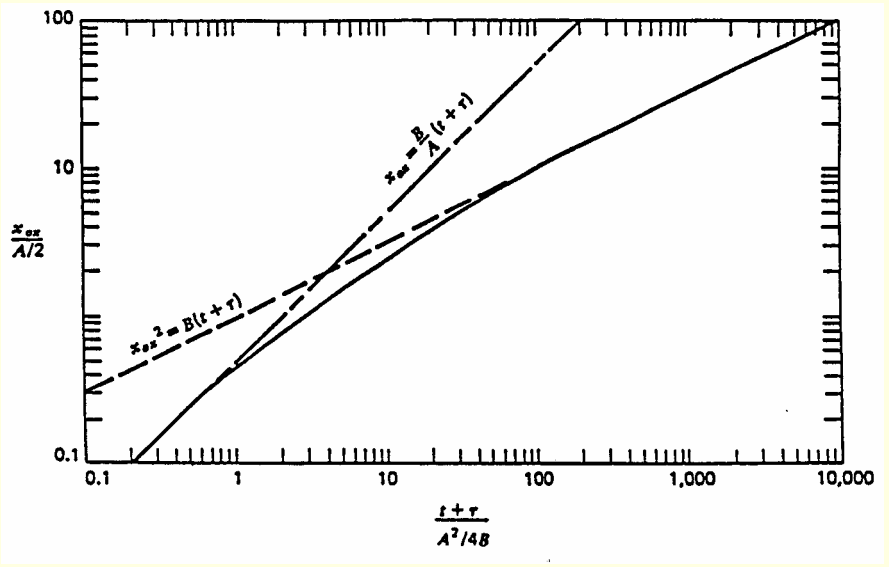
Rate constants for Wet Oxidation of Si

Temp (°C)	A (μ m)	Parabolic Rate Constant, B (μ m2/hr)	Linear Rate Constant, B/A (μ m/hr)	τ (hr)
1200	0.05	0.720	14.40	0
1100	0.11	0.510	4.64	0
1000	0.226	0.287	1.27	0

Rate constants for Dry Oxidation of Si

Temp (°C)	A (μ m)	Parabolic Rate Constant, B (μ m2/hr)	Linear Rate Constant, B/A (μ m/hr)	τ (hr)
1200	0.040	0.045	1.12	0.027
1100	0.090	0.027	0.30	0.067
1000	0.165	0.0117	0.071	0.37

Deal and Grove, "General Relationship for the Thermal Oxidation of Silicon", J. of Applied Physics, **36**, p3770, (1965)



Source: Wolf, "Silicon Processing for the VLSI Era, Lattice Press, 1986

Low Temperature Oxide (LTO)

- Lot Temperature Oxide (LTO) can be used over aluminum moralization (below 350°C)

- Example reactions:

  Silane + oxygen: $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$

  Tetrathoxysilane (TEOS) decomposition: $Si(OC_2H_5)_4 \rightarrow SiO_2$ + by- products

  Dichlorosilane + nitrous oxide: $SiCl_2H_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl$

Deposition Type	PECVD	$SiH_4 + O_2$	TEOS	$SiCl_2H2+N_2O$	Thermal
Typical temp.	200 °C	450 °C	700 °C	900 °C	1100 °C
Step coverage	varies	nonconformal	conformal	conformal	conformal
Density (g/cm^3)	2.3	2.1	2.2	2.2	2.2
Stress (MPa)	300 comp – 300 tens	300 tens	100 com	300 comp	300 comp
Dielectric strength (10^6 V/cm)	3 - 6	8	10	10	10
Etch rate in 100:1 HF (nm/min)	40	6	3	3	3

After Adams, “Dielectric and Polysilicon Film Deposition” in “VSLI Technology” Sze [ed], McGraw-Hill, Inc. 1983

Doping

- Purpose of doping in MEMS:
  - Make P++ etch stop
  - Change restivity of the film (e.g. make piezoresistor, connecting wire)
- Dopant Types
  - P-type (boron)
  - N-type (phosphorous, arsenic)
- Doping Methods
  - Diffusion
  - Ion implantation

Diffusion: Predeposition

- Dopants were diffused thermally into the substrate in furnace at 950~1280°C
- Fick's law to describe diffusion of dopant in silicon
  - **Fick's first law:** ***The dopant flux is proportional to the concentration gradient***

$$J = -D\frac{\partial C(x,t)}{\partial x}$$

  - **Fick's second law:** ***The flux gradient is proportional to the time ratio change***

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \Rightarrow D\frac{\partial^2 C(x,t)}{\partial x}$$

If diffusion coefficient is independence of position

  - Initial conditional
    - $C(x,0)=0$
  - Boundary condition
    - $C(0,t)=C_s$
    - $C(\infty,t)=0$
  - Solution to Fick's Second Law

$$C(x,t) = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

erfc is the complementary error function, $(Dt)^{1/2}$ is the diffusion length

  - Total amount of impurity Q(t) in the diffused layer

$$Q(t) = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt}$$

  - Junction depth x_j is the distance in the silicon at which the diffuse profile is equal to the substrate background concentration, $C_{sub} \Rightarrow C(x_j,t)=C_{sub}$

$$x_j = 2\sqrt{Dt}\, erfc^{-1}\frac{C_{sub}}{C_s}$$

Diffusion: Thermal Diffusion

- Thermal diffusion: ***Total quantity of impurity Q_o (atom/cm²) is fixed***
  - Initial condition
    - $C(x,0)=0$
  - Boundary condition
    - $C(x,\infty)=0$
    - $\int_0^\infty C(x,t)dx = Q_o$
  - Solution to Fick's second law

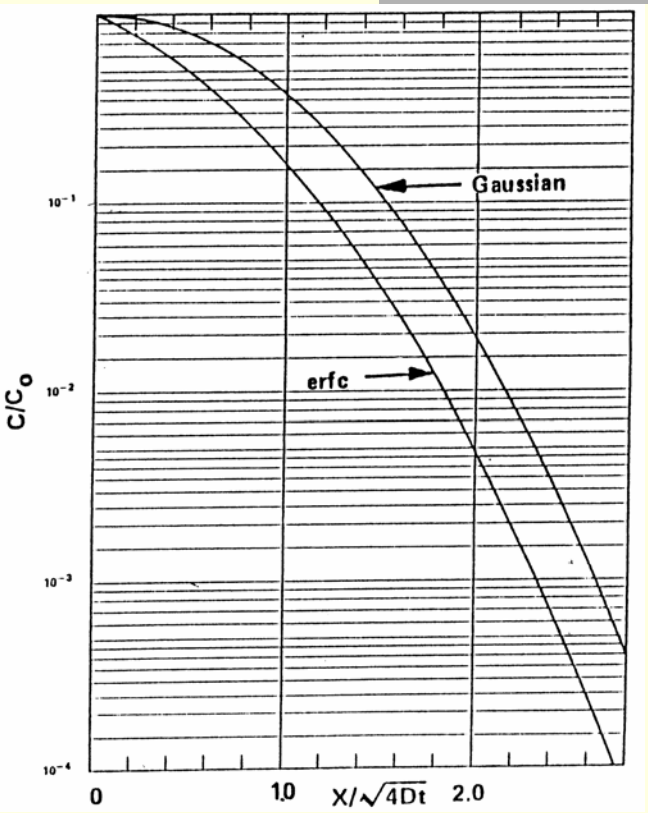
$$C(x,t) = \frac{Qo}{\sqrt{\pi Dt}} e^{\left[\frac{-x^2}{4Dt}\right]}$$

  - The surface concentration C_s is the above equation at x=0

$$C_s = C(0,t) = \frac{Q_o}{\sqrt{\pi Dt}}$$

  - The junction depth in this case is

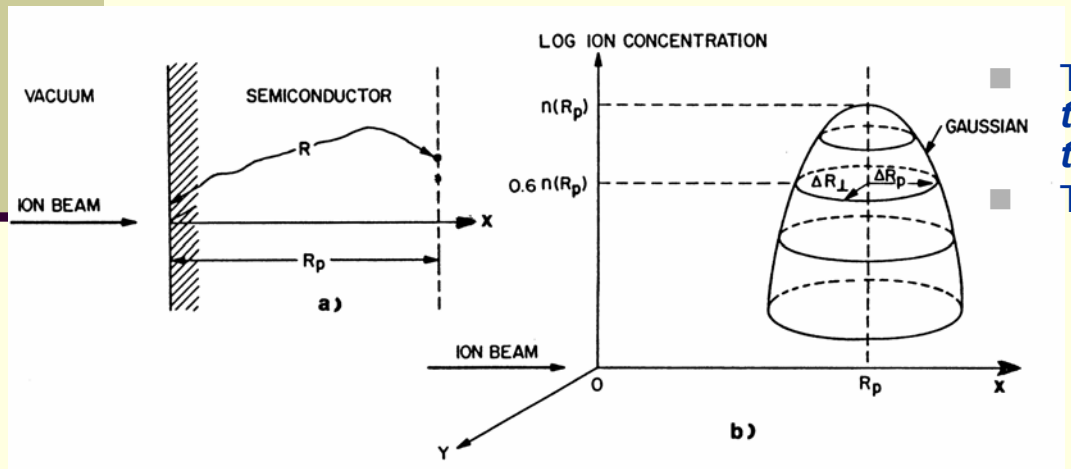
$$x_j = \left[4Dt \ln \frac{Q_0}{C_{sub}\sqrt{\pi Dt}} \right]^{\frac{1}{2}}$$



Source: Wolf, "Silicon Processing for the VLSI Era, Lattice Press, 1986

Ion Implantation

- Dopant ions bombarded into targeting substrate by high energy
- Ion implantation are able to place any ion at any depth in the sample
- Will produce crystal damage ⇒ can be eliminate by annealing at 700~1000°C
- Terms:
  - Projected range, **R_p**: *average distance traveled by ions parallel to the beam*
  - Projected straggle, **ΔR_p**: *fluctuation in the projected range*



Source: Wolf, "Silicon Processing for the VLSI Era, Lattice Press, 1986

- Dose, ϕ: the number of implanted ion per unit area (typically 10^{11}-10^{16} atoms/cm^2)

$$\phi = \frac{It}{q_i A}$$

- The concentration profile, to the first order is Gaussian

$$n(x) = \underbrace{\left(\frac{\phi}{\sqrt{2\pi}\Delta R_p}\right)}_{\text{peak concentration}} \exp\left[\frac{-(x-R_p)^2}{2\Delta R_p{}^2}\right]$$

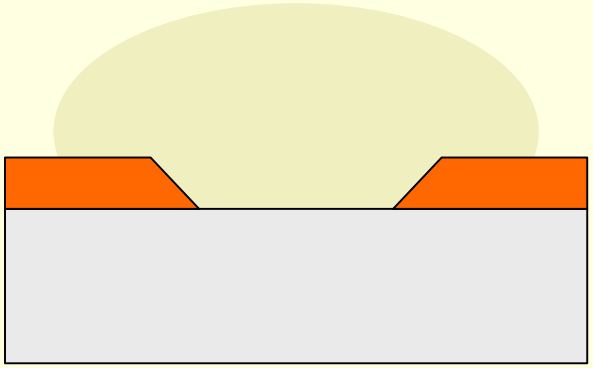
- The range is determined by: ***acceleration***, ***the ion mass***, and ***the stopping power of the material***
- The concentration is max. at x=R_p, then

$$n(x=R_p) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \cong \frac{0.4\phi}{\Delta R_p}$$

Diffusion vs. Ion Implantation

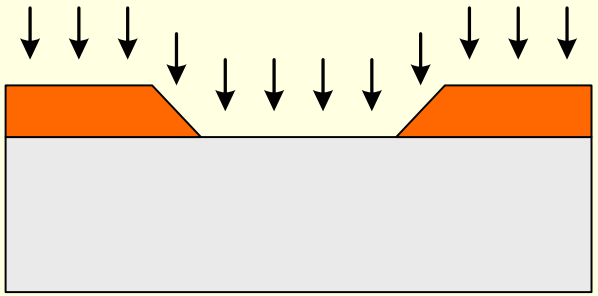
Diffusion

Furnace, 950~1280 C



Ion Implantation

Vacuum, Room Temp.



	Diffusion	**Ion Implantation**
Dopant uniformity and reproducible	±5% on wafer, ±15% overall	±1% overall
Contamination danger	High	Low
Environment	Furnace	Vacuum
Temperature	High	Low (Room Temp.)

Evaluation of Doping Process

- Sheet Resistance Measurement: 4-Point Probe
  - Sheet resistant, R_s, of the film can be described as

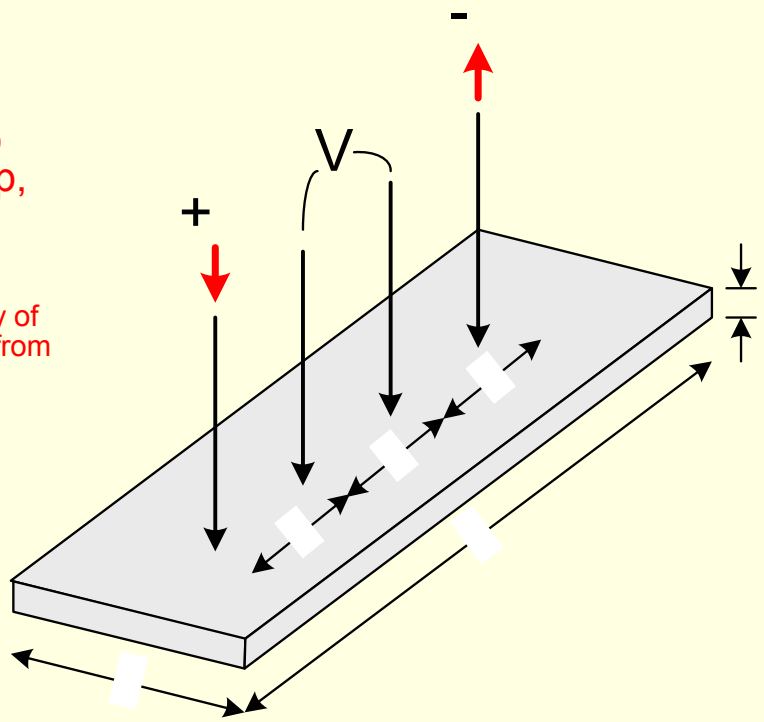
    $R_s(\Omega/\square)=\rho(\Omega\text{-cm})/x_j(cm)$

  - A current I is forced between outer two probes, then measure the voltage drop, V, between inner two probes

    $R_s=(V/I)F_1$

    F_1 is the correction factor depending on the geometry of the probes (specimen thickness, distance of probes from the edge to specimen

s/D	F_1	s/D	F_1
0	4.532	0.05	4.436
0.005	4.531	0.06	4.395
0.01	4.528	0.07	4.348
0.02	4.517	0.08	4.294
0.03	4.497	0.09	4.235
0.04	4.470	0.10	4.171



Source: Wolf, "Silicon Processing for the VLSI Era, Lattice Press, 1986

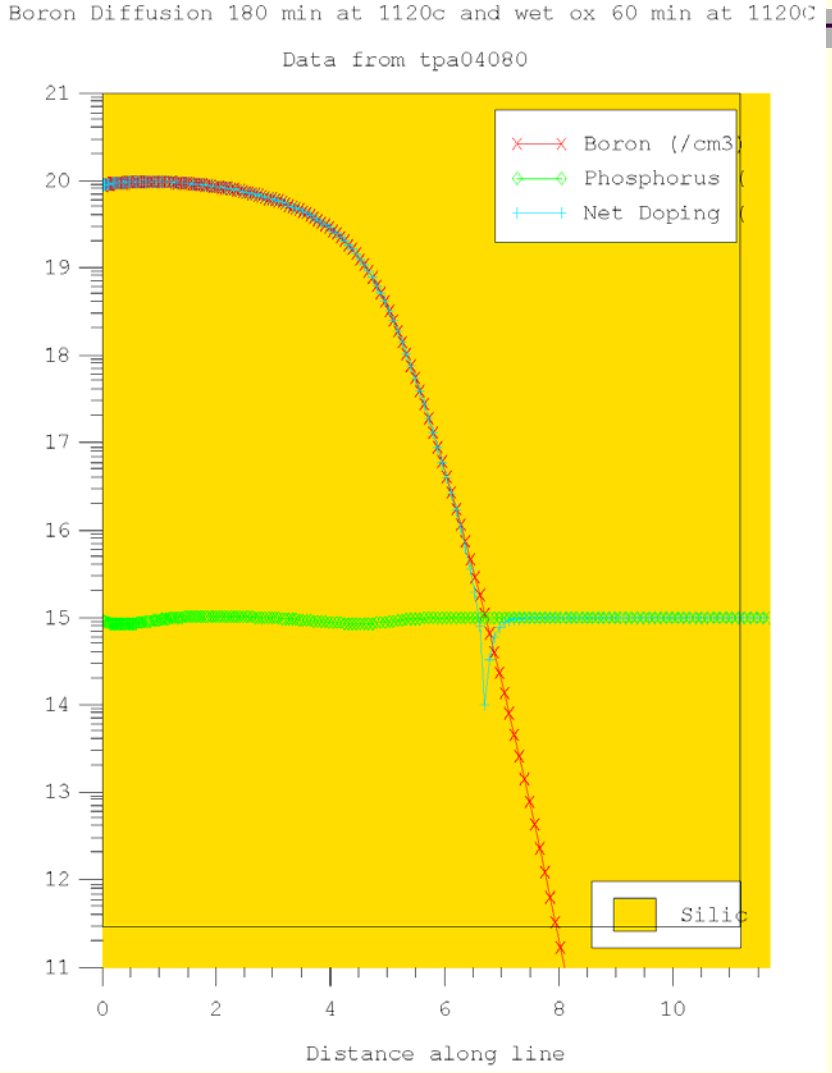
Tools For Simulation

- S-Suprem (Athena)
  - USD $ 2500 /2yrs for educational

SILVACO INTERNATIONAL

- Cheaper solution, use E*ECAD
  - USD $ 0.5 /use
  - www.eecad.com

E*ECAD



Additive Process

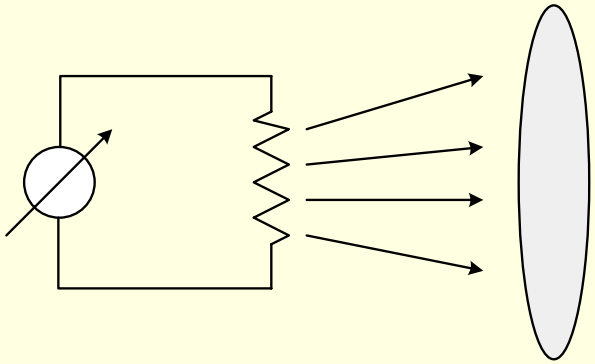
- Oxidation
- **Physical Vapor Deposition (PVD)**
- Chemical Vapor Deposition (CVD)

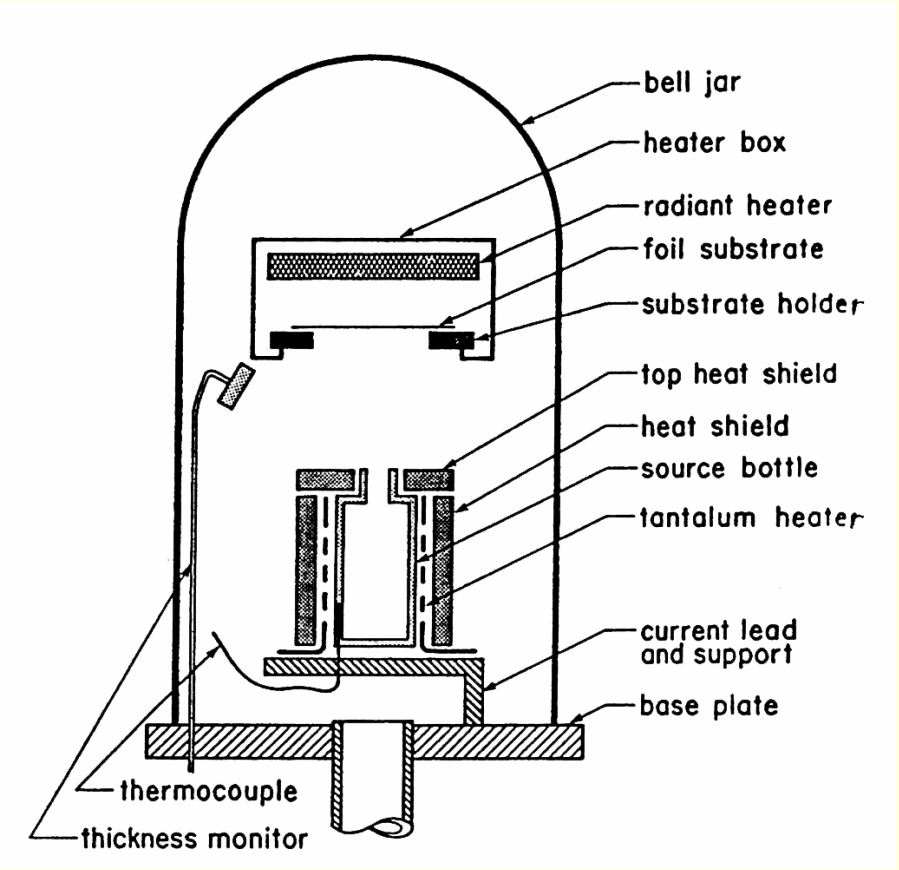
Physical Vapor Deposition (PVD)

- Thermal Evaporation
- Sputtering
- Molecular Beam Epitaxy (MBE)

Thermal Evaporation

- Achieve by sublimating of heated metal onto substrate



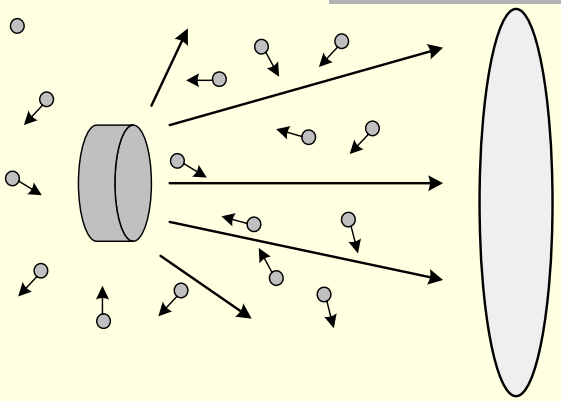


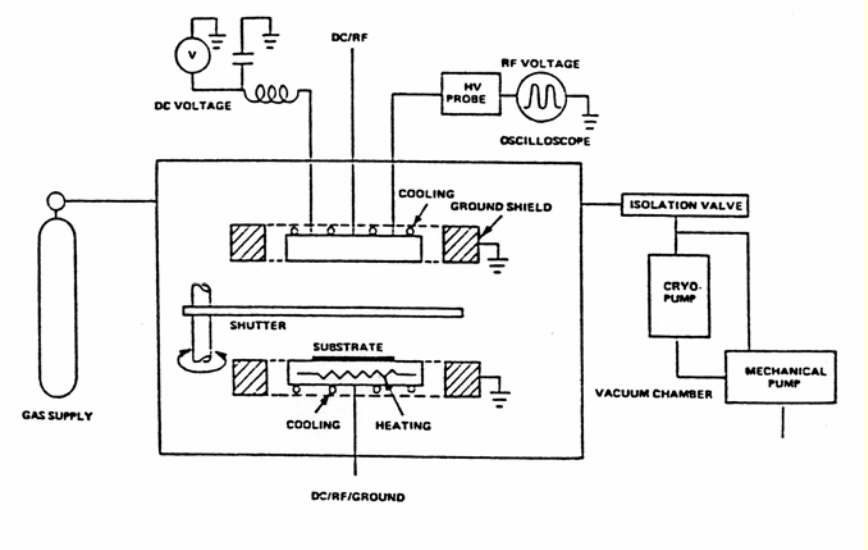
From: Madou, “Fundamentals of Micrfabrication” CRC Press, 1997

Sputtering

1. Sputtering was achieved by accelerated inert ion (Ar^+) by DC or RF drive in plasma through potential gradient to bombard metallic target

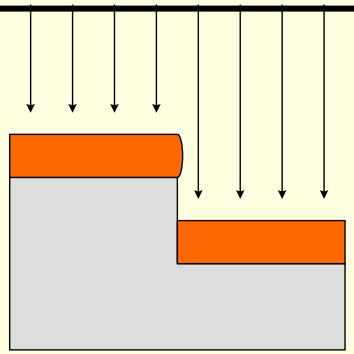
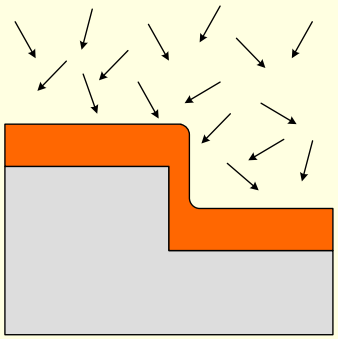
2. Then the targeting material is sputtered away and deposited onto substrate placed on anode





From: Wolf and Tauber, "Silicon Processing" Lattice Press,1986

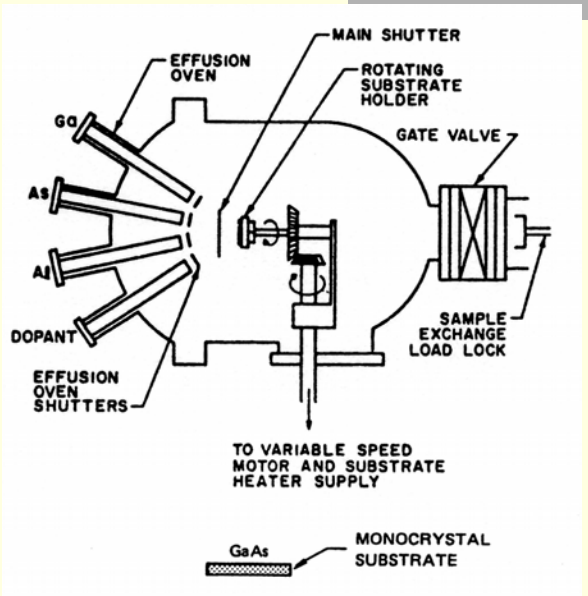
Comparison Between Thermal Evaporation and Sputtering

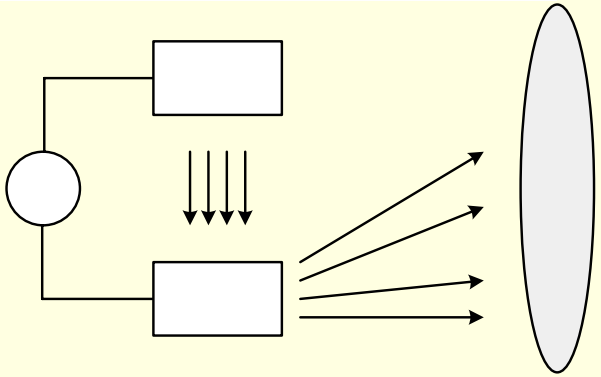
	Thermal Evaporation	Sputtering
Rate	Thousand atomic layers at a time	One atomic layer at a time
Choice of materials	Limited	Almost unlimited
Surface damage	Very low	Ionic bombardment damage
In-situ cleaning	Not available	Can be easily done
Adhesion	Poor	Good (on most materials)
Uniformity	Difficult to control	Easy to control
Film properties	Difficult to control	Can be controlled by pressure, bias, and temperature
Step Coverage		

Molecular Beam Epitaxy

- Streams of atoms from solid/gas source traveling through an ultra-high vacuum (10^{-11} Torr) to a heated single-crystal sample

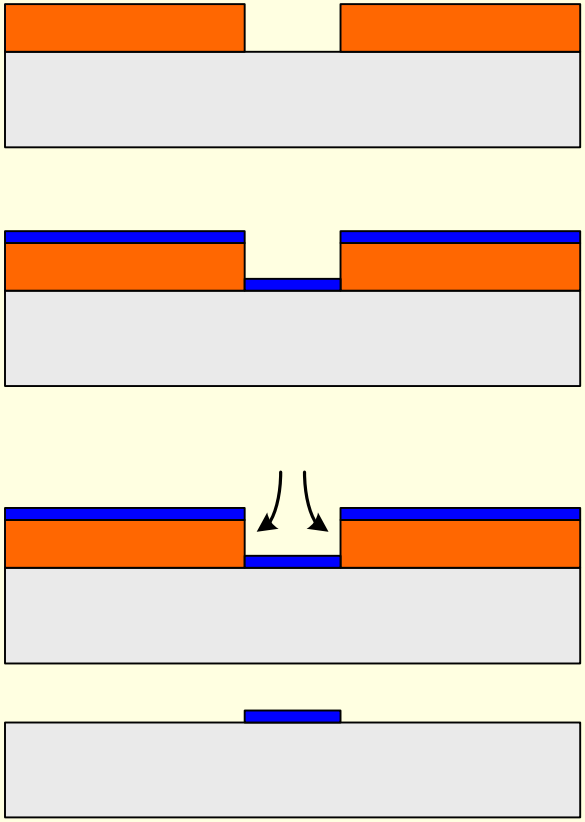
- Benefit:
  - Capable of depositing one monolayer at a time
  - Allows deposit stacks of monolayers from different materials
  - Precise control layer thickness and doping profile on a single atomic layer is possible



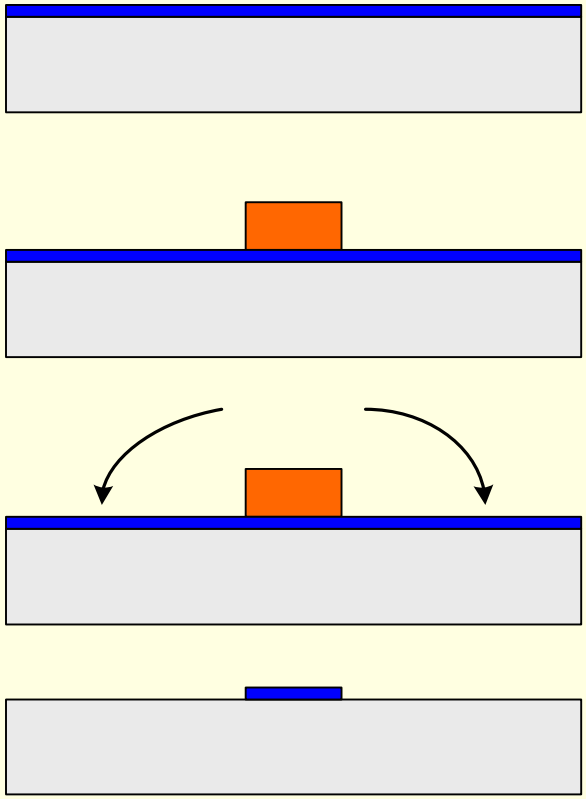


Patterning Metals

Lift-off Process



Wet etch Process



Additive Process

- Oxidation
- Physical Vapor Deposition (PVD)
- **Chemical Vapor Deposition (CVD)**
- Electrochemical Deposition

Chemical Vapor Deposition (CVD)

- Materials deposited via CVD
  - Polysilicon, silicon nitride (Si_3N_4), silicon oxide (SiO_x), silicon carbide (SiC), etc.
- How does CVD Work?
  - Gaseous reactants are introduced into chamber in elevated temperature
  - Reactant reacts and deposits onto substrate
- Types of CVD
  - LPCVD, APCVD, PECVD
- CVD results depend on pressure, gas, and temperature
  - Can be diffusion or reaction limited
  - Varies from film composition, crystallization, deposition rate, and electrical and mechanical properties

LPCVD Polysilicon

- Polysilicon can be used as resistor, conductor, Ohmic contacts to crystalline silicon, and mechanical structure

- Polycrystalline Silicon
  - $SiH_4 \rightarrow Si + 2H_2$
  - Typical deposition temperature: 600°C ~ 650°C
  - Microstructure and mechanical properties depend on deposition temperature and pressure
  - Can be *in situ*-doped,
    - n-type: arsine (AsH_3), phosphine (PH_3) $\Rightarrow$ Decrease doping rate
    - p-type: diborane (B_2H_6), $\Rightarrow$ Increase doping rate
    - Usually have large intrinsic stress (>500MPa) $\Rightarrow$ Needs annealing to reduce stress

Comparison of Material Properties of Si Single Crystalline with Poly Crystalline

Material Properties	Single Crystal Silicon	Polysilicon
Thermal Conductivity (W/cm°K)	1.57	0.34
Thermal Expansion (10^{-6}/°K)	2.33	2-2.8
Specific Heat (cal/g°K)	0.169	0.169
Piezoresistive Coefficient	n-Si (π_{11}=-102.2) p-Si (π_{44}=+138.1) Gauge factor of 90	Gauge factor of 30
Density (cm^3)	2.32	2.32
Fracture Strength (GPa)	6	0.8-2.84 (undope)
Poisson Ratio	0.262 max for (111)	0.23
Young's Modulus (GPa)	190	161

From: Madou, "Fundamentals of Micrfabrication" CRC Press, 1997

CVD Nitride

- Silicon nitride can be used as passivation layer for electronic devices, and can served as mask for selective etching (e.g. KOH and TMAH)

- Nitride often deposited by silane ($SiH_{4)}$ or dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) at 700~900°C
  - $3SiCl_2H_2+4NH_3 \rightarrow Si_3N_4+6HCl+6H_2$
  - Generally exhibit large tensile stress (1 GPa)
  - Stress can be reduced below 100 MPa if the film is silicon-rich

Comparison of Different CVD Nitride

- LPCVD Nitride
  - Stoichiometric (Pronunciation: "stoi-kE-O-'me-trik)Si_3N_4
  - High tensile stress, limits film thickness (can be improved by silicon-rich film)
  - Dense, good for mask or passivation layer
- PECVD Nitride
  - Non- stoichiometric
  - Low tensile stress, lower density

Subtractive Process

- Dry Etching
  - Dry Chemical Etching
  - Plasma-assisted Etching
  - Deep Reactive Ion Etching (DRIE)
- Wet Etching
  - Isotropic Wet Etching
  - Anisotropic Wet Etching
  - Electrochemical Etching

Subtractive Process

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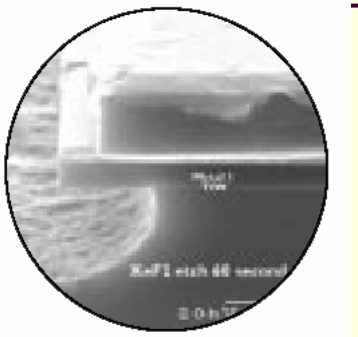
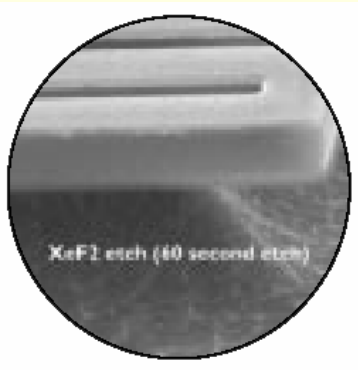
Dry Chemical Etching

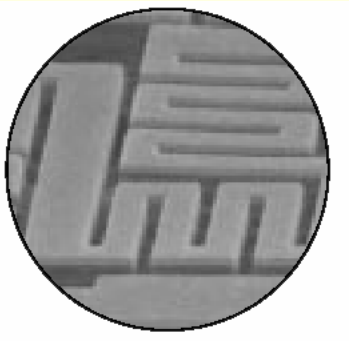
- HF Vapor Etching
- Xenon Difluoride (XeF_2) Etching
  - $2XeF_2+Si \rightarrow 2Xe+SiF_4$
  - Isotropic etching (typically 1-3μm/min)
  - Rough surface
  - IC compatible
  - Does not attack aluminum, silicon dioxide, and silicon nitride



Isotropic etching. The metal layer is bounded by two layers of TiW

Released MEMS Mesh.



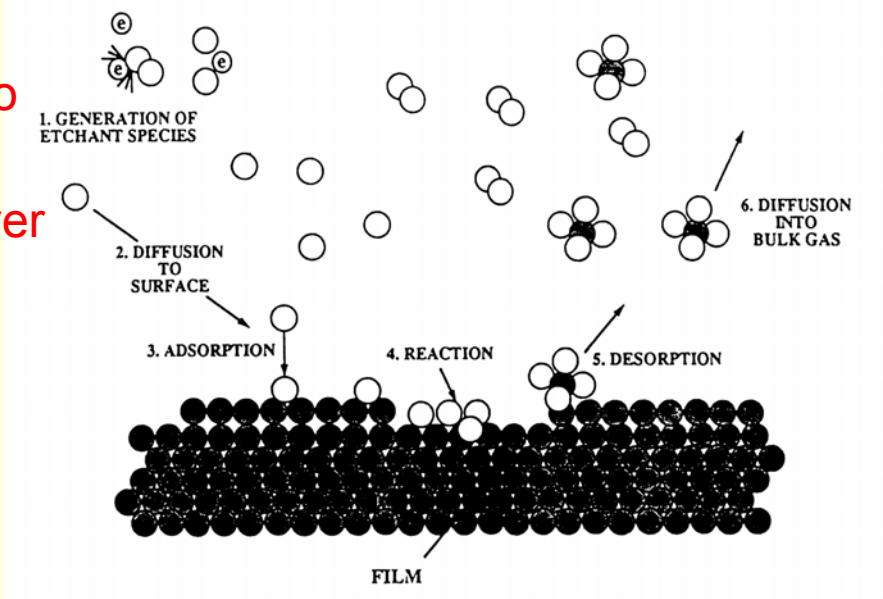


Undercutting of a metal/polysilicon resistor.

From: Xactix Inc. Pittsburgh, PA 15203

Plasma-Assisted Etching

- Reaction Mechanism
  1. Produce reactive species in gas-phase
  2. Reactive species diffuse to the solid
  3. Adsorption, and diffuse over the surface
  4. Reaction
  5. Desorption
  6. Diffusion
- Some gases for silicon etch: SF_6/ C_2ClF_5 (Freon^{TM} 115), Cl_2/$CClF_3$ (Freon^{TM} 13), H_2/CF4 (Freon^{TM} 4)



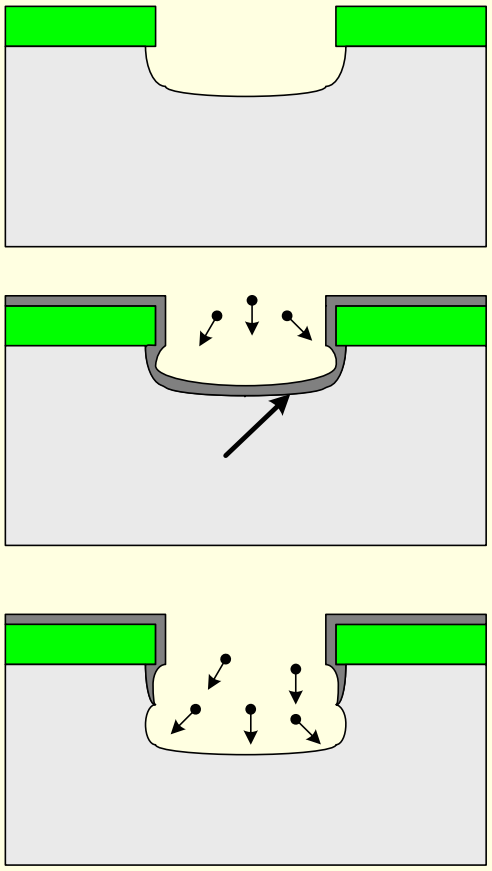
Schematic of plasma etch process

From: Madou, "Fundamentals of Micrfabrication" CRC Press, 1997

Deep Reactive Ion Etching (DRIE)

- A very high-aspect-ratio silicon etch method (usually > 30:1)
- BOSCH Process (1.5 - 4 μm/min)
  - SF_6 to etch silicon
  - ~10nm flourcarbon polymer (similar to Teflon) is plasma deposited using C_4H_8
  - Energetic ions (SF_x^+) removed protective polymer at the bottom trench

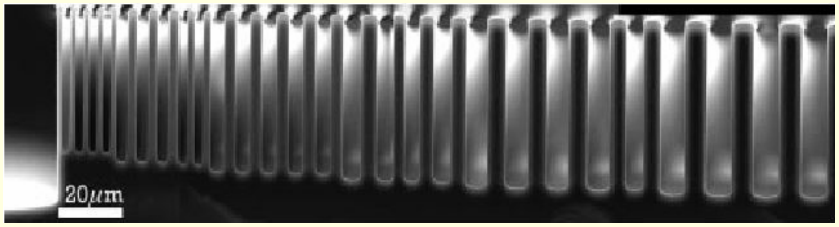
BOSCH Process



Deep Reactive Ion Etching (DRIE)

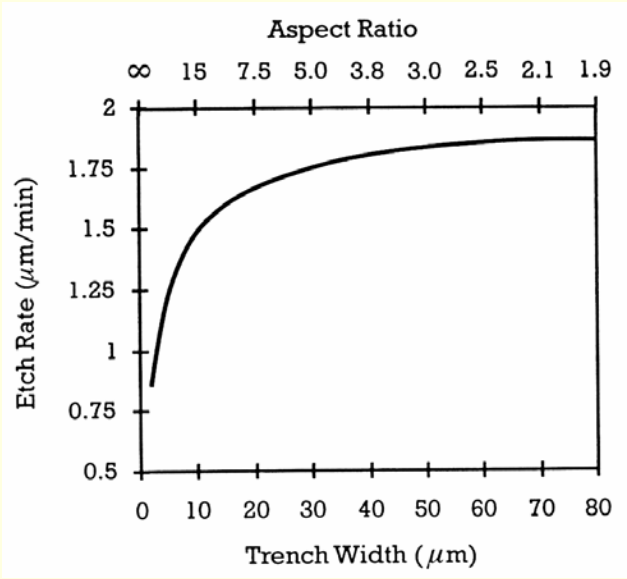
(continue...)

- Etch rate of DRIE Process limited by the aspect ratio of the trench



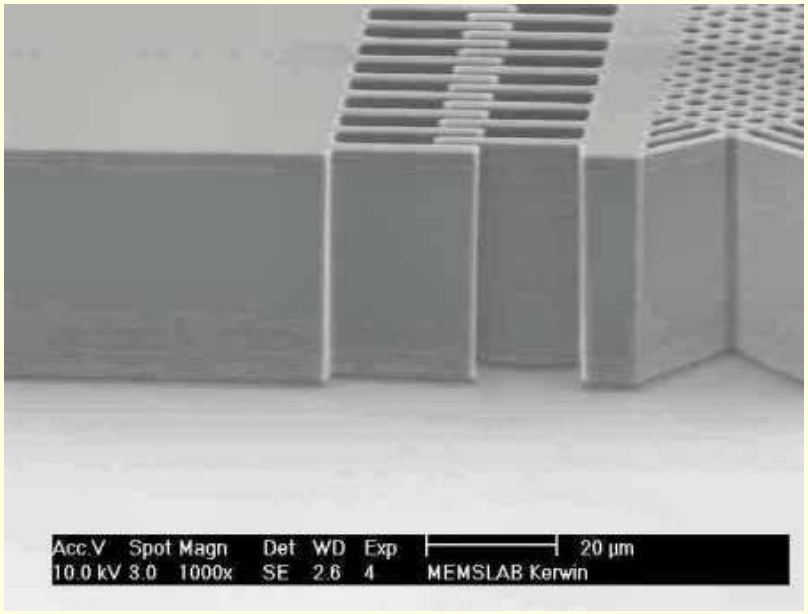
Aspect Ratio-Dependent Etching (ARDE) in DRIE
From: Maluf, "An Introduction to MEMS Engineering" Artech House (2000)

- Cryogenic Process
  - Wafer cooled to cryogenic temperature (~77K by LN_2)
  - The etchant gas itself then condenses on the sidewalls (SiO_xF_y), protecting them from being etched

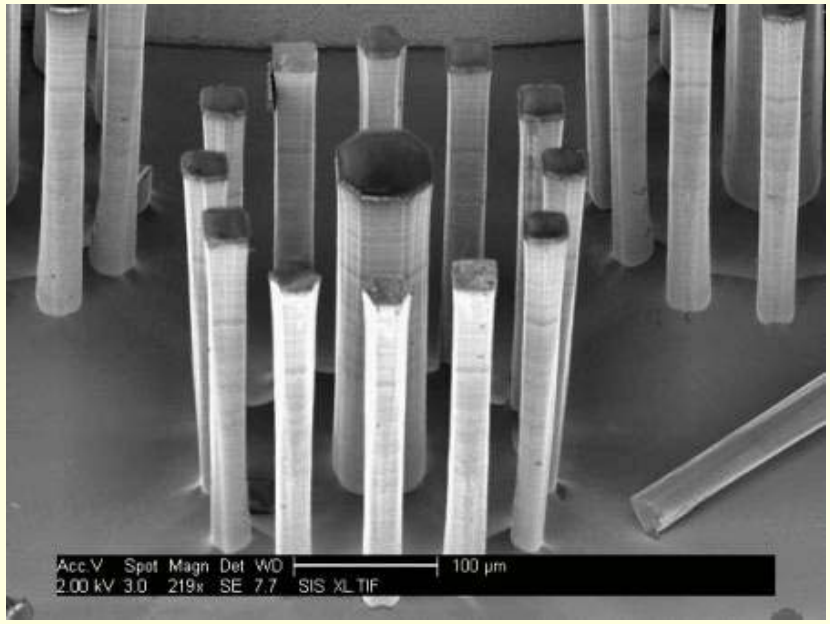


Etch rate dependence on feature size and aspect ratio
From: Maluf, "An Introduction to MEMS Engineering" Artech House (2000)

Deep Reactive Ion Etching (DRIE)



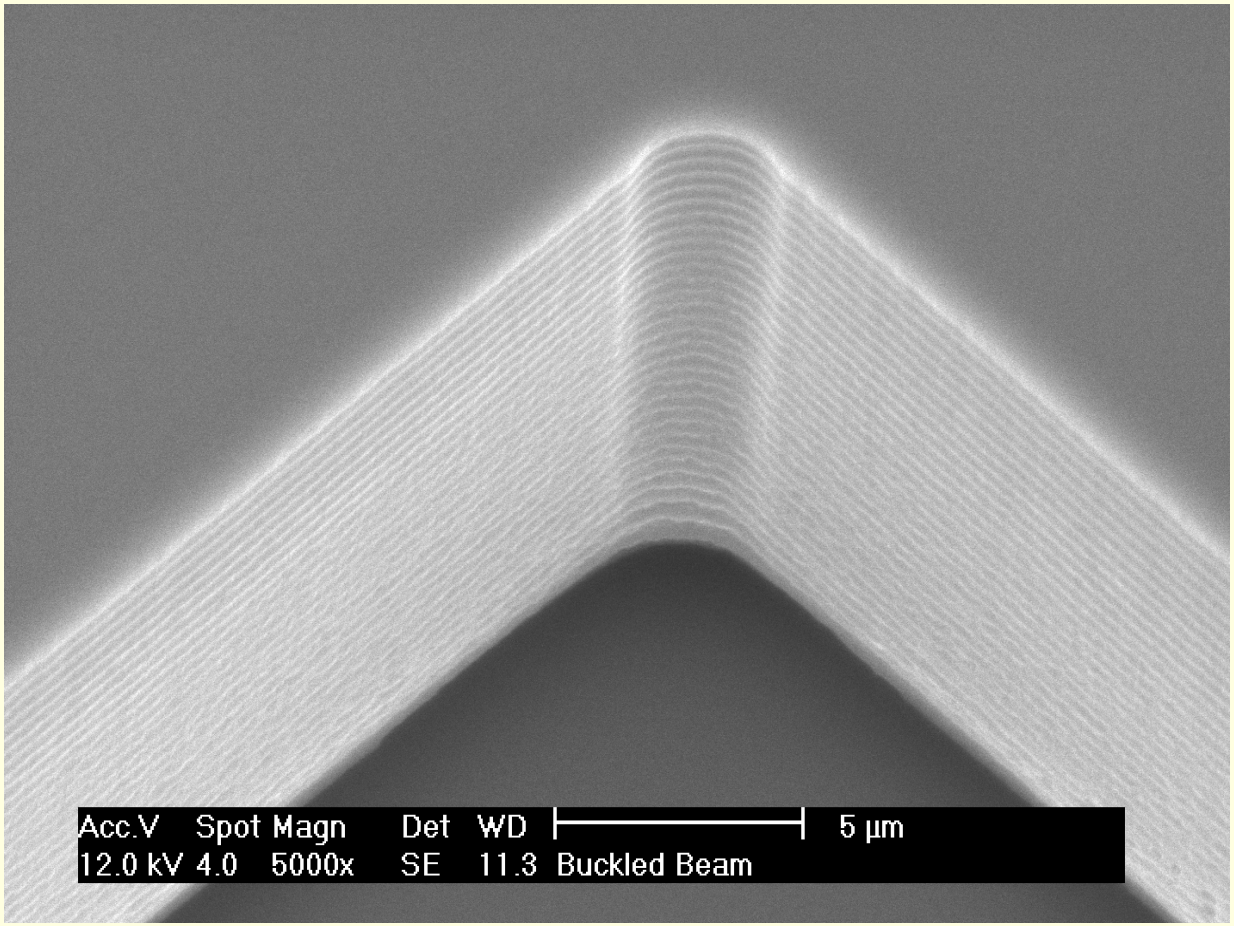
Side view of a comb structure etched with the DRIE



DRIE etched pillars. Central pillars diameters are 70- μ m and outer pillar diameters are 20- μ m

Photo Source: Washington Technology Center
http://microfab.watechcenter.org/photos/photos.asp

Deep Reactive Ion Etching (DRIE)



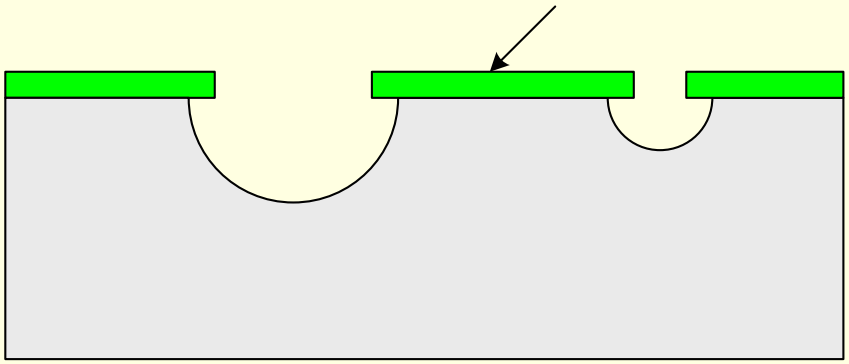
DRIE by Bosch process, Courtesy of Jun Guo, CWRU

Subtractive Process

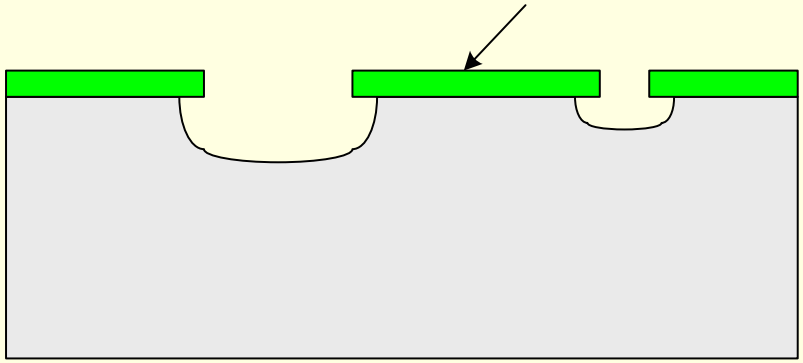
- Dry Etching
  - Dry Chemical Etching
  - Plasma-assisted Etching
  - Deep Reactive Ion Etching (DRIE)
- Wet Etching
  - Isotropic Wet Etching
  - Anisotropic Wet Etching
  - Electrochemical Etching

Isotropic Wet Etching

- Isotropic etchants etch in all direction at nearly the same rate
- Commonly use chemical for Si: HNA (HF/HNO_3/Acetic Acid)
  - A mass transfer limited reaction $\rightarrow$ needs stirring
  - $18HF+4HNO_3+3Si \rightarrow 2H_2SiF_6 +4NO_{(g)} +8H_2O$



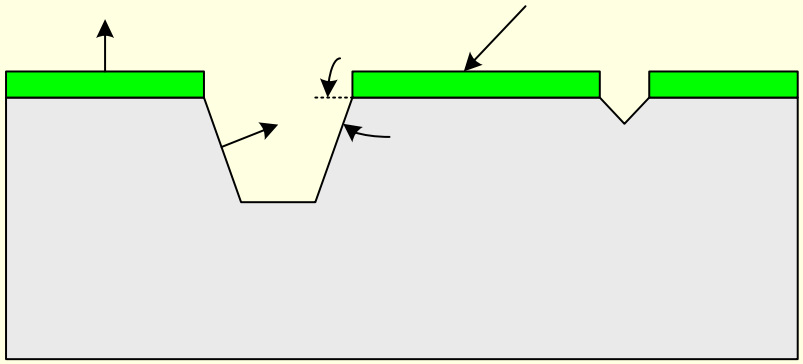
Isotropic etching: with agitation

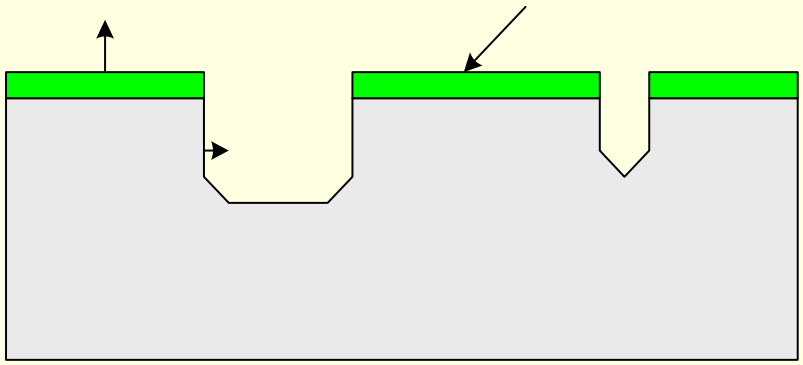


Isotropic etching: without agitation

Anisotropic Wet Etching

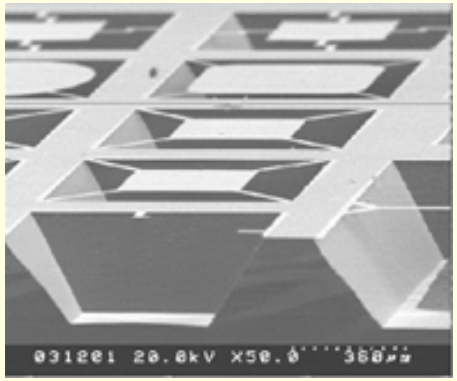
- Anisotropic etchants etch much faster in one direction than in another
- Alkali Hydroxide Etchants (KOH, NaOH, CeOH, RbOH,..)
  - Silicon (s) + Water + Hydroxide Ions → Silicates + Hydrogen
- Example: KOH on silicon
  - Slower etch rate on (111) planes: fewer dangling bonds
  - Higher etch rate on (100) and (110) plan (400 times more faster than the (111) plane)
  - Typical concentration of KOH is around 40 wt%





Anisotropic Wet Etching (cont.)

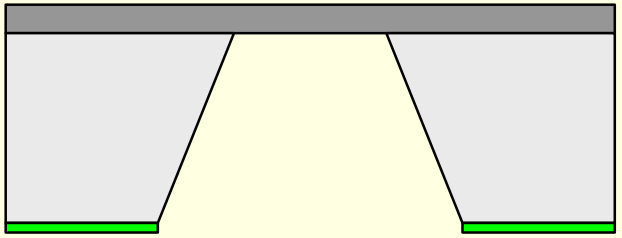
- TMAH (tetramethyl-ammonium hydroxide), $(CH_3)_4NOH$
  - Surface morphology is rougher
  - Etch rate and surface roughness decrease as the TMAH concentration is increased
  - Si can be dissolved in TMAH and lower pH $\Rightarrow$ increase selectivity toward aluminum but increase surface roughness
  - Etch-stop selectivity can be improved by adding isopropyl alcohol
- EDP (ethylene diamine pyrochatechol)
  - Selectivity toward P+ doping is higher but selectivity on the (100):(111) is only 35
  - EDP mixture are very corrosive and carcinogenic (causing cancer)!!!

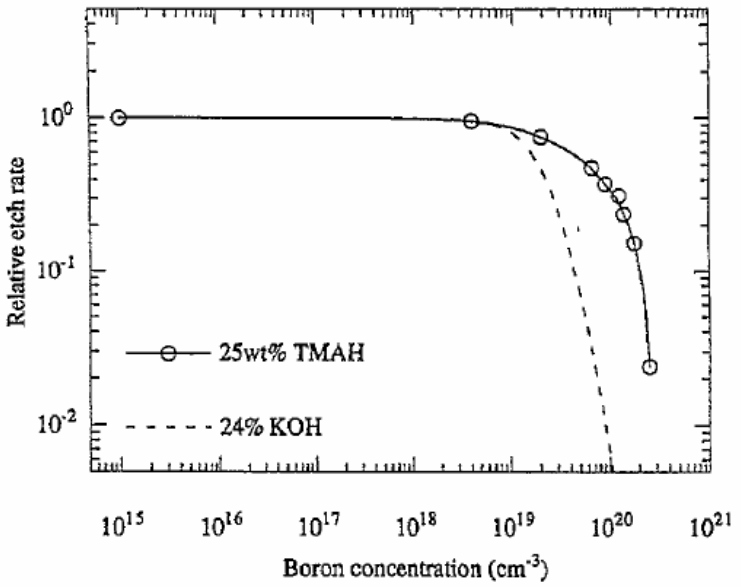


From: ITRI, Micromchined floating plates
http://www.itri.org.tw/mems/english/research/mt101.htm

Etch Stop

- Boron Etch Stop
  - Etch rate greatly decreased at highly P^+ doped silicon
  - P^+ layer can be create by gaseous or solid boron diffusion
  - Can be used with EDP, TMAH, and KOH-type etchant

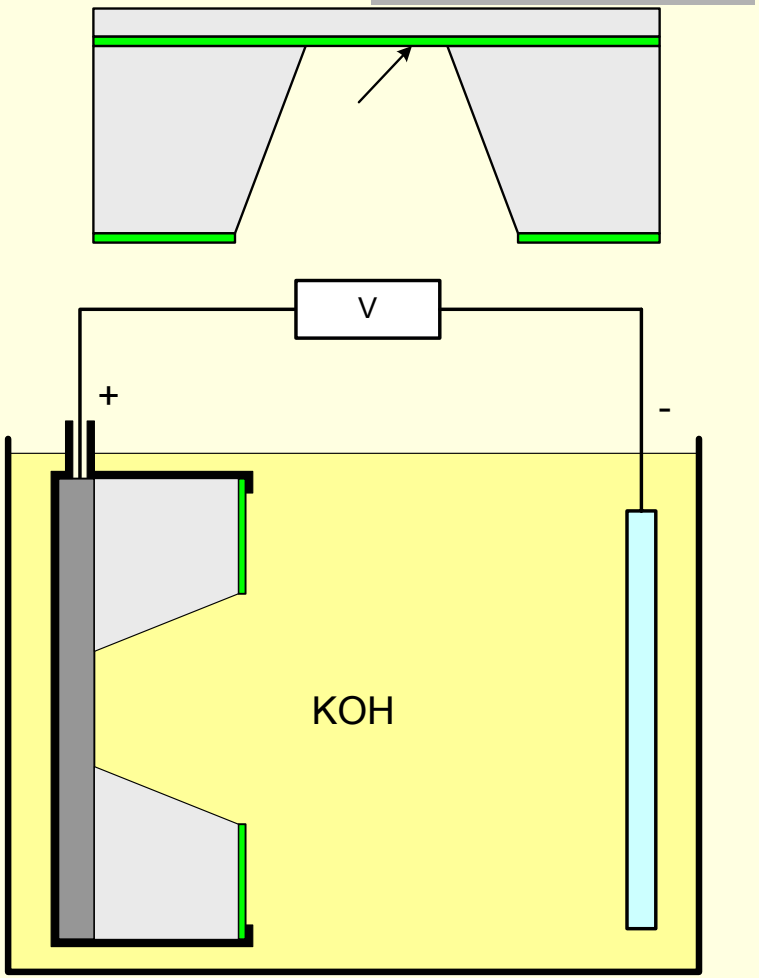




Steinsland et al. “Boron etch-stop in TMAH solution”, Sensors and Actuators, A 54 p728-732 (1996)

Etch Stop (cont.)

- Insulator Etch Stop
  - Etch stops at insulator layer (e.g. SiO_2)
  - Using SOI wafer to eliminate doping step, electronic devices can be fabricate on Si epi-layer
- Electrochemical Etch Stop
  - p-type Si is etched away in echants (KOH, EDP, TMAH)
  - Formation of SiO_2 by anodic oxidation when the etchant reaches the junction
  - Etch-rate drop equivalent to the selectivity over SiO_2



Comparison of Selected Silicon Etchants

	HNA	Alkali-OH	EDP	TMAH	XeF_2	SF_6	DRIE
Etch Type	wet	wet	wet	wet	Dry[1]	dry	dry
Anisotropic?	no	yes	yes	yes	no	varies	yes
Si etch rate (μ m/min)	1 to 3	1 to 2	1 to 30	≈ 1	1 to 3	≈ 1	> 1
Si roughness	low	Variable[2]	low	Variable[2]	High	variable	low
Al selective	no	no	no[3]	yes[4]	yes	yes	yes
Au selective	likely	yes	yes	yes	yes	yes	yes
Nitride etch (nm/min)	low	low	low	1 to 10	NA	low	low
Oxide etch (nm/min)	10 to 30	1 to 10	1 to 80	1	low	low	low
P^+ etch stop	no	yes	yes	yes	no	no	no
CMOS compatible?	no	no	yes	yes	yes	yes	yes
Cost	low	low	moderate	moderate	moderate	high	high
Safety	moderate	moderate	low	high	moderate	high	high

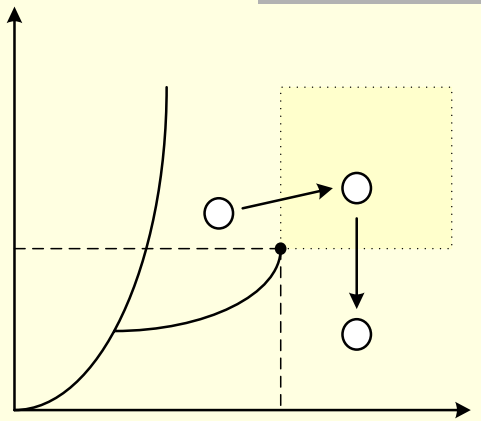
1 Sublimation from solid source
2 Varies by concentration and temperature
3. Some formulation of EDP does not attack Al
4 Can be control by adding Si, polysilicice acid or pH control

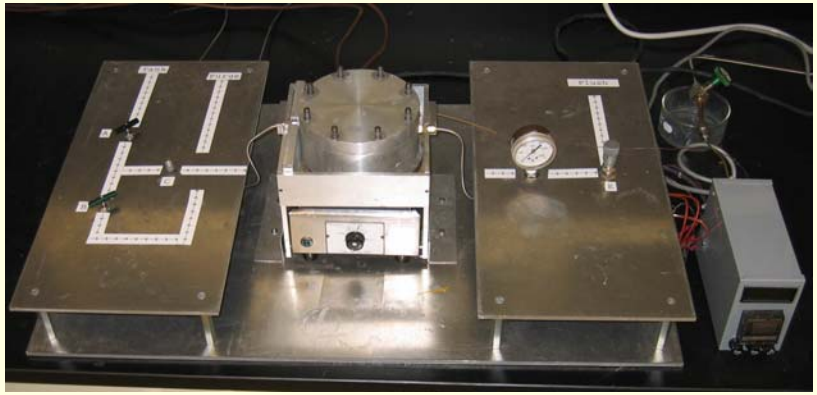
From Kovac, "Micromachined Transducers Source Book", McGraw-Hill, 1998

Supercritical Release

- To prevent sticking problem of releasing polysilicon structure from LTO sacrificial layer (Mulhern; 1993)

- Release steps:
  1. LTO sacrificial layer was HF etched and rinsed in DI water without air dry
  2. Water was exchanged with methanol by dilution
  3. Transfer to pressure vessel
  4. Methanol replaced by liquid CO_2 at 25°C in 1200 psi
  5. Heat the chamber to 35°C and vent CO_2 at 35°C



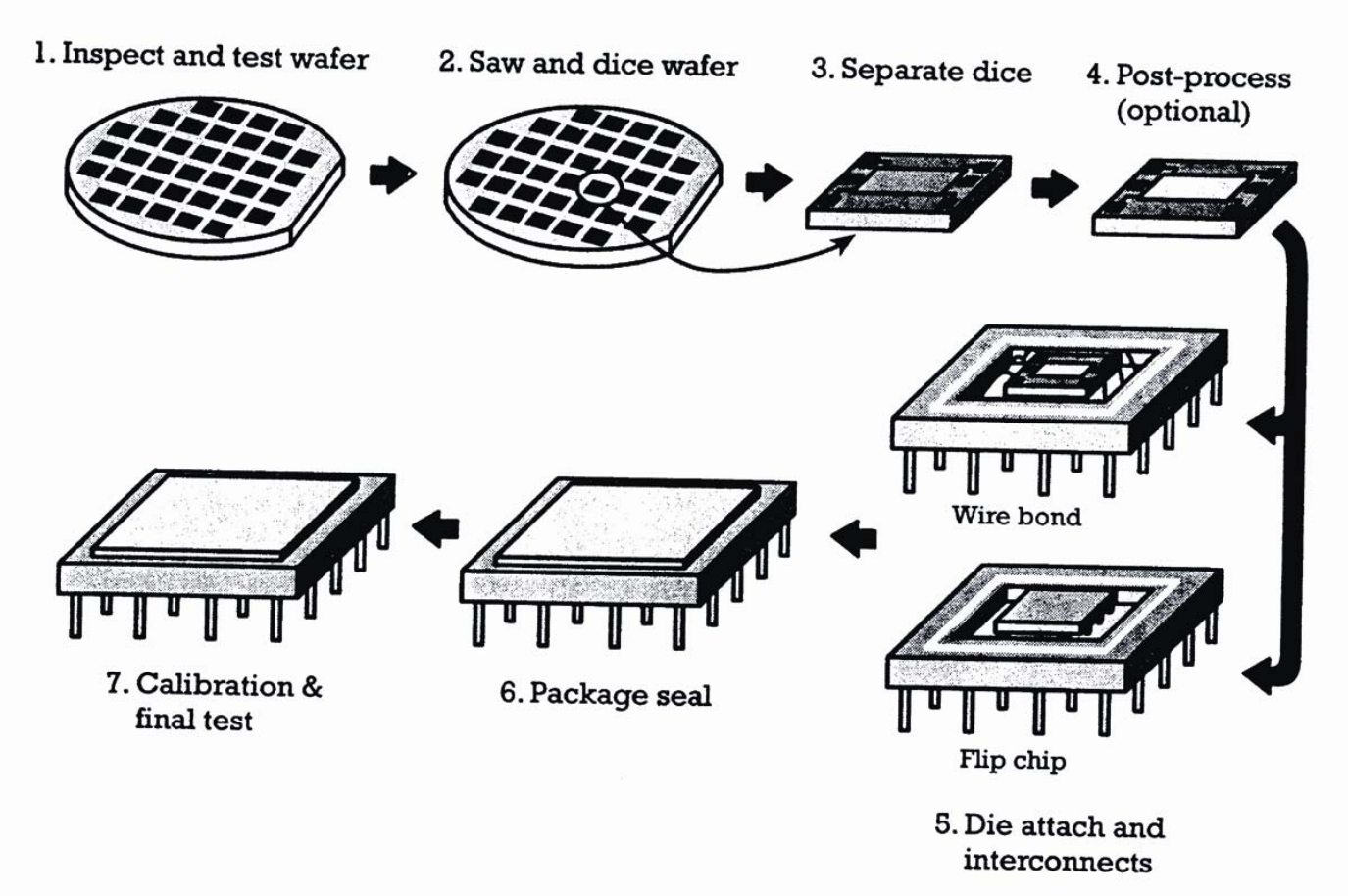


CWRU Supercritical release setup

Packaging

- More the 70% of sensor cost determined from packaging!
- Packaging involves:
  - Bonding
  - Wafer scribing
  - Lead attachment
  - Encapsulation in protective body ($$)
  - Testing: include leak test and electrical integrity ($$)

Simplified Process Flow for MEMS Packaging



Source: Maluf, "An Introduction to Microelectromechanical Systems Engineering" Artech House Publishers, 2000

Functions for Packaging

- Packaging provides at least 4 functions:
  - Signal redistribution
    - Redistribute electrical contacts from IC over a larger, more manageable surface $\Rightarrow$ fan out the electrical path
  - Mechanical support
    - Provide rigid support, stress release and protection from environment
  - Power distribution
    - Similar to signal redistribution, but more robust
  - Thermal management
    - Support adequate thermal transport to sustain operation for the product lifetime

Packaging Technologies

- Wafer Bonding
- Wafer Dicing
- Thermal Management
- Stress Isolation
- Protective Coating
- Hermetic Packaging
- Die Attach Process
- Wiring and Interconnection
- Types of Packaging Solutions

Packaging Technologies

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Wafer Bonding

- Silicon Fusion Bonding (Direct Wafer Bonding)
- Anodic Wafer Bonding (Field-Assisted Bonding)
- Intermediate-Layer Bonding
  - Eutectic Bonding
  - Adhesive Bonding
  - Solder Bonding

Why Wafer Bonding?

- Complex Structures
  - SOI Wafers
  - Multi-wafer stacked structure
  - Fluidic channels
- Enclosed Cavities
  - Pressure sensor
  - Vacuum sealing

Silicon Fusion Wafer Bonding

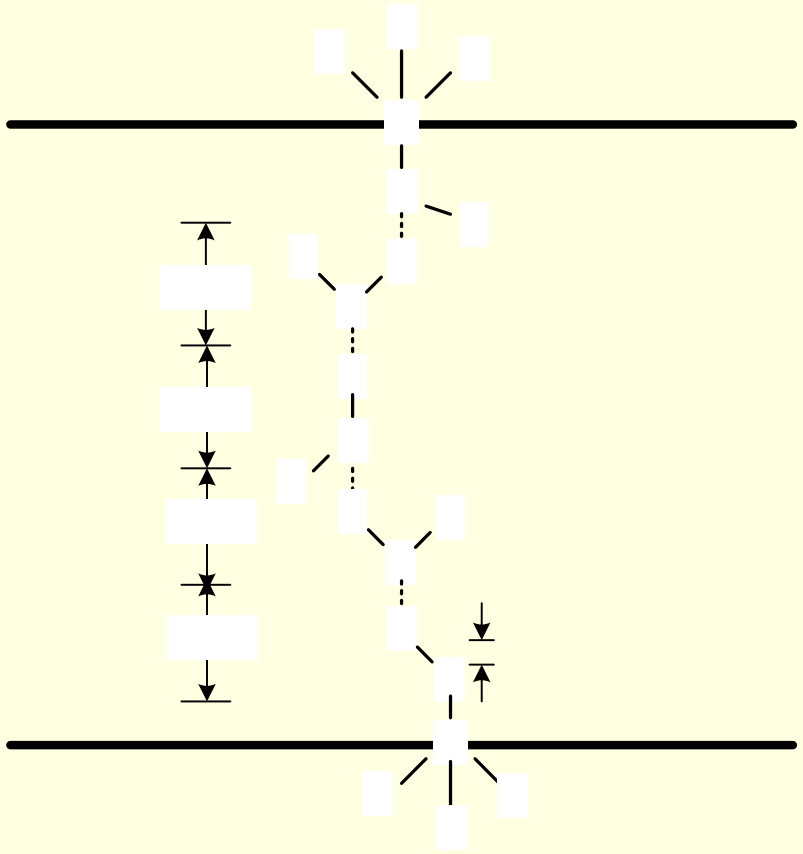
- Bonding steps
  - Make two bonding surface hydroxyl $\Rightarrow$ hydrophilic
  - Hydrogen bonds formed when wafers contacts and held initially
  - Bonding reaction occurs at room temperature
  - Annealing above 1000 °C to strengthen the bond

Hydrophilic Silicon Surface

- A hydrous thin oxide (native oxide) is strained oxide and highly reactive, it react readily with water to form Si-OH (silanol) groups on its surface
- OH groups are strongly polarized, they can form hydrogen bridge bond with water (that cause Si surface hydrophilic after RCA1)
- If thermal oxide covered on top of Si, during RCA cleaning, water and OH ions can also break the Si-O-Si (siloxane) bonds of the oxide and form Si-OH group
- The Si wafers with hydrophilic surface can bond spontaneously at room temperature

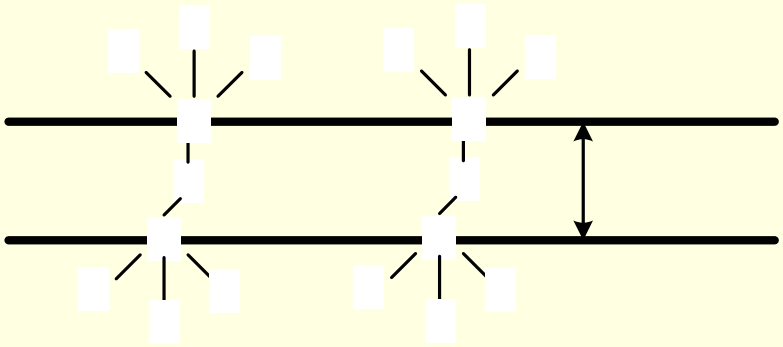
Mechanism for Wafer Bonding:
Room Temperature Bonding

- Van der Waals Interactions
  - Originated from atomic and molecular electric dipole whose orientations are correlated in such a way that they attract each other
- If hydrogen bonding can be realized across 2 mating surfaces, it will result in strong dipole-dipole Van der Waals attraction forces between these surfaces
- If silicon surface is hydrophilic and water molecules are present with separation of 10 Å, the linkages of 2 or 3 water molecules may bridge the gaps of 2 mating surfaces at room temperature



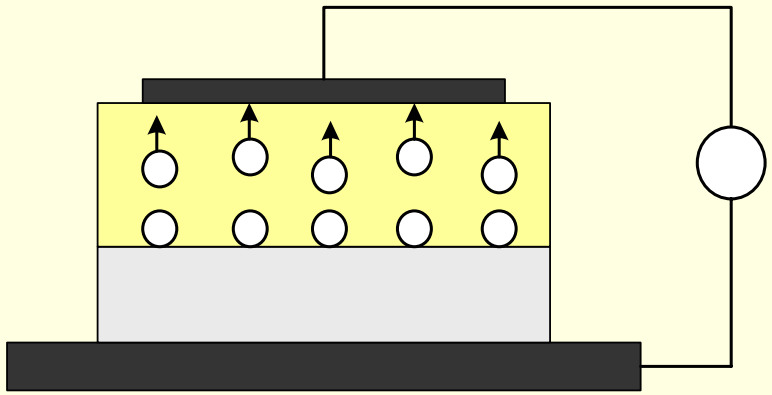
Mechanism for Wafer Bonding:
Annealing

- Hydrogen bond (0.1-0.4 eV) is weaker than Si-Si (1.9 eV) and Si-O (4.5 eV) bonds
- For Si/Si bonding pairs, annealing at 800 °C viscous flow of native oxide will fill up interface gap to increase contact area and forms siloxane (Si-O-Si) bonds to increase bonding strength
- For Si/SiO_2 and SiO_2/SiO_2 bonds, thermal oxide is less strained and has lower water concentration, annealing above 1000 °C would be necessary to introduce SiO2 mass transport and viscous flow at bonding interface



Anodic Wafer Bonding

- Bonding procedure:
  1. Heat the substrate to 300-500°C
  2. Apply high voltage (500-1500V) across two substrates
  3. Sodium ions (Na+) migrate away from the silicon-glass interface toward cathode leaving behind fixed negative charges
  4. The electrostatic attraction holds two substrate together and formed chemical bonding



Bonding Issues

- Geometry Issues
  - Surface energy reduced when wafer bonded
  - Flatness:
    - Wafer will bend if the surface is not flat $\Rightarrow$ Increase strain energy
    - Wafer pairs will bond until the reduction of surface energy equals strain energy cost
  - Wafer thinning could reduce strain energy

- Cleanliness Issues
  - Wafer cleaning prior bonding (reverse RCA cleaning)
    - Interval time should be as short as possible
  - Avoid particulate contamination:
    - Will create void in the bonded region
    - Void will amplify by wafer stiffness and heat treatment
    - e.g. 1 μm incompressible particle in 4" dia., 525 μm-thick wafer bonding will leads 0.5 cm unbond area

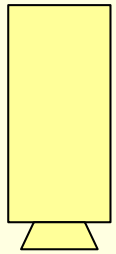
An example: 3C-SiC-on-Insulator by Wafer Bonding

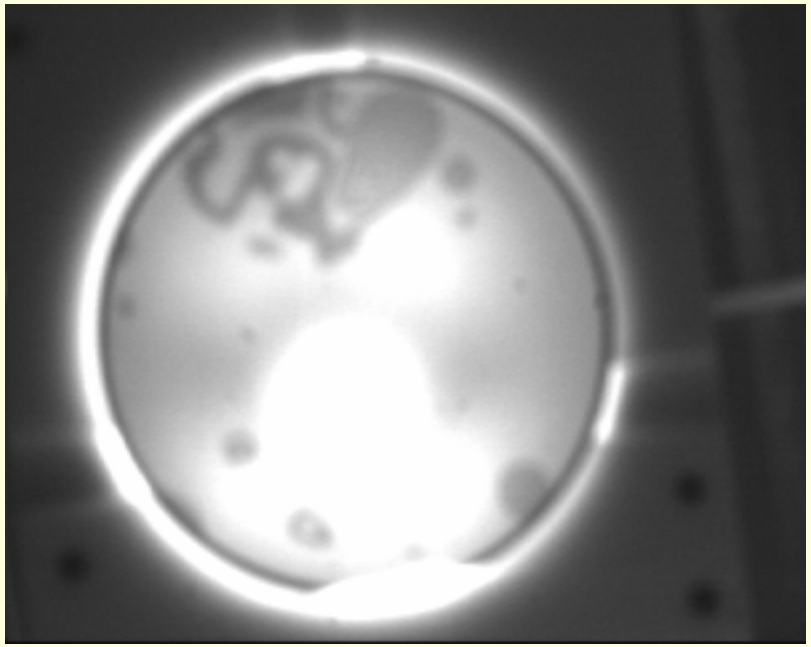
Intermediate-Layer Bonding

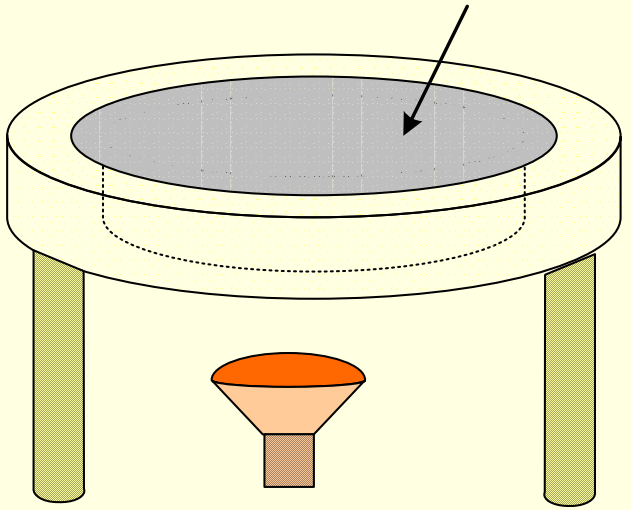
- Thermocompression Bonding (Eutectic Bonding)
  - Use gold layer and apply heat and pressure
  - Eutectic temperature for Au-Si alloy: 363°C
  - High bonding strength: 148 MPa (compare to fusion bonding of 5-15 MPa)
- Polymeric Adhesives
  - Polyimides
  - Silicons
  - Epoxy resins

Bonding Result Inspection

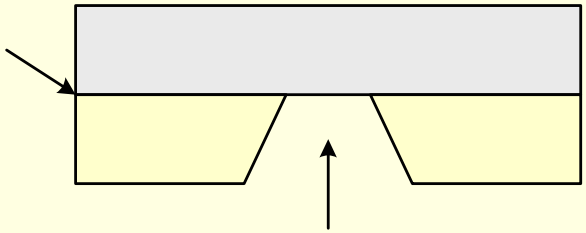
- Silicon in transparent in infrared spectrum ⇒ Can use infrared light for inspection



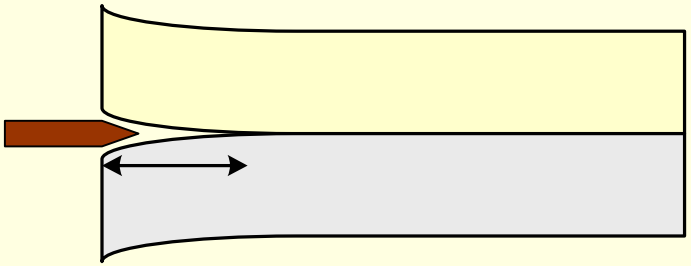




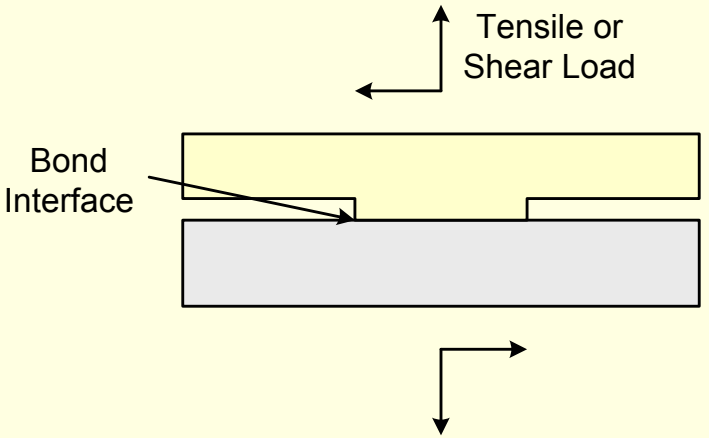
Bonding Strength Test

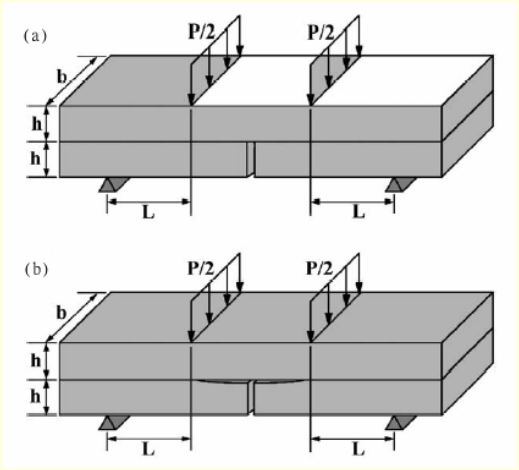


Burst Test



Maszera Test



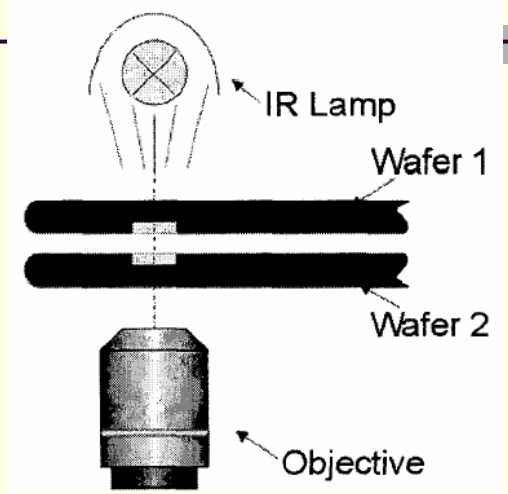


Tensile and Shear Test

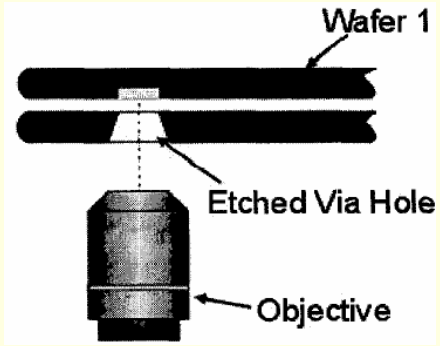
Ayón et al, Sensor and Actuator, A, Vol. 103 (2003) p1-8

Alignment for Wafer Bonding I

- **Infrared Alignment**
  - Silicon in transparent in infrared spectrum ⇒ Can view both wafers and align to each other
  - Limitation:
    - Require double side polished wafer
    - Diffraction effect associate with IR imaging ⇒ Large alignment error (± 5μm)



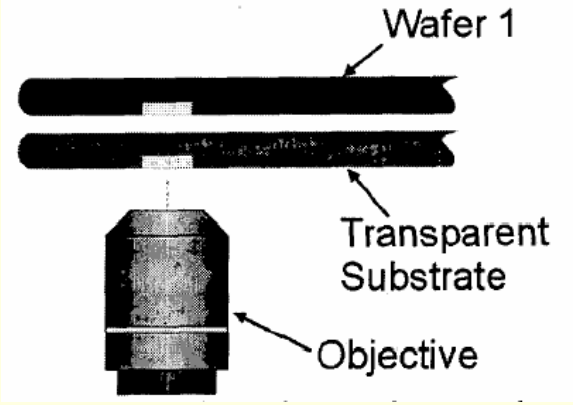
- **Through Wafer Via Holes**
  - Etch a via hole on one wafer to see through the other wafer's registration mark
  - Limitation:
    - Large alignment error (can not use in micron level alignment)



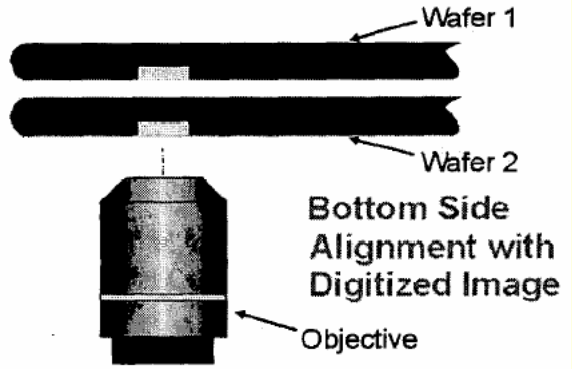
Mirza et al, 2000 Proc. of the 50th Electronic Components and Technology Conf. p676-680

Alignment for Wafer Bonding II

- **Transparent Substrate**
  - One of the substrate is transplant (e.g. glass)
  - Very high alignment precision
  - Can be use in chip-scale packaging and I/O fan out packaging
  - Limitation: Does not fit all cases



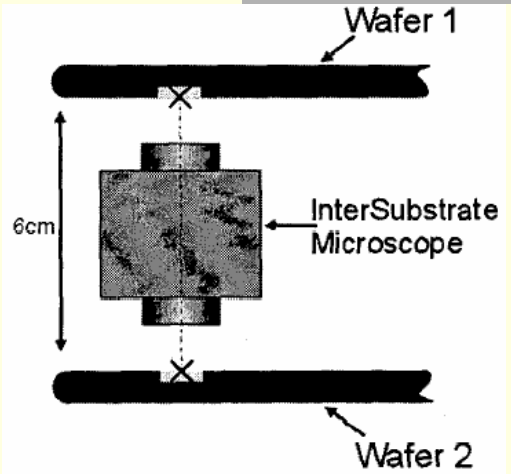
- **Backside Alignment**
  - Currently industry standard for wafer bonding alignment
  - Place alignment keys on the back side of one wafer, then align to the first wafer
  - Limitation:
    - Alignment error in the order of 1 μm
    - Not desire for CMOS application to place the alignment marks on the backside



Mirza et al, 2000 Proc. of the 50th Electronic Components and Technology Conf. p676-680

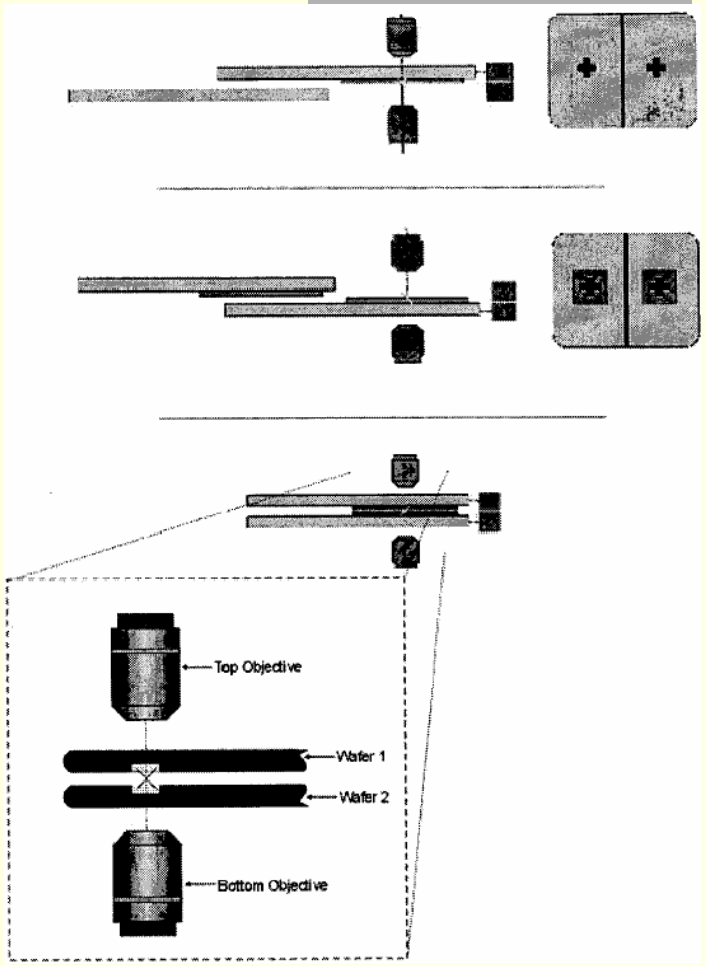
Alignment for Wafer Bonding III

- **Intersubstrate Alignment**
  - Adopt from flip chip technology
  - Special microscope inserted between wafers to align both wafers
  - Microscope retracted, two wafers bond together
  - Limitation:
    - Long-term mechanical precision required



Alignment for Wafer Bonding IV

- **SmartView™ Alignment**
  - Each microscope observe one alignment key on the wafer, then store electronically
  1. Top wafer out, alignment key store by bottom microscope, then retract
  2. Bottom wafer out, alignment key store by top microscope, then retract
  3. Two wafers are automatically aligned to each other by calculating the relative X, Y locations of alignment keys
  - Key factors:
    - Wafer separation less than 50 μm
    - Require rigid viewing port
    - Capable for micron-level alignment

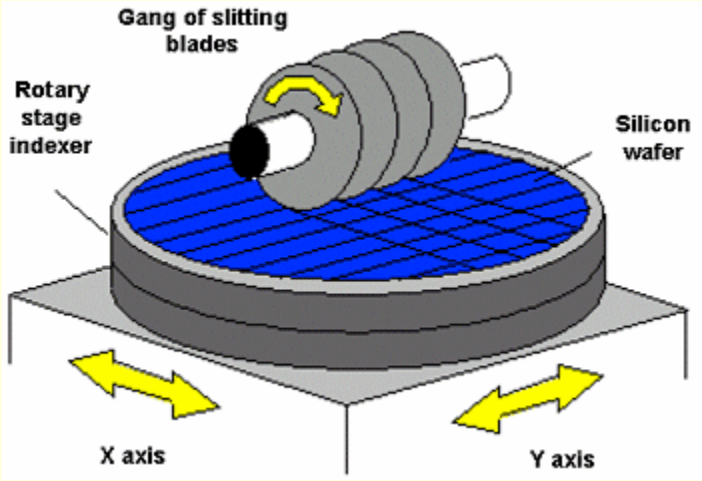


Packaging Technologies

- Wafer Bonding
- **Wafer Dicing**
- Thermal Management
- Stress Isolation
- Protective Coating
- Hermetic Packaging
- Calibration and Compensation
- Die Attach Process
- Wiring and Interconnection
- Types of Packaging Solutions

Wafer Dicing

- To secure wafer, use blue “sticky” tape to hold silicon wafer or bond to dummy wafer by crystal bond
- A diamond or carbide blade is 75-250 μm wide (your chip design should separate at least 2-3 × of the blade)
- Dicing usually use water to cool blade during dicing ⇒ makes the process unclean (and lots of vibrations)
  - Tricks to avoid contamination on the device side:
    - Forming shallow dimple in the blue tape and mount wafer upside down (Analog Device)
    - Bonded a cap or cover made of silicon or glass to protect MEMS structures (Bosch Process)
- Release after dicing



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Thermal Management

- Thermal management in
  - IC
    - To cool integrated circuit during operation
  - MEMS
    - Die level
      - Ensure long-term stability of (piezoresistive) sense element by verifying the no thermal gradients arise within the membrane
    - Package level
      - Must take all accounts from die level
      - In addition, packaging does not interfere with the die-level thermal isolation scheme
      - Ceramics and metal have high thermal conductivity $\Rightarrow$ good candidate materials for housing

Packaging Technologies

- Wafer Bonding
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- **Stress Isolation**
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Stress Isolation

- Piezoresistive pressure sensor also very sensitive to stress $\Rightarrow$ undesired stress from packaging housing should be omitted
- Slow creep in the adhesive or epoxy will cause long-term drift
  - Choose a right kind of epoxy (company's secret)

Packaging Technologies

- Wafer Bonding
- Wafer Dicing
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- Stress Isolation
- **Protective Coating**
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Protective Coating

- Protect sensor from humidity, acid and corrosive environment
  - The most common solution is to coat a layer of parylene by chemical vapor deposition
    - Resistant to automotive exhaust gas, fuel, salt, spray, water, alcohol, and organic solvents
    - Will not suit for extended exposure to highly acidic or alkaline solutions
  - Alternating coating material: Silicon carbide (SiC)

Packaging Technologies

- Wafer Bonding
- Wafer Dicing
- Thermal Management
- Stress Isolation
- Protective Coating
- **Hermetic Packaging**
- Die Attach Process
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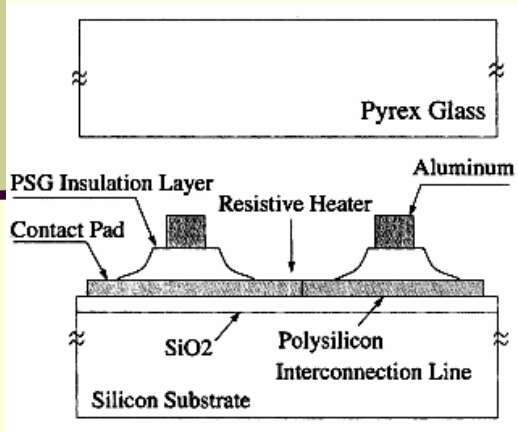
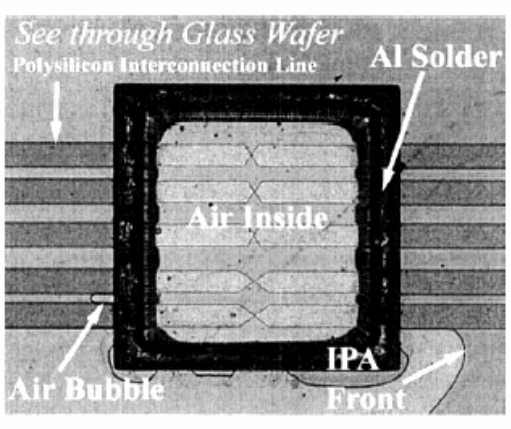
Hermetic Packaging

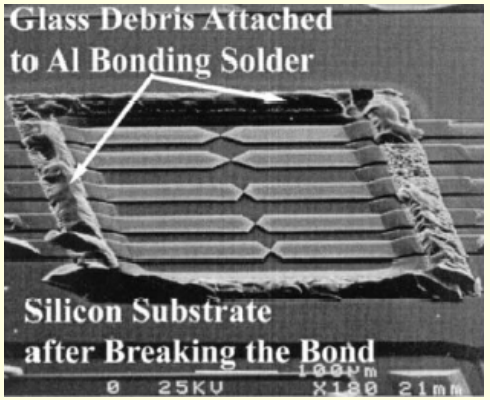
- Hermetic packaging
  - Definition of hermetic packaging:
    - Prevent diffusion of helium (He)
    - Leak rate should be lower than 5×10^{-8} cm^{-3}/s in small volume package (<0.40 cm^{-3})
  - Prevent the diffusion of moisture and water vapor through its walls
  - Increase long-term reliability of electronic component

Hermetic Packaging: An Example

- Hermetic packaging by RTP
  (Chiao and Lin, Sensors and Actuators, A91, 2001 p404-408)
  - Al-Glass hermetic wafer bonding using RTP 2 sec at 990°C
  - Accomplishments:
    - Survived IPA and autoclave test
    - The RTP bonding process can overcome at least 2 mm step-up surface roughness as created by the polysilicon interconnection line
    - Enclosed MEMS device still operative after RPT process







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- Wiring and Interconnection
- Types of Packaging Solutions

Die Attach Process

- Individual dies are mounted onto metal or ceramic package, using metal alloy or organic/inorganic adhesives
- Metal alloy: solder
  - Eutectic and Noneutectic:
- Organic adhesive: epoxies, silicon, and polyimides
  - Inexpensive, easy to automated, cure at lower temperature
- Inorganic adhesive: glass matrices embedded with silver and resin
  - Mostly used in the brazing of pressed ceramic package

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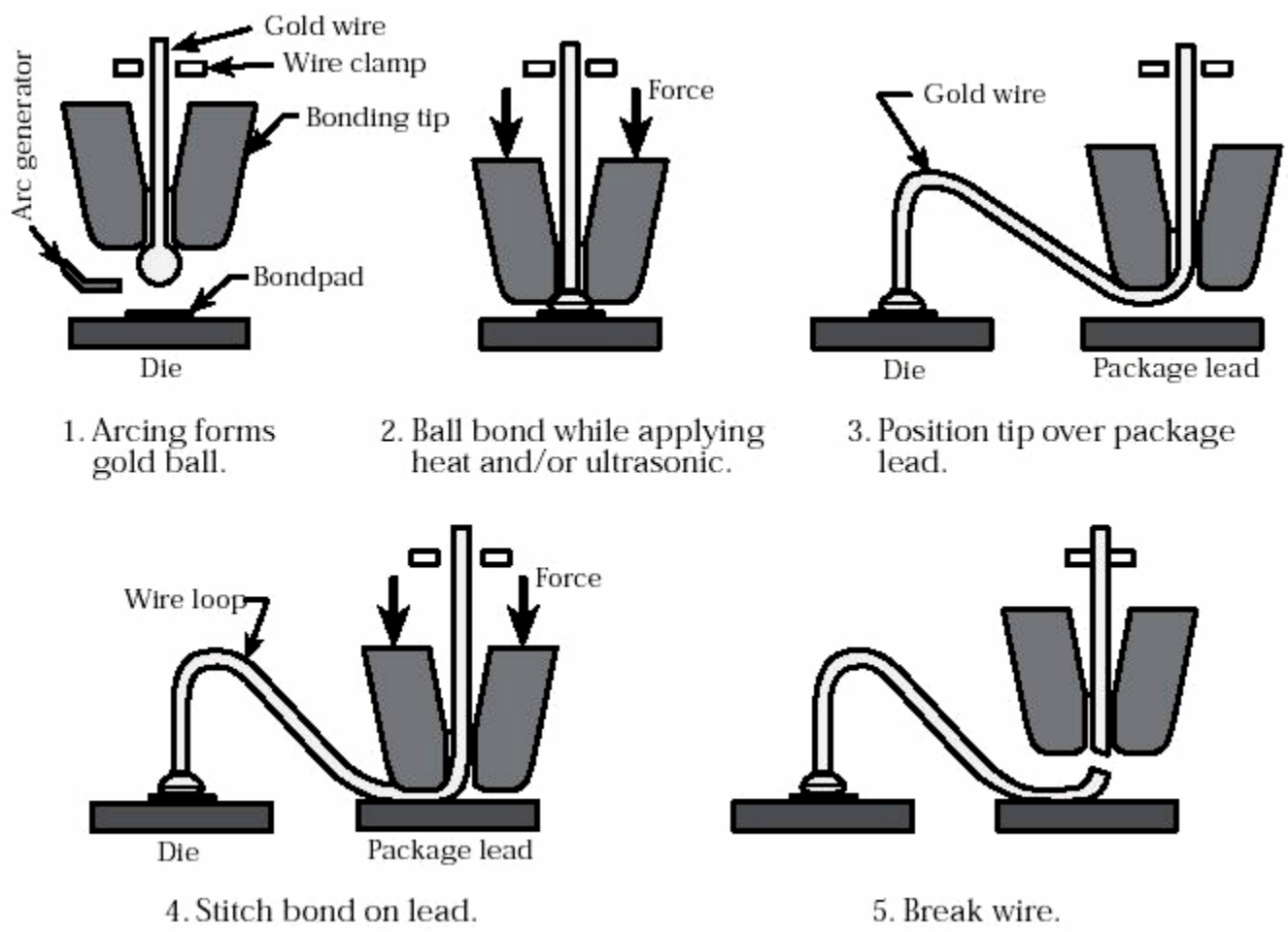
Wiring and Interconnection: Wire Bonding

- Most popular way to connect MEMS/IC die to the package. Mostly use gold or aluminum for interconnection

- Gold wire
  - Use thermosonic wire bonding, i.e. simultaneous combining heat (150°C), pressure, and ultrasonic energy to bond area
  - Gold wire first forms a “ball bond” to Al bond pad on the die, then “stitch” bond to the package lead

- Aluminum wire
  - Use ultrasonic energy to bond
  - Slower the Au bond, but thicker wire is available for higher current

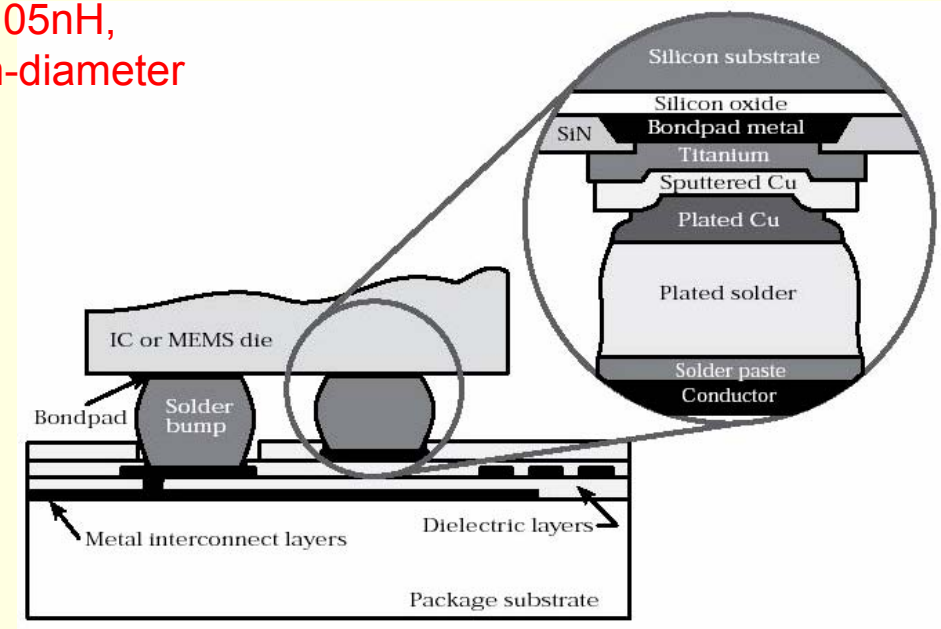
Thermosonic Ball and Stitch Bonding



Source: Maluf, "An Introduction to Microelectromechanical Systems Engineering" Artech House Publishers, 2000

Wiring and Interconnection: Flip Chip

- Increase density of I/O connections
- Reduce interconnect's inductance (<0.05nH, compare to 1nH in 125μm long, 25 μm-diameter wire)
- Process Flow:
  1. Sputter Ti adhesion promoter layer
  2. Sputter thin Cu
  3. Pattern Ti and Cu
  4. Electroplated thicker Cu
  5. Electroplate solder bump (Ti-lead alloy)
  6. Position die to screen-printed substrate
  7. Heating in oven or under infrared radiation and reflow solder



Source: Maluf, "An Introduction to Microelectromechanical Systems Engineering" Artech House Publishers, 2000

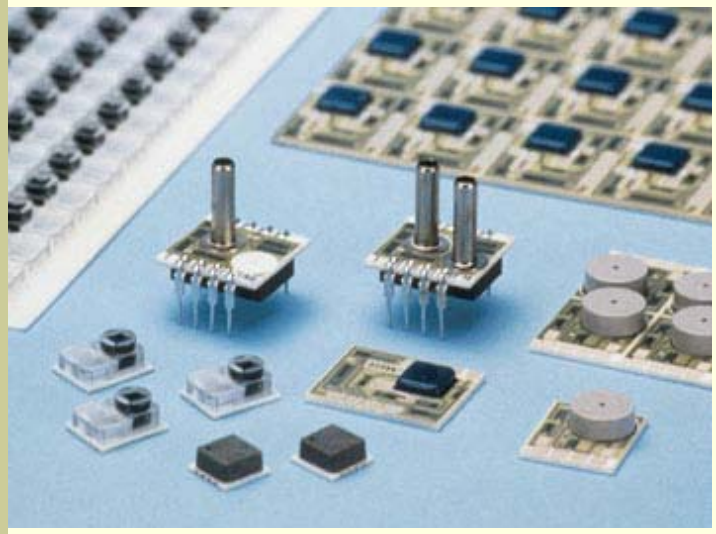
Packaging Technologies

- Wafer Bonding
- Wafer Dicing
- Thermal Management
- Stress Isolation
- Protective Coating
- Hermetic Packaging
- Calibration and Compensation
- Die Attach Process
- Wiring and Interconnection
- **Types of Packaging Solutions**

Types of Packaging Solutions

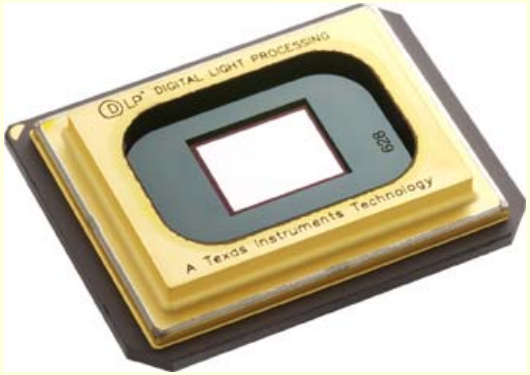
- Ceramic Packaging
  - Majority of ceramics are electrical insulator and good thermal conductors
  - Customizable
- Metal Packaging
  - Many adopted by TO-type (Transistor Output) packages: Prototypes in small volume easy to acquire
  - Hermetic sealed
- Molded Plastic Packaging
  - Not hermetic, low cost, very reliable
  - Two approaches:
    - Postmolding: Mold after the die is attached to lead frame
    - Premolding: Plastic mold is previously molded before die is attached

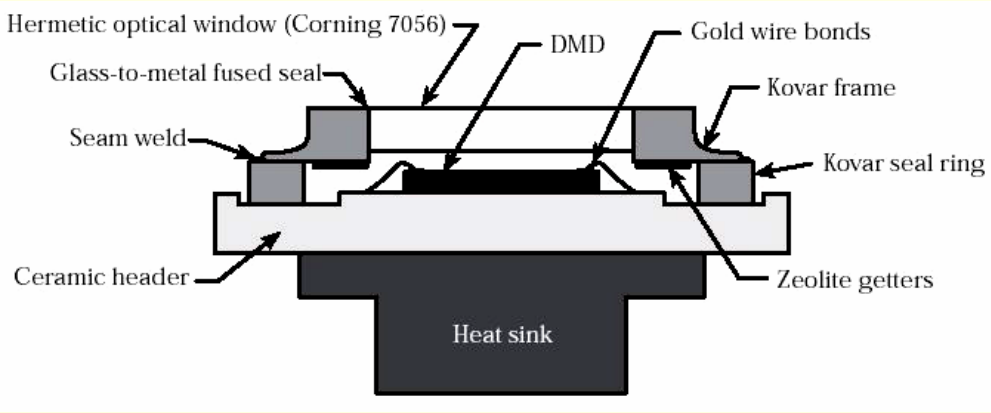
Examples of Ceramic Packaging



Ceramic packages for various pressure sensors

Source: Lucas NovaSensors

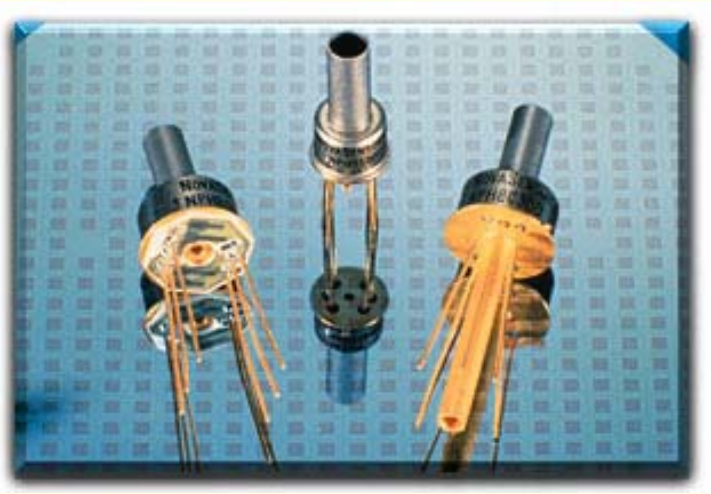




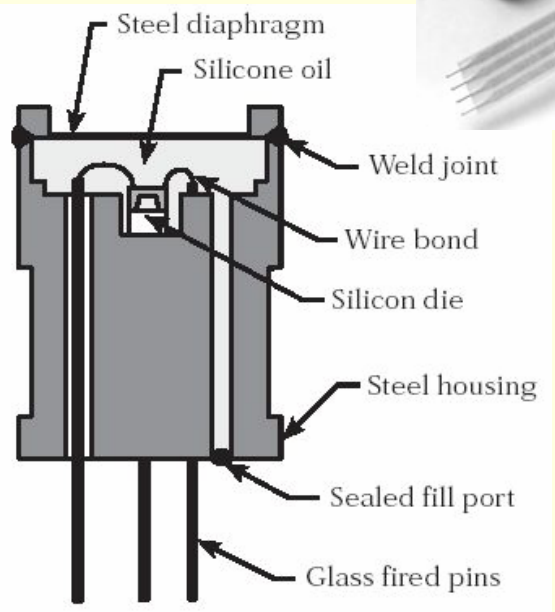
Package of TI DMD™ (Digital Micromirror Device), device shown is SVGA: 800x600; 480,000 mirrors; type A packaging

Source: Texas Instrument, www.dlp.com

Examples of Metal Packaging

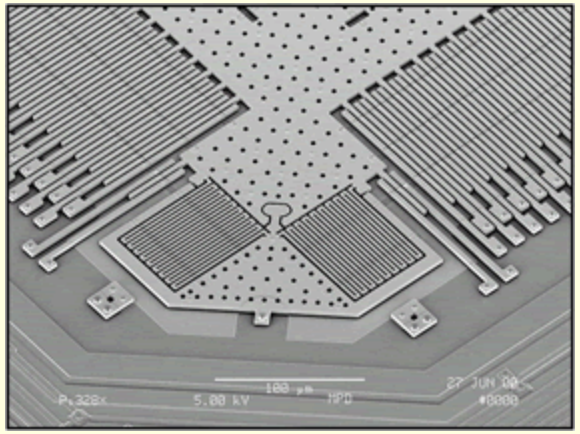


TO-8 Metallic packaged pressure sensors (Source: GE NovaSensors)



The piezoresistive sensor chip is housed in a fluid-filled cylindrical cavity and isolated from measured media by a stainless steel diaphragm and body. (Source: GE NovaSensors and Maluf's Book)

Special Topic: Accelerometer



加速度傳感器

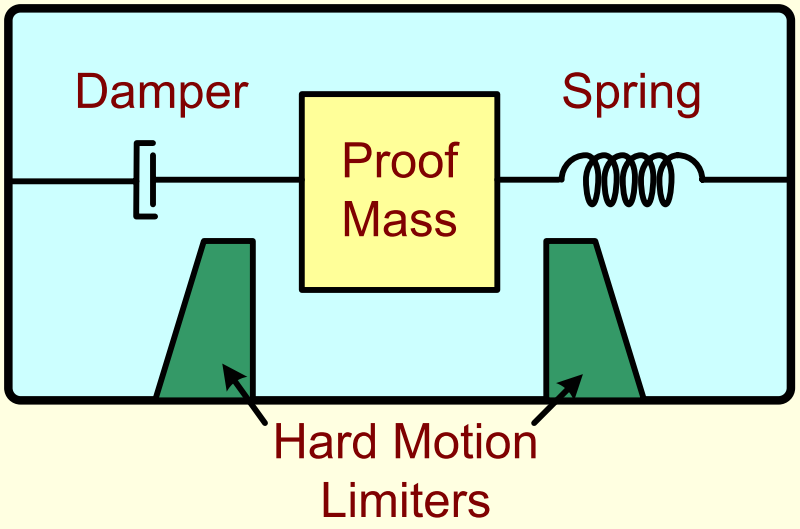
Applications for Accelerometers

- Automotive Industries
  - Deploying airbag
  - Navigation
- Healthcare
  - Pacemakers
- Other
  - Vibration analysis of industrial machinery
  - Hand-held vibration from video camera

Types of Accelerometer

- Accelerometer sense acceleration by using proof mass on which external acceleration can act, and measure the
  - Displacement of the proof mass or force Exerted by the proof mass against the frame
    - Strain gauge, capacitors, strain-sensitive resonant beams, magnetometers, optical detectors (interferometers, etc.), tunneling sensors, etc.
  - The force required to keep it in place
    - Force-balanced, closed-loop control system

Theory of Operation (Passive)



- Assuming linear acceleration for the accelerometer,

$$a = \frac{d^2x}{dt^2} = \frac{dv}{dt}$$

The displacement of the proof mass can be measured by

$F=m\cdot a=k\cdot x_{rel}$,

- A *damper* is to help controlling the frequency response of the accelerometer, which provides a force that is proportional to the velocity of the proof mass relative to the frame, v_{rel},

$$F_{damper} = bv_{rel} = b\frac{dx_{rel}}{dt}$$ where b is damping coeff.

- Overall second-order force equation,

$$F = m\frac{d^2x}{dt^2} = kx_{rel} + b\frac{dx_{rel}}{dt}$$

- Mechanical resonant frequency and quality factor are,

$$\omega_0 = \sqrt{\frac{k}{m}} \quad \text{and} \quad Q = \omega_0\frac{m}{b} = \frac{\sqrt{mk}}{b}$$

Theory of Operation (cont.)

- For a sinusoidal excitation acceleration, the displacement vs. acceleration frequency is,

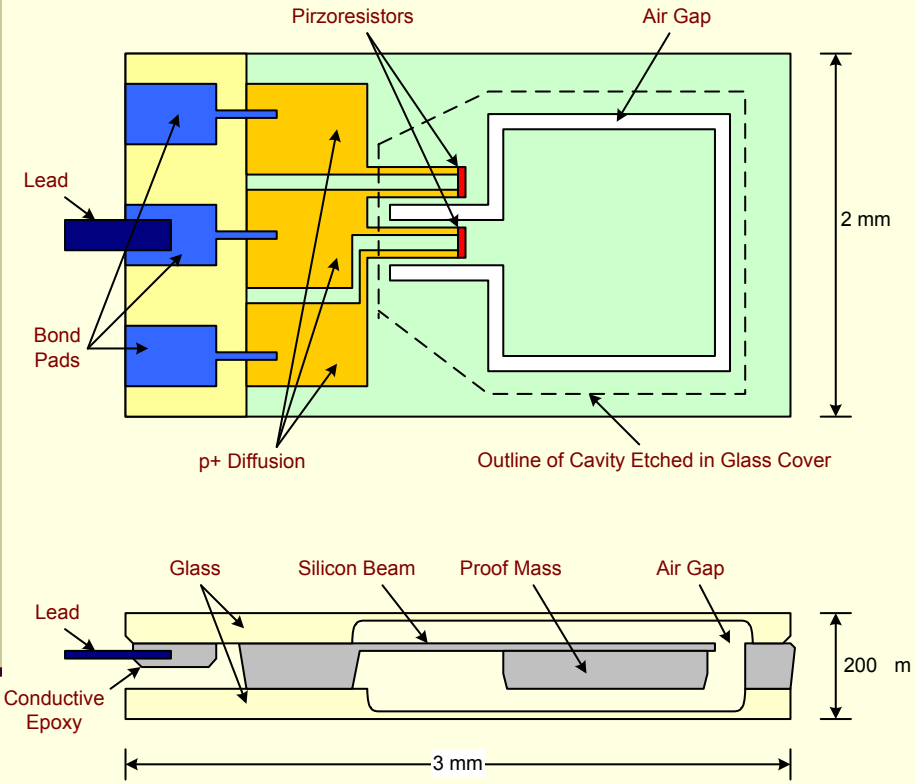
$$|x(\omega)| = \frac{1}{\sqrt{\left(1-\frac{\omega^2}{w_0^2}\right)^2 + \frac{\omega^2}{Q_2\omega_0^2}}}\left(\frac{m}{k}\right)\left|\frac{d^2x}{dt^2}\right|$$

- In the majority of passive accelerometer design,
  - Spring constant (k) $\Rightarrow$ stiffness of silicon beam(s)
  - Damping coefficient (b) $\Rightarrow$ squeeze-film effects in gaps between proof mass and the support structure

- For a second-order system, ideal ("flat") transient response occurs when Q=½. This case referred to as critical damping.

- This can be controlled by *the proof mass (m)*, *the spring constant (k)*, and *the damping coefficient (b).*

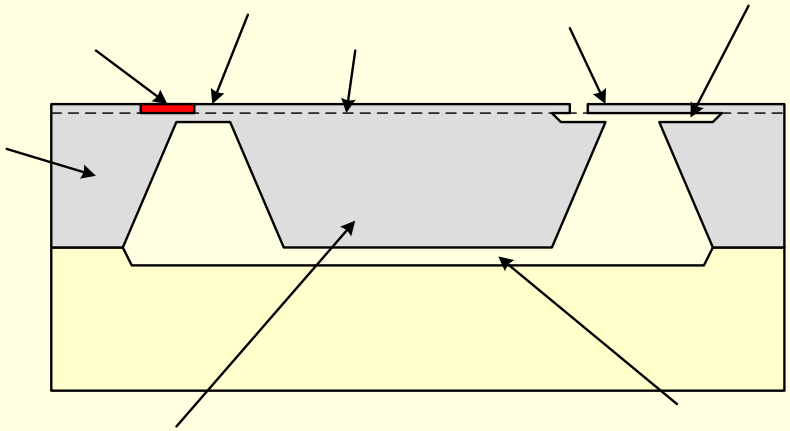
Strain-Gauge Accelerometers



Roylance and Angell "Batch-Fabricated Silicon Accelerometer", IEEE Transactions on Electron Devices, vol. ED-26, no.12, Dec. 1979, p1911-1917

- One of earliest μ-machined accelerometer (1979) for biomedical implants to measure heart wall accelerations
- Displacement of proof mass was measured by diffused piezoresistors
- Facts:
  - Resolution: 0.001 g
  - FSR: ± 200 g
  - Sensitivity: 50 $\mu V/(g \cdot V_{Supply})$
  - Variation in sensitivity vs. Temperature: -0.2% ~ -0.3%
  - Resonant frequency: 2,330 Hz

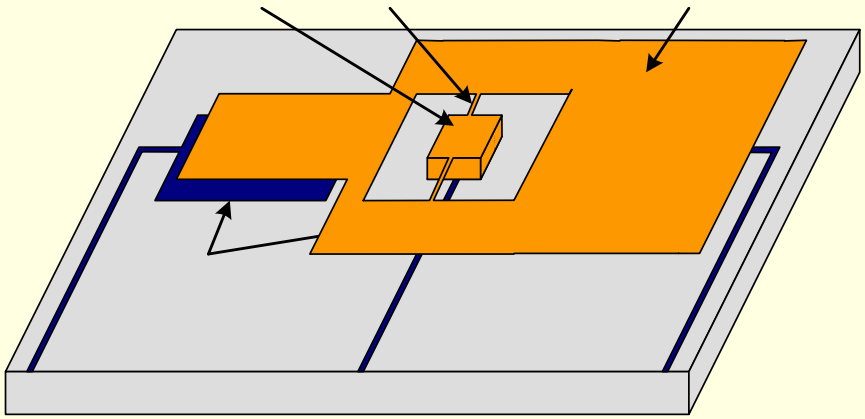
Strain-Gauge Accelerometers



Allen et. al. “Accelerometer Systems with Build-in Testing”
Sensors and Actuators, vol. A21-A23, Feb.-Apr., 1990, p381-386

- Improved structure:
  - Si fusion bonding to form precisely controlled upper layer over pre-defined cavity (Gap 2)
  - Electrostatic Self-test capability
    - Thermally expanded beam under electrical control, which can buckle and push the proof mass downward
    - Can measure acceleration simultaneously

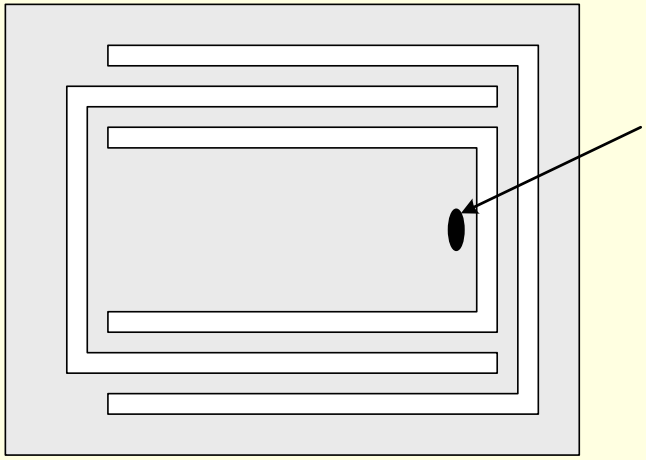
Capacitive Accelerometers

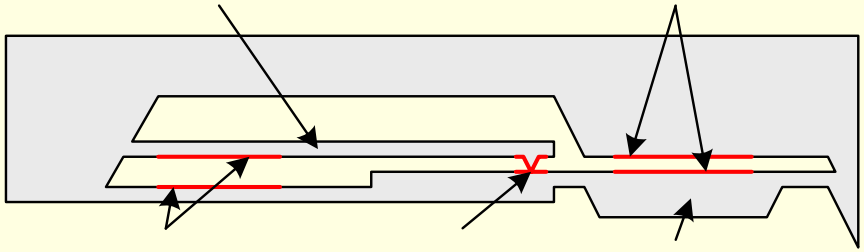


Cole “New Sense Element Technology for Accelerometer Subsystems” Proceedings of Transducers ’91, San Francisco, CA, June 24-27, 1991, p93-96

- Asymmetrical plate will rotate under acceleration ⇒ Underlying sensing plate will measure the varying ratio of the capacitance
- Sensitivity of the device can be controlled by the dimension of torsion bar (e.g. 25 g device ⇒ $8\mu m \times 100\mu m \times 5\mu m$)

Tunneling Accelerometers





- Tunneling current $I = I_0 e^{\left(-\beta\sqrt{\phi}z\right)}$

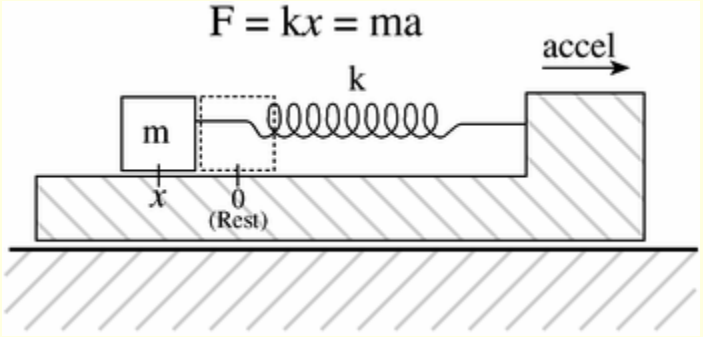
  where I_0: Scaling factor, dep. on materials, tip shape
  β: Conversion factor, typical 10.25 $eV^{-½}$/nm
  ϕ: Tunneling barrier height, typical 0.5 eV
  z: tip/surface separation in nm, typical 1 nm

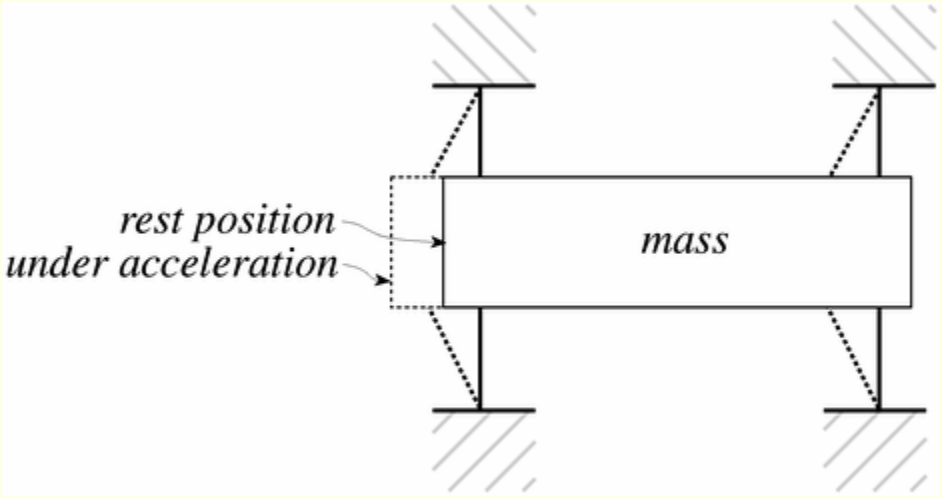
- Tunneling transducer is very sensitive to small displacement at the sub-nanometer level

- Very nonlinear behavior ⇒ Require closed-loop feedback to linearize the system

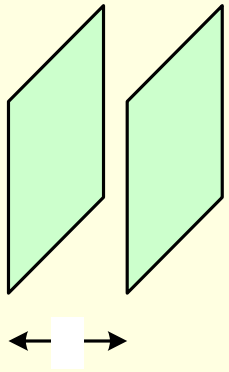
- Active device: Electrostatic actuation to maintain constant tunneling current during acceleration, so the tip does not actually move

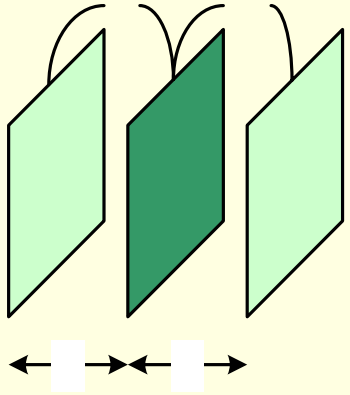
Force-Balanced Accelerometers





Force-Balanced Accelerometers





- Assuming capacitors at rest place,

$$C = \frac{\varepsilon A}{x_0} \equiv \frac{k}{x_0}$$

- When the middle plate moves x, then 2 capacitors, C_A and C_B, will become

$$C_A = \frac{k}{x_o + x} \quad \text{and} \quad C_B = \frac{k}{x_o - x}$$

- Then C_A and C_B can be rewritten as

$$C_A = C\frac{x_o}{x_o + x} \quad \text{and} \quad C_B = C\frac{x_o}{x_o - x}$$

then,

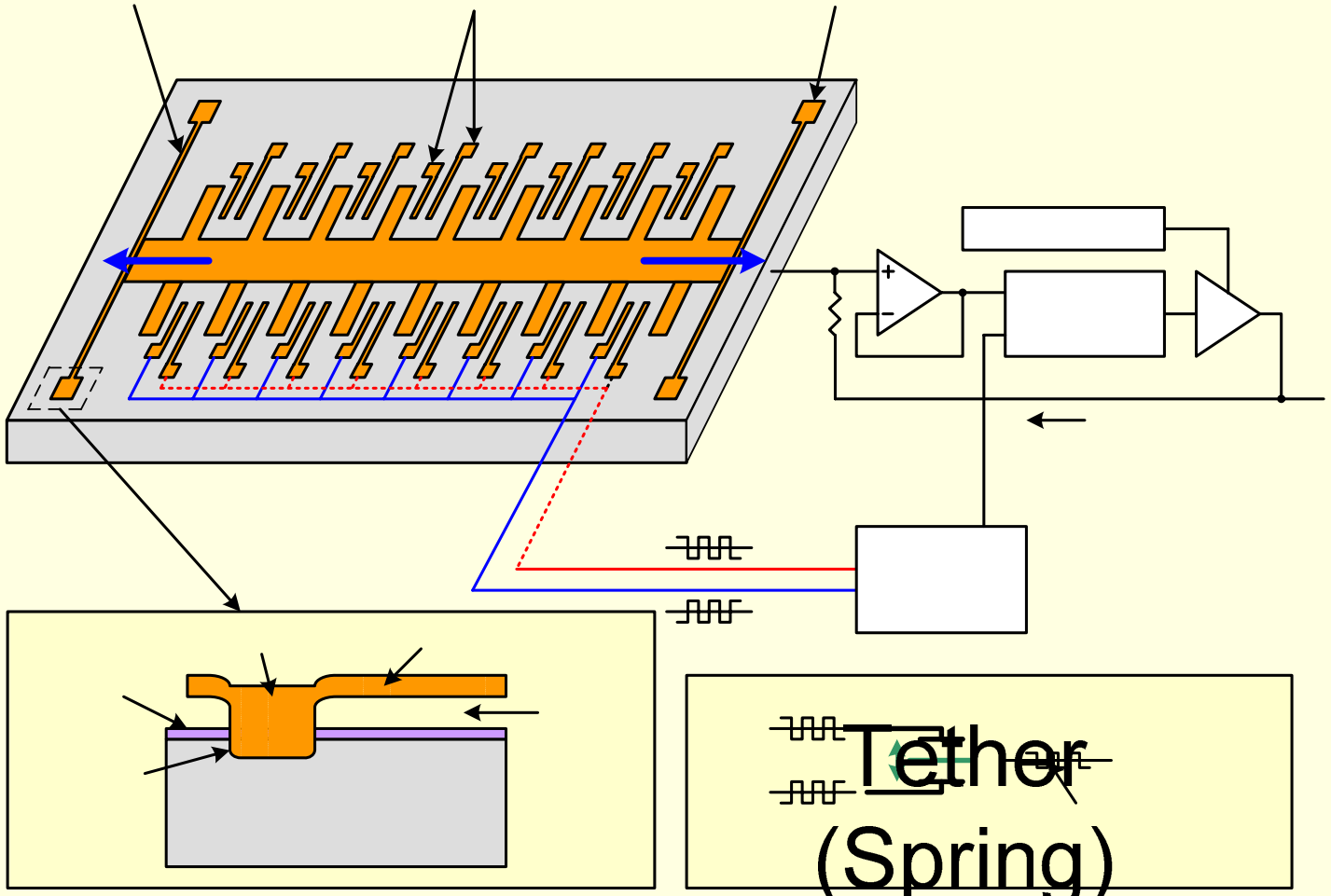
$$\Delta C = C_A - C_B = Cx_o\left(\frac{1}{x_o + x} - \frac{1}{x_o - x}\right) = Cx_o\left(\frac{-2x}{x_o^2 - x^2}\right) = \frac{-2kx}{x_o^2 - x^2}$$

for a small displacement, ΔC is approximate to

$$\Delta C \approx \left(\frac{-2k}{x_0^2}\right)x$$

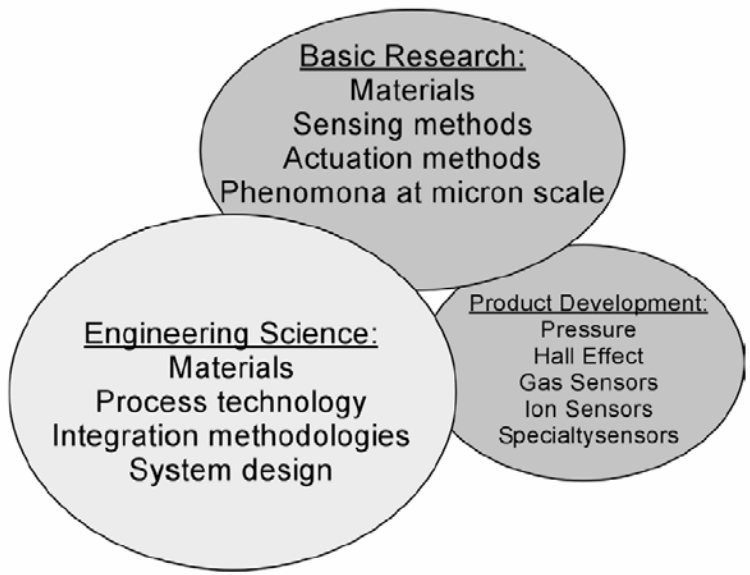
Force-Balanced Accelerometers

Analog Device ADXL-50

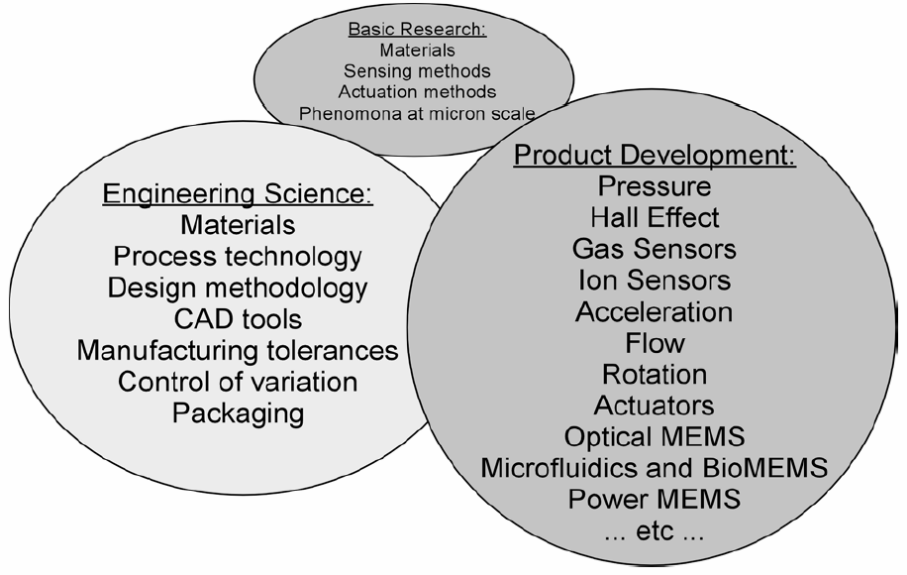


Summary: MEMS Future

"MEMS in the future will be judged less by what is learned and more by what is or can be accomplished in the practical world."
Stephen Senturia, Transducer '03



State of MEMS in 1981



State of MEMS in 2003

Source: Senturia, IEEE Transducers 03 Conference, Jun 2003, Boston, MA 1A2.2

Useful Books and Websites

- Books:
  - Gregory Kovacs: Micromachined Transducers Sourcebook (ISBN: 0072907223)
  - Marc Madou: Fundamentals of Microfabrication 2nd Edition (ISBN: 0849308267)
  - Stephen Senturia: Microsystem Design (ISBN: 0792372468)
  - Stanley Wolf: Silicon Processing for the VLSI Era, Vol. 1 – Process Technology (ISBN: 0961672161)
- Websites:
  - All About MEMS: http://www.allaboutmems.com/
  - MEMS Net: http://www.memsnet.org/
  - World of MEMS: http://www.mems.de/index.htm