1. Description

1.1. Project

Project Name	sous_vide_cooker
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 6.4.0
Date	02/13/2022

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration
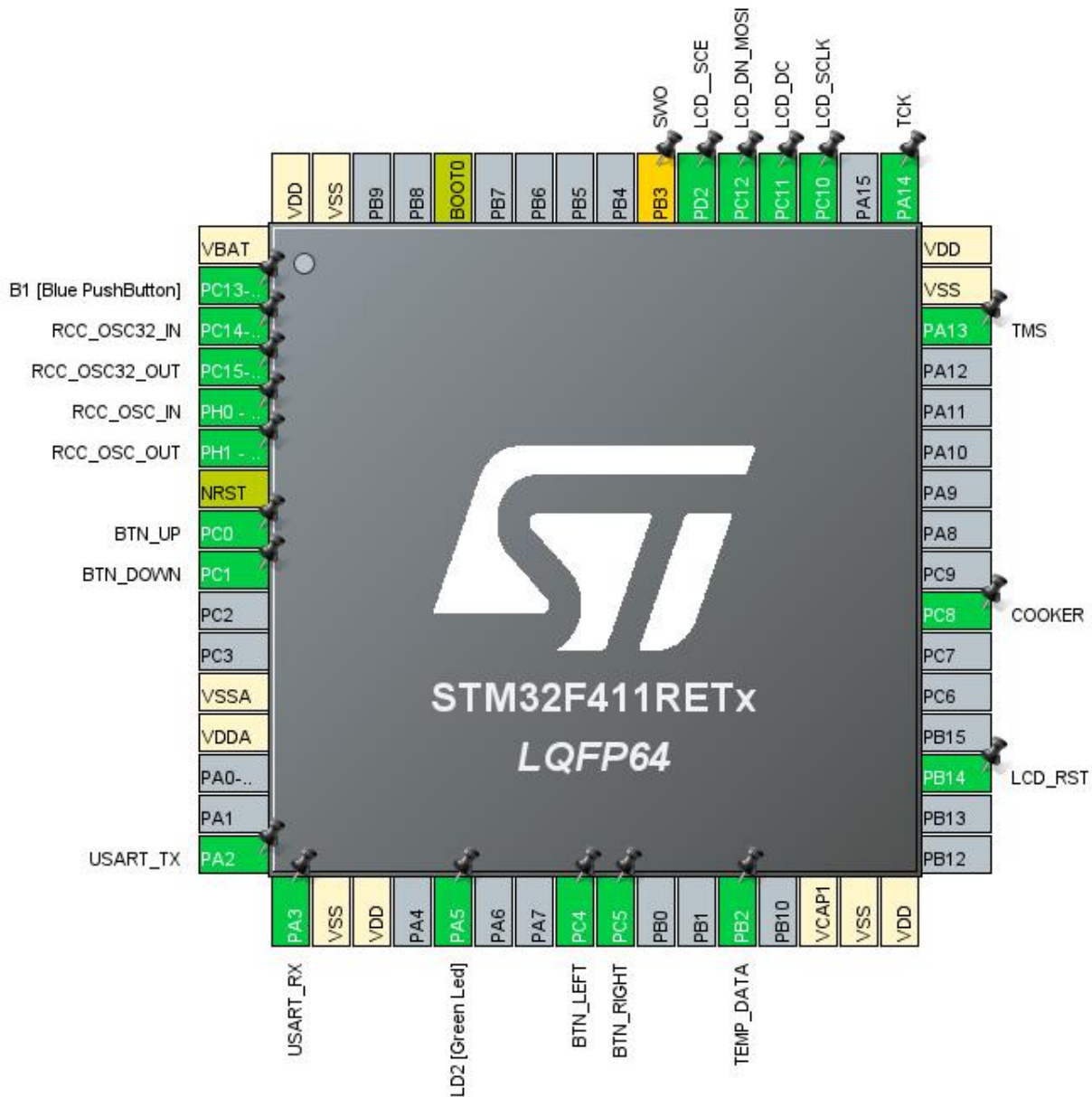
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	BTN_UP
9	PC1 *	I/O	GPIO_Input	BTN_DOWN
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
24	PC4 *	I/O	GPIO_Input	BTN_LEFT
25	PC5 *	I/O	GPIO_Input	BTN_RIGHT
28	PB2 *	I/O	GPIO_Input	TEMP_DATA
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14 *	I/O	GPIO_Output	LCD_RST
39	PC8 *	I/O	GPIO_Output	COOKER
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10	I/O	SPI3_SCK	LCD_SCLK
52	PC11 *	I/O	GPIO_Output	LCD_DC
53	PC12	I/O	SPI3_MOSI	LCD_DN_MOSI
54	PD2 *	I/O	GPIO_Output	LCD__SCE
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

 * The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
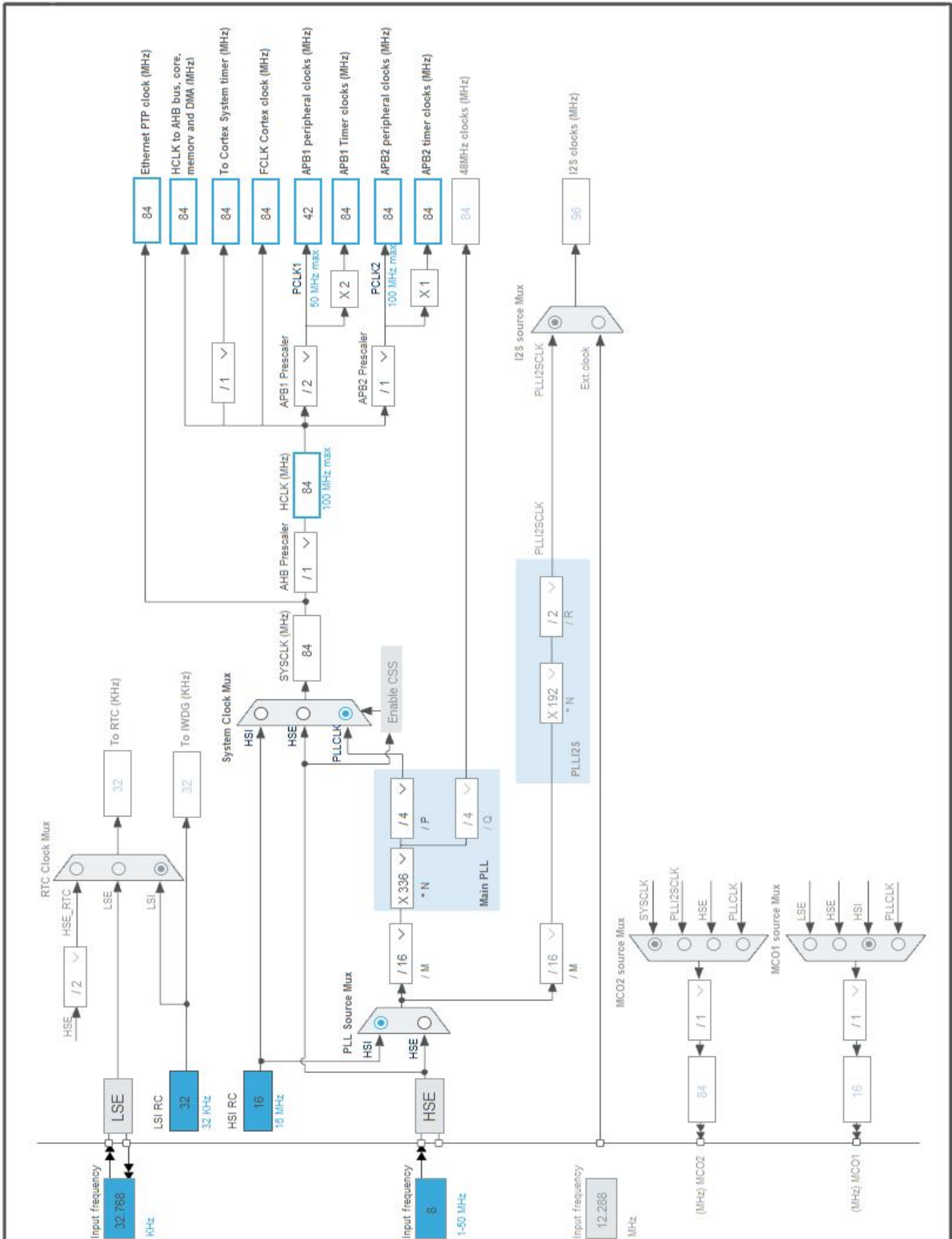
5. Software Project

5.1. Project Settings

Name	Value
Project Name	sous_vide_cooker
Project Folder	C:\Users\mszab\projects\STM32CubeIDE\sous_vide_cooker
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART2_UART_Init	USART2
4	MX_TIM3_Init	TIM3
5	MX_SPI3_Init	SPI3
6	MX_TIM10_Init	TIM10

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	DS10314_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	1.7

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 µA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19 days, 6 hours	Average DMIPS	125.0 DMIPS

6.6. Chart

Consumption Profile by Step
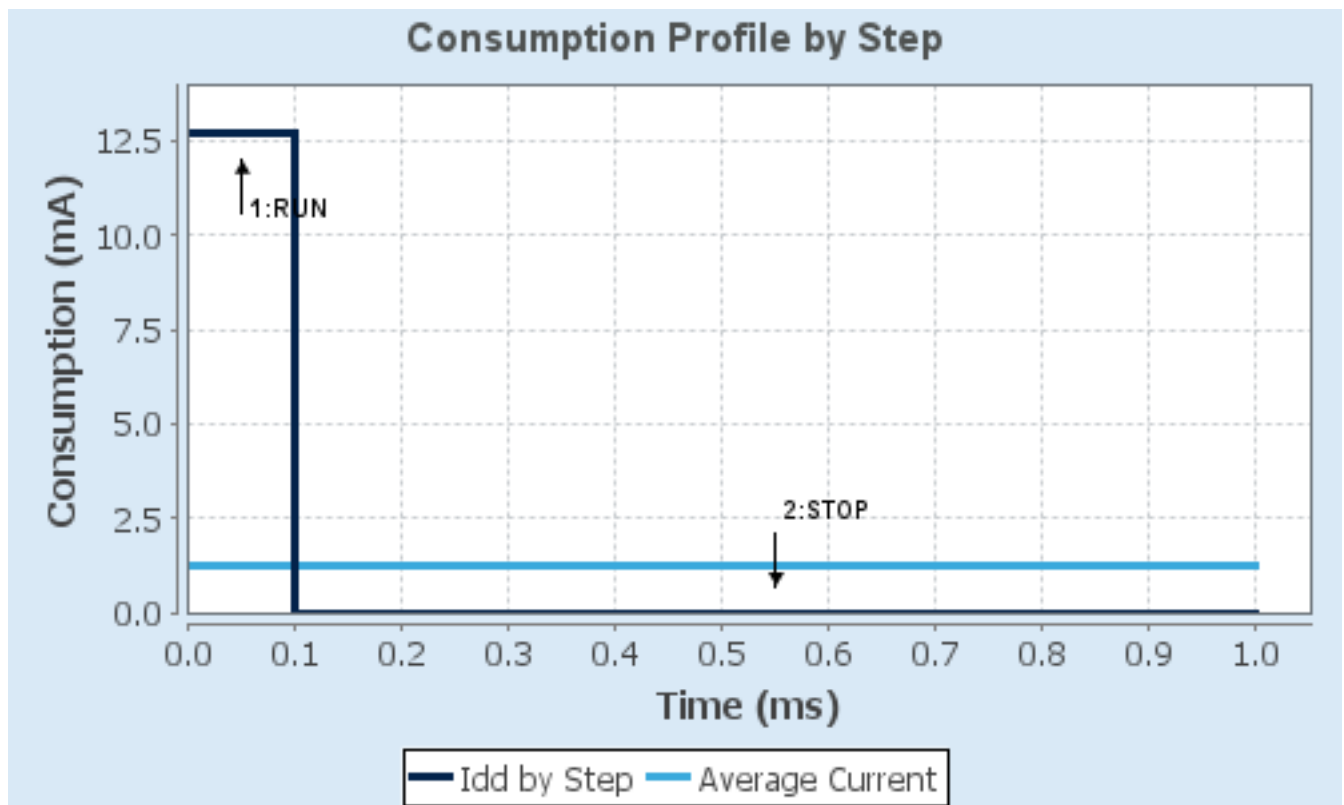
7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.2. SPI3

Mode: Transmit Only Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**2.625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. TIM3

Clock Source   : Internal Clock

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**42000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2 - 1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.5. TIM10

mode: Activated

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84 -1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xffff-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.6. USART2

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LCD_SCLK
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LCD_DN_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_RX
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13-ANTI_TAMP	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_UP
	PC1	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_DOWN
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PC4	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_LEFT
	PC5	GPIO_Input	Input mode	**Pull-up ***	n/a	BTN_RIGHT
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TEMP_DATA
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	COOKER
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DC

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD__SCE

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

| Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM3 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM3 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00115249.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00119316.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00137034.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156364.pdf

Application note   http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note   http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note   http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note   http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note   http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note   http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note   http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note   http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note   http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note   http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note   http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note   http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note   http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note   http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note   http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note   http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note   http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note   http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note   http://www.st.com/resource/en/application_note/DM00725181.pdf