Lab 3 – Programming Combinational Logic on the Basys FPGA Board

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Overview

The purpose of lab 3 was to help understand configuration file, and and how to link it to the of logic components on Basys board.

New Concepts

Some concepts for this lab included creating and implementing a UCF file with Basys 2 syntax, creating configuration files, and programming Adept.

Analysis

Part 2 Procedure:

1. Use specs from lab 2 regarding systems functionality
2. On board LEDs act as sprinkler valves
3. Basys switches SW2 = A, SW1 = B, SW0 = C, and SW7 = E

Truth table:

E	A	B	C	d0	d1	d2	d3	d4	d5	d6	d7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Part 3 Procedure:

1. Create the circuit
2. Create UCF file
3. Plug into Basys 2 board
4. Select .bit file and click “program” button
5. Test program

Truth table:

SW3	SW2	SW1	SW0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0

Records

Part 1:

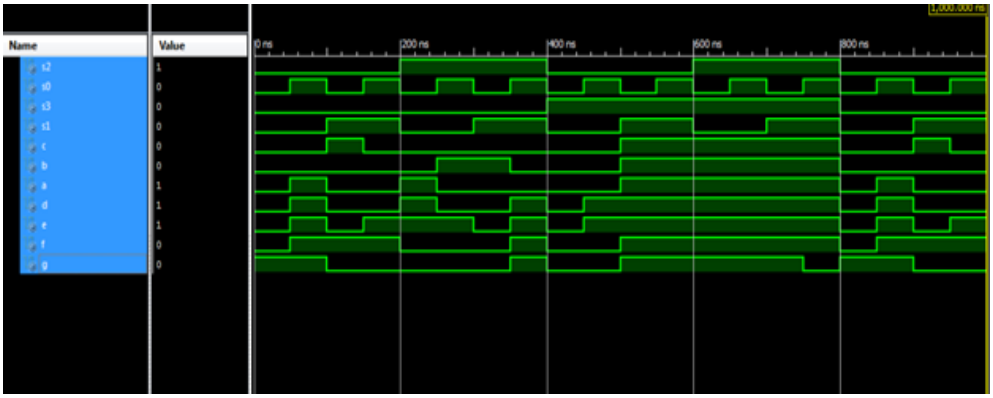
```
# Pin assignment for LEDs
NET "d" LOC = "p15" ; # Bank = 3, Signal name = LD0
# Pin assignment for SWs
NET "i1" LOC = "p36"; # Bank = 3, Signal name = SW1
NET "i2" LOC = "p38"; # Bank = 2, Signal name = SW0
```

Part 2:

```
NET "E" LOC = "P6";
NET "A" LOC = "P29";
NET "B" LOC = "P36";
NET "C" LOC = "P38";

NET "d0" LOC = "P2";
NET "d1" LOC = "P3";
NET "d2" LOC = "P4";
NET "d3" LOC = "P5";
NET "d4" LOC = "P7";
NET "d5" LOC = "P8";
NET "d6" LOC = "P14";
NET "d7" LOC = "P15";
```

Part 3:



```
# Inputs
NET "sw0" LOC = "p38";
NET "sw1" LOC = "p36";
NET "sw2" LOC = "p29";
NET "sw3" LOC = "p24";
# Outputs
NET "a" LOC = "p25";
NET "b" LOC = "p16";
NET "c" LOC = "p23";
NET "d" LOC = "p21";
NET "e" LOC = "p20";
NET "f" LOC = "p17";
NET "g" LOC = "p83";
// ANx
NET "an0" LOC = "p26";
NET "an1" LOC = "p32";
NET "an2" LOC = "p33";
NET "an3" LOC = "p34";
```

Discussion

The results of my tests were successful, from creating a simple AND gate to programming a 7-segment LED display. Learning how each LED display was connected to create a number was challenging, and finding the right path to create each number/letter, from 0-9 and A-F, took some time.

Conclusion

The purpose of this lab was to understand Xilinx ISE software, simulations, ICFs, and how to implement them on the BASYS board. In the first experiment, we went through the whole cycle of system design, analysis, synthesis, and FPGA based hardware implementation, all to make a simple AND gate. The second experiment gave us more practice by doing the same things but in a more practical matter.The last experiment got us familiar with how LEDs are programmed.

Questions

1. Can there be a difference in logical behavior between the intended logic entered and simulated and, the logic actually synthesized for FPGA? Why?
Yes, there can be a difference in logical behavior between the intended logic and simulated logic because the schematic might be wrong.

2. Why do we need a configuration file?
A configuration file sets up initial conditions, such as setting the clock to JTAG. That way the schematic and code will work properly with the hardware attached, specifically the BASYS board.

3. Is there a functional difference in circuitry between Lab 1, Part 3 and Basys board for this particular application?
No, there is no functional difference.

4. What must be done in order to use switches SW3 and SW7 instead of SW0 and SW1? How about using LED5 instead of LED0?
In order to use switches SW3 and SW7, we must change our UCF file, and change our P38 (SW0) and P36(SW1) to P24(SW3) and P6(SW7).
To use LED5 instead of LED0, we must change our UCF file from P15 to P4.