Lab 1 - Xilinx Environment

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Overview:

This lab was to help us get started with ISE Design Suite. I first began by creating a logic schematic consisting of AND, OR, and NAND gates. Then, I learned how to set up a test bench and create a ucf/bit file to make it compatible to run in adept.

New Concepts:

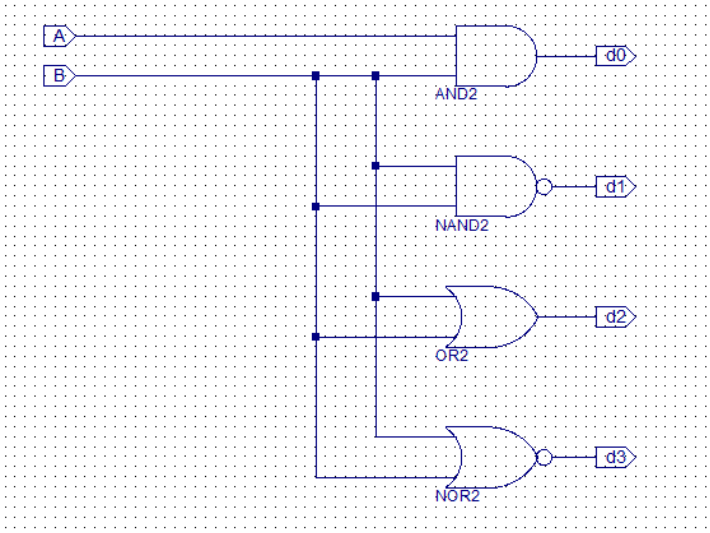
This lab introduced the new design environment and all the features that are accessible. Also this lab acts as a basis for the labs to come.

Analysis:

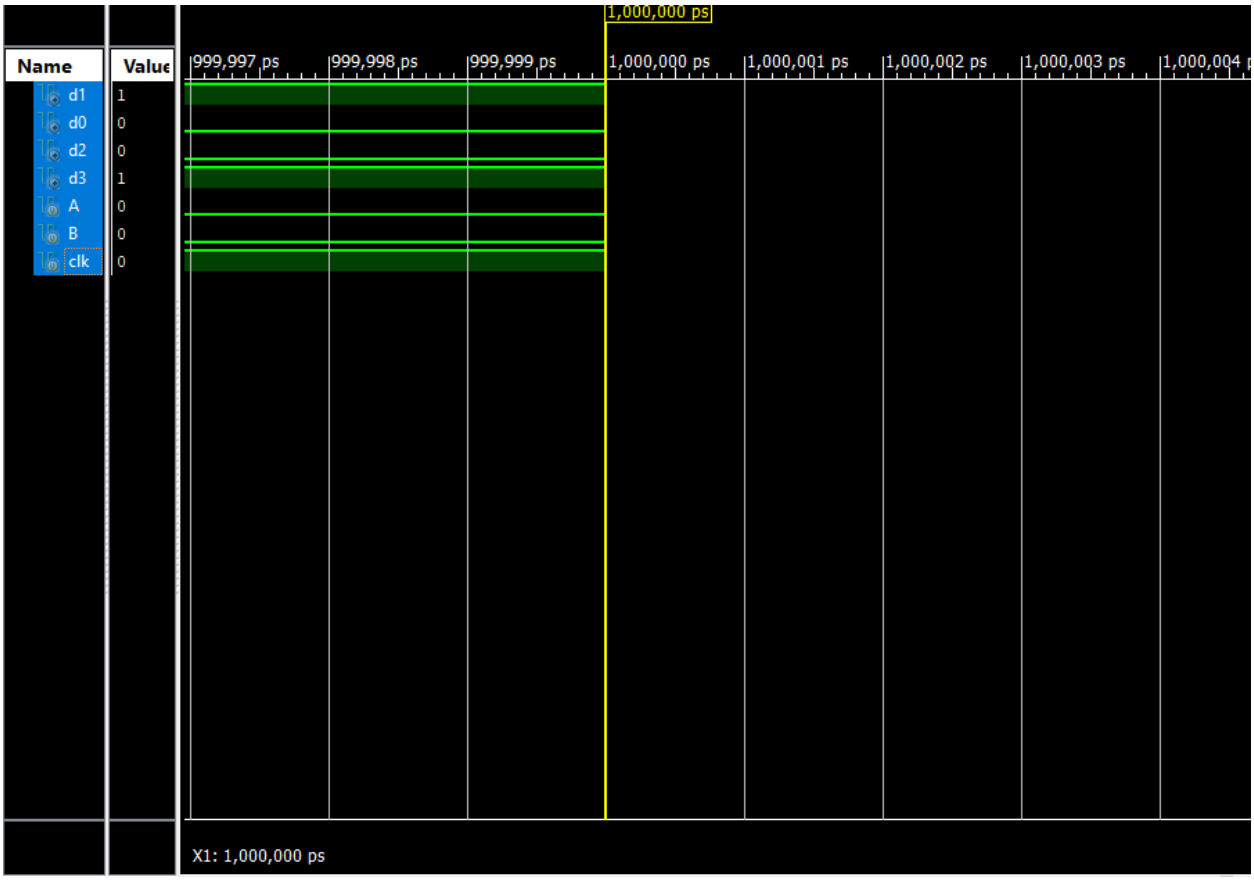
I first created a logic schematic using AND, OR, and NAND gates. Then, I set up a basic test bench that initializes the buttons and leds. The UCF file linked inputs/outputs to the buttons and LEDs on the BAYSYS board.

Records:

Schematic



Simulation



UCF -

NET "A" LOC = "pA7"

NET "B" LOC = "pM4"

NET "d0" LOC = "pG1"

NET "d1" LOC = "pP4"

NET "d2" LOC = "pN4"

NET "d3" LOC = "pN5"

Discussion:

Everything worked as planned, as the lab was very straightforward. The only issue was with the environment itself, where I had to tweak some of the files to get some of the functionality on the x64 bit to work.

Conclusion:

The main goal of this lab is to help us get started with the tools and language needed for this class. All the tools used and learn will be beneficial to know in the upcoming labs.