# Lab 2 – Decoders and Muxes

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Overview

This lab focuses on the construction of decoders and muxes. I first began by creating a 3x8 circuit and implemented it into a sprinkler system. I then did something similar where I created a 4x1 mux. For both circuits, I utilized two kinds of implementation: structural and behavioral.

New Concepts

New concepts were learning new Verilog syntax and creating test benches and structures within modules.

Analysis

In the first part of the lab I created a schematic of a 3x8 decoder and implemented the truth table of the sprinkler system as shown below. Similarily, I created a 4x1 mux, and generated a test bench in verilog. Then, simulating the schematic and test bench I created the waveform.

Truth Table:

| E | A | B | C | d0 | d1 | d2 | d3 | d4 | d5 | d6 | d7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

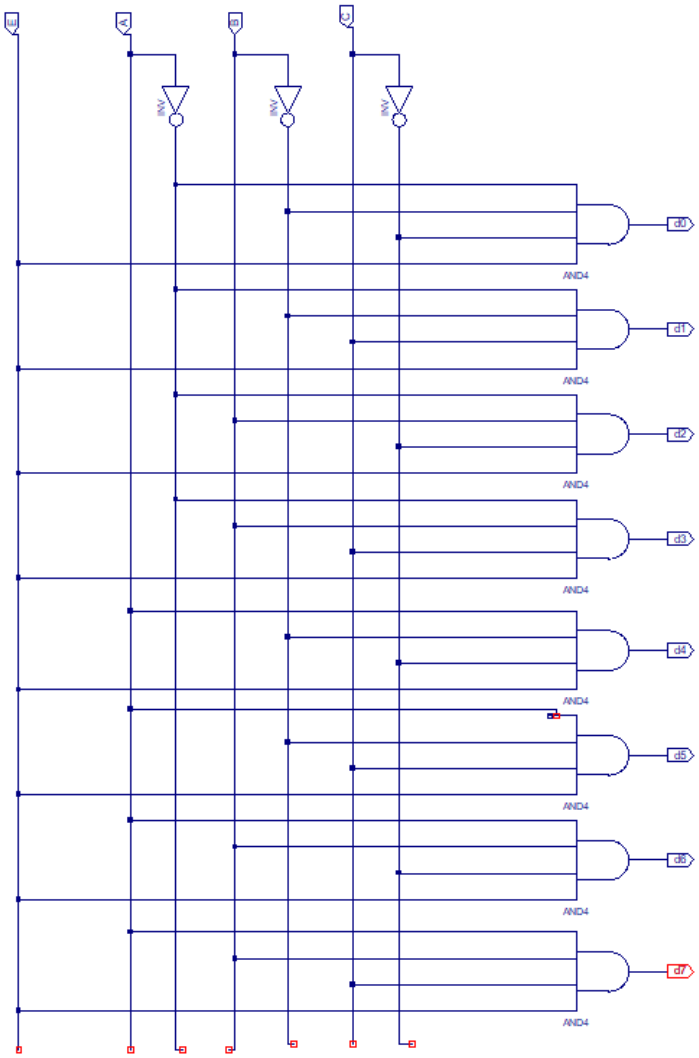
Truth table:

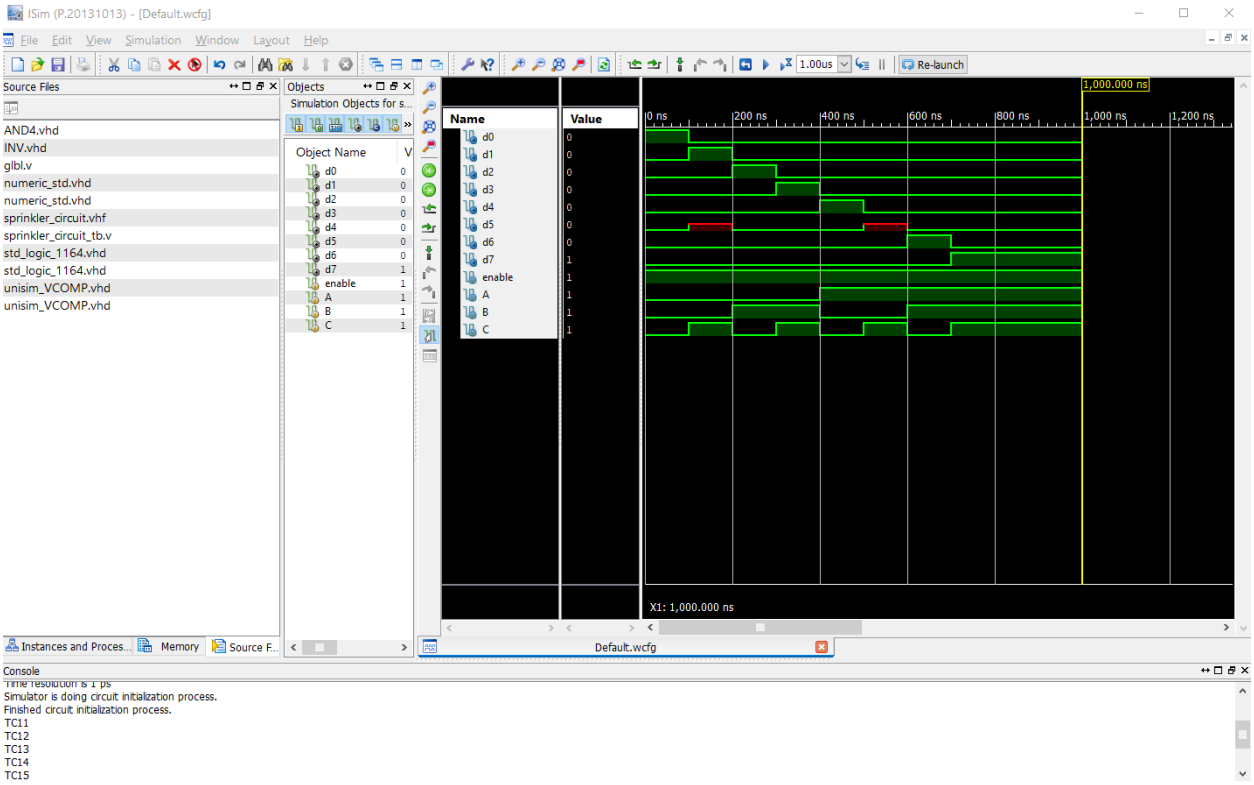
| S0 | S1 | I3 | I2 | I1 | I0 | D |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Boolean equation: D = S0'.S1.I0 + S0'.S1.I1 + S0.S1'.I2 + S0.S1.I3

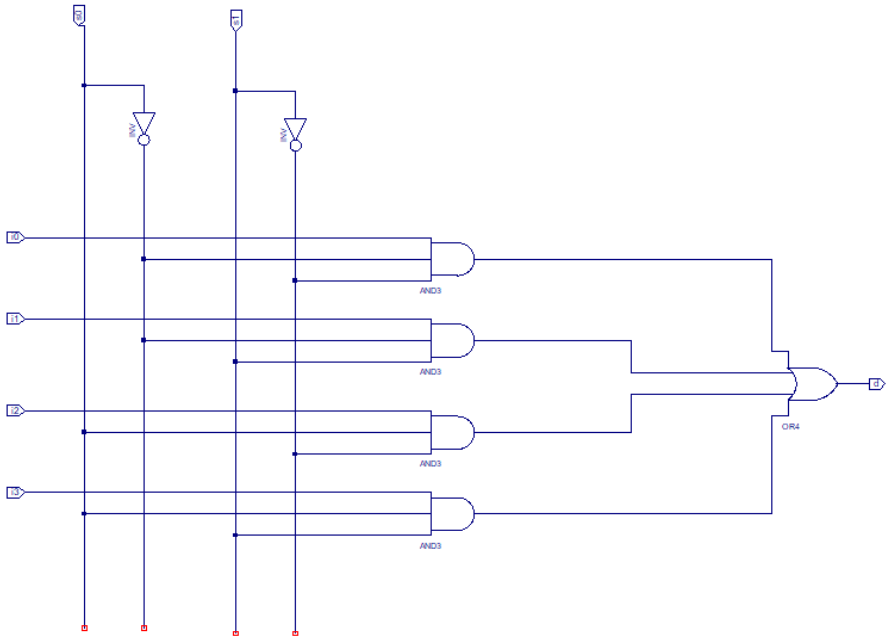
Records

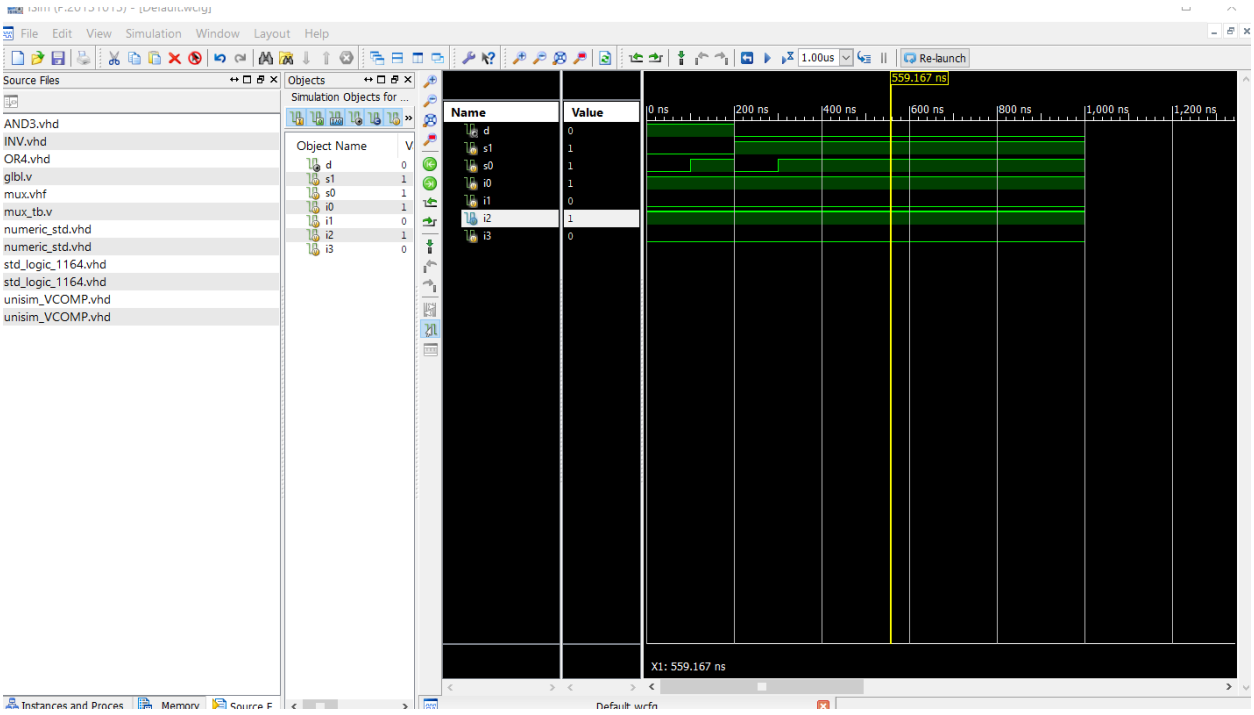
Part 1:


A
B
C
INV
INV
INV
d0
d1
d2
d3
d4
d5
d6
d7
AND4
AND4
AND4
AND4
AND4
AND4
AND4
AND4


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Source Files
AND4.vhd
INV.vhd
glbl.v
numeric_std.vhd
numeric_std.vhd
sprinkler_circuit.vhf
sprinkler_circuit_tb.v
std_logic_1164.vhd
std_logic_1164.vhd
unisim_VCOMP.vhd
unisim_VCOMP.vhd
Objects
Simulation Objects for s...
Object Name
d0
d1
d2
d3
d4
d5
d6
d7
enable
A
B
C
Name
Value
0 ns
200 ns
400 ns
600 ns
800 ns
1,000 ns
1,200 ns
1,000.000 ns
X1: 1,000.000 ns
Instances and Proces...
Memory
Source F...
Default.wcfg
Console
Simulator is doing circuit initialization process.
Finished circuit initialization process.
TC11
TC12
TC13
TC14
TC15

## Part 2:


INV
INV
AND3
AND3
AND3
AND3
OR4




## Discussion

I had trouble with creating a module within a module. My syntax did not properly link the test benches with the schematic, therefore causing a "run aborted" error when running the iSim simulator. I fixed this by recreating the module and properly linking it beforehand. I also had a issue creating the waveform in part 2 of the lab. For some reason, when I ran the iSim simulator all my values were X's and U's.

## Conclusion

In this lab, we reviewed and got to know more of the Xilinx ISE, simulated and designed a 3x8 decoder and 4x1 mux. We also generated a testbench and waveform for both schematics. Although we had some issues in the beginning with getting a working simulation, we were able to fix it by switching between different versions of the Xilinx software. With properly working test benches, we were able to visualize our schematics through the waveforms.

## Questions

1. What is a waveform?

   A waveform is a visual representation of a testbench.
2. What is a test bench?

   A test bench is a possibility of inputs and outputs in order to help correct our code.
3. Can we replace the 4-input AND gates in the circuit with 2-input AND gates? If yes, how?

   Yes: (((A.B).C).E)