

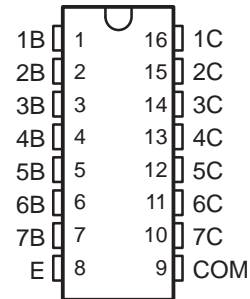
- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Interchangeable With ULN2001A Series

description

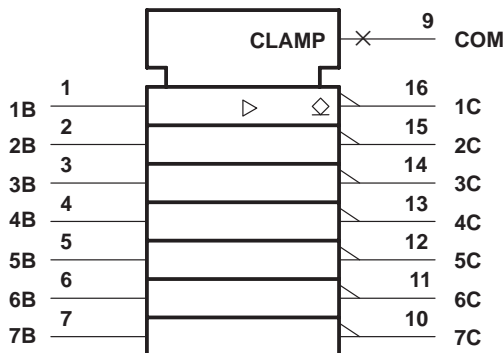
The ULQ2003A is a monolithic high-voltage, high-current Darlington transistor array. The device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULQ2003A has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

The ULQ2003A is offered in standard 16-pin dual in-line (N) and surface-mount (D) packaging. The device is characterized for operation over the junction temperature range of -40°C to 105°C .

D OR N PACKAGE
(TOP VIEW)

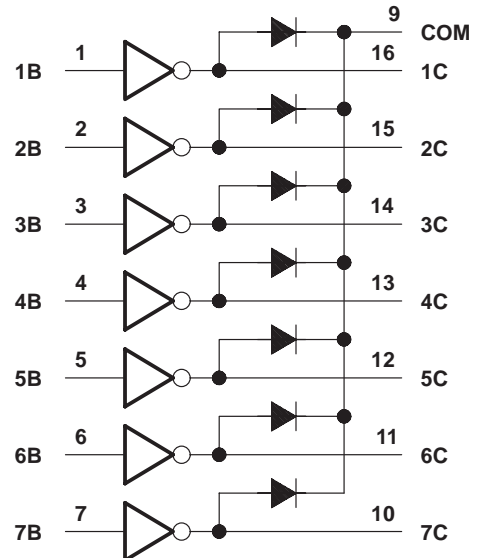


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

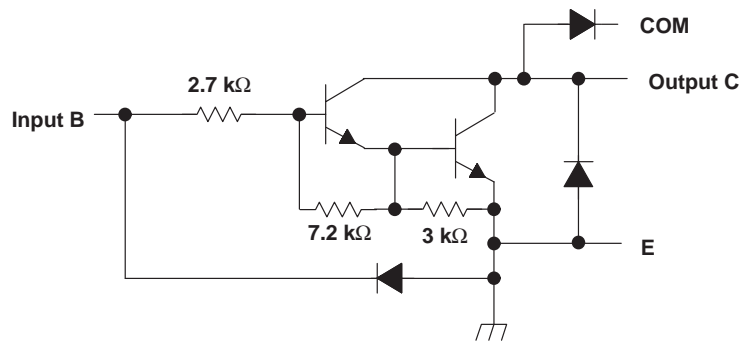
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ULQ2003A
DARLINGTON TRANSISTOR ARRAY

SLIS072 – DECEMBER 1996

schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Collector-emitter voltage	50 V
Clamp diode reverse voltage (see Note 1)	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figures 13 and 14)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	–2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Operating junction temperature range, T_J	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics over operating junction temperature range, $T_J = -40^{\circ}\text{C}$ to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	$V_{CE} = 2\text{ V}$, See Figure 5	$I_C = 200\text{ mA}$			2.7	V
			$I_C = 250\text{ mA}$			2.9	
			$I_C = 300\text{ mA}$			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$I_I = 250\text{ }\mu\text{A}$, See Figure 4	$I_C = 100\text{ mA}$		0.9	1.2	V
			$I_C = 200\text{ mA}$		1	1.4	
			$I_C = 350\text{ mA}$		1.2	1.7	
I_{CEX}	Collector cutoff current	$V_{CE} = 50\text{ V}$, See Figure 1	$I_I = 0$,			100	μA
V_F	Clamp forward voltage	$I_F = 350\text{ mA}$, See Figure 7			1.7	2.2	V
$I_{I(off)}$	Off-state input current	$V_{CE} = 50\text{ V}$, See Figure 2	$I_C = 500\text{ }\mu\text{A}$,	30	65		μA
I_I	Input current	$V_I = 3.85\text{ V}$, See Figure 3			0.93	1.35	mA
I_R	Clamp reverse current	$V_R = 50\text{ V}$, See Figure 6				100	μA
C_i	Input capacitance	$V_I = 0$, $f = 1\text{ MHz}$			15	25	pF

switching characteristics over operating junction temperature, $T_J = -40^{\circ}\text{C}$ to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8			1	10	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1	10	μs
V_{OH}	High-level output voltage after switching	$V_S = 50\text{ V}$, See Figure 9	$I_O \approx 300\text{ mA}$,	$V_S - 500$			mV

PARAMETER MEASUREMENT INFORMATION

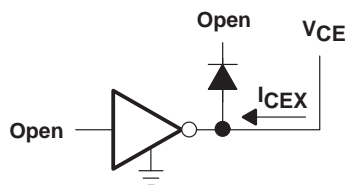


Figure 1. I_{CEX} Test Circuit

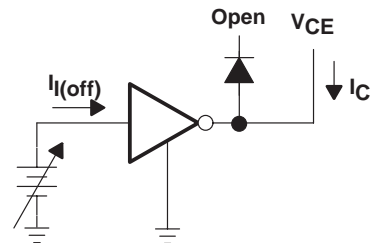


Figure 2. $I_{I(off)}$ Test Circuit

PARAMETER MEASUREMENT INFORMATION

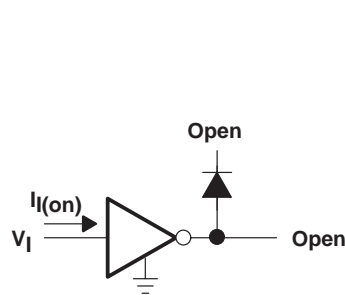


Figure 3. I_I Test Circuit

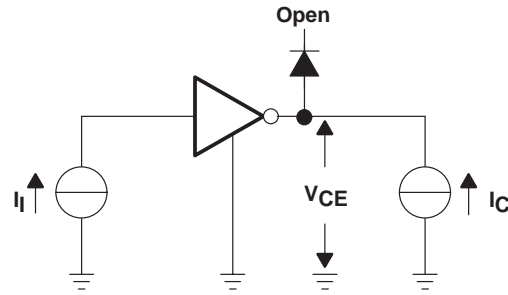


Figure 4. $V_{CE(sat)}$ Test Circuit

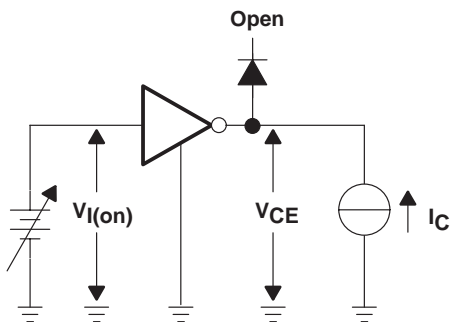


Figure 5. $V_{I(on)}$ Test Circuit

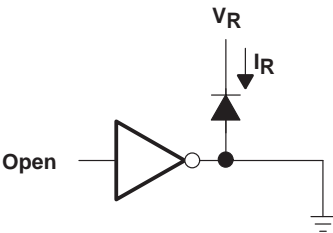


Figure 6. I_R Test Circuit

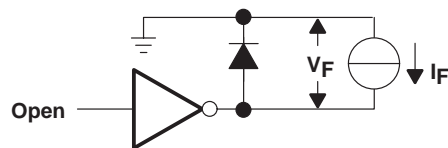
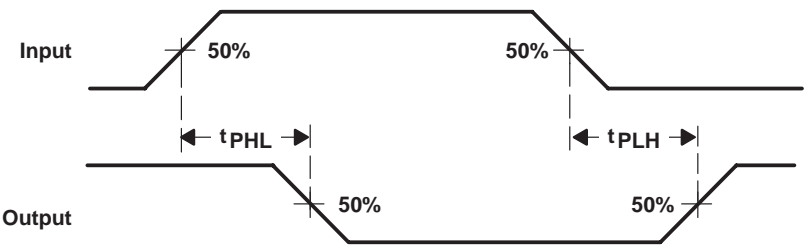


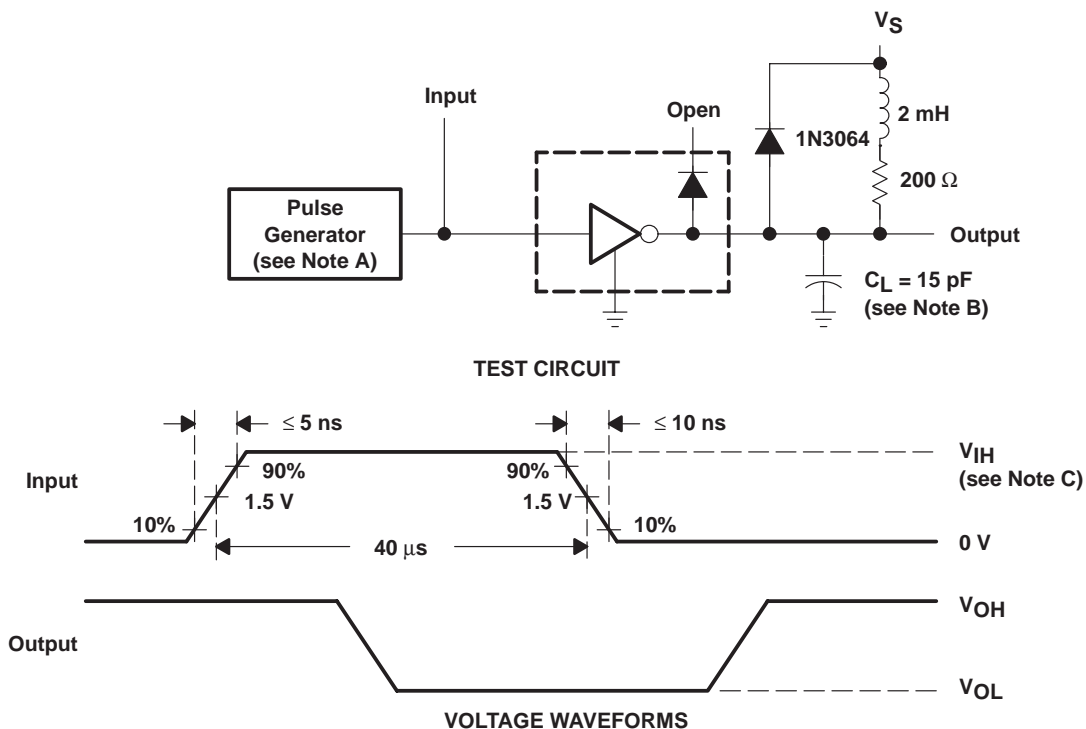
Figure 7. V_F Test Circuit



VOLTAGE WAVEFORMS

Figure 8. Propagation Delay Time Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50\ \Omega$.
 B. C_L includes probe and jig capacitance.
 C. $V_{IH} = 3\text{ V}$

Figure 9. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

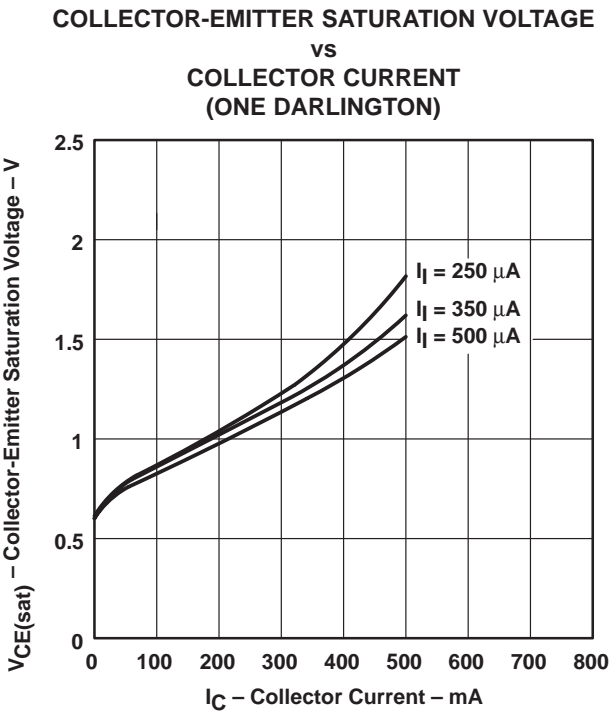


Figure 10

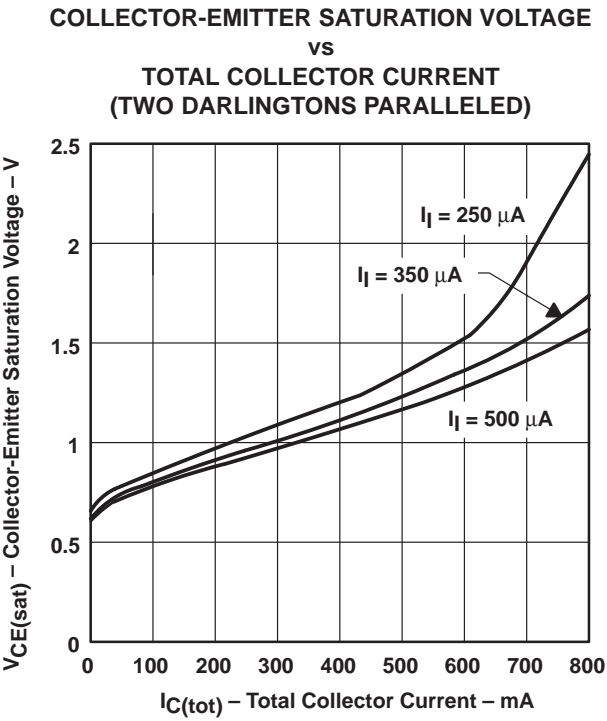


Figure 11

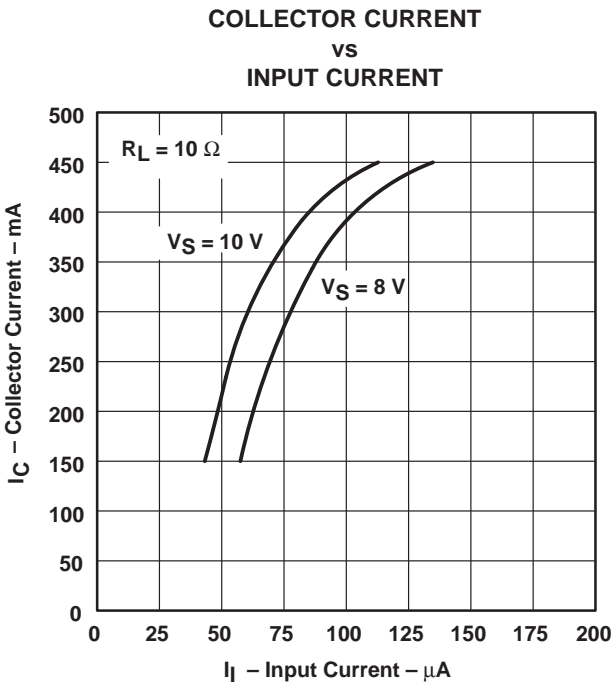


Figure 12

THERMAL INFORMATION

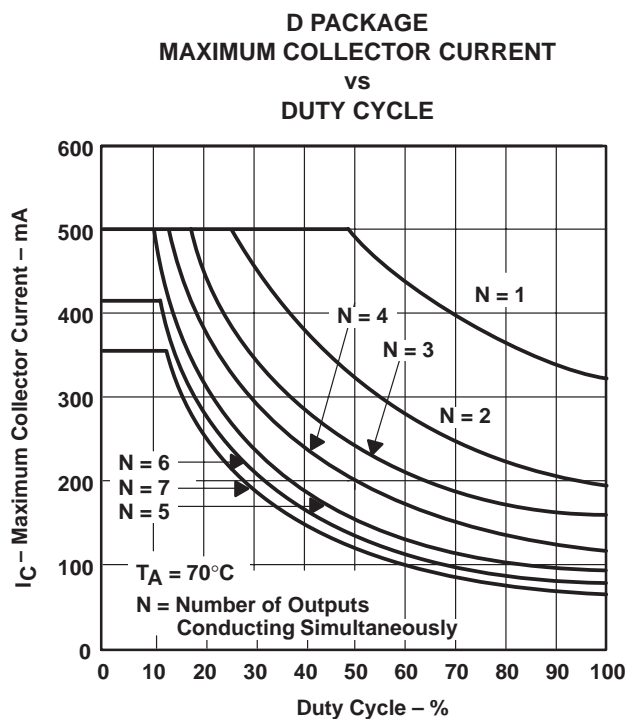


Figure 13

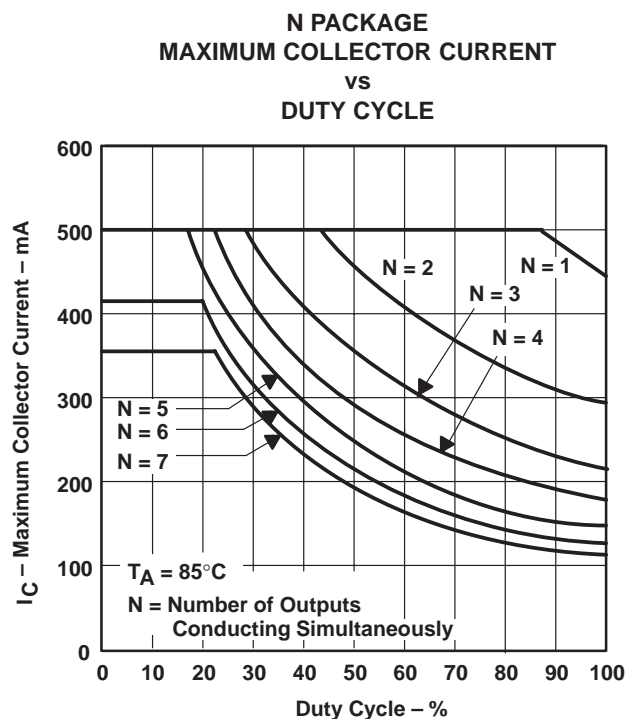


Figure 14

APPLICATION INFORMATION

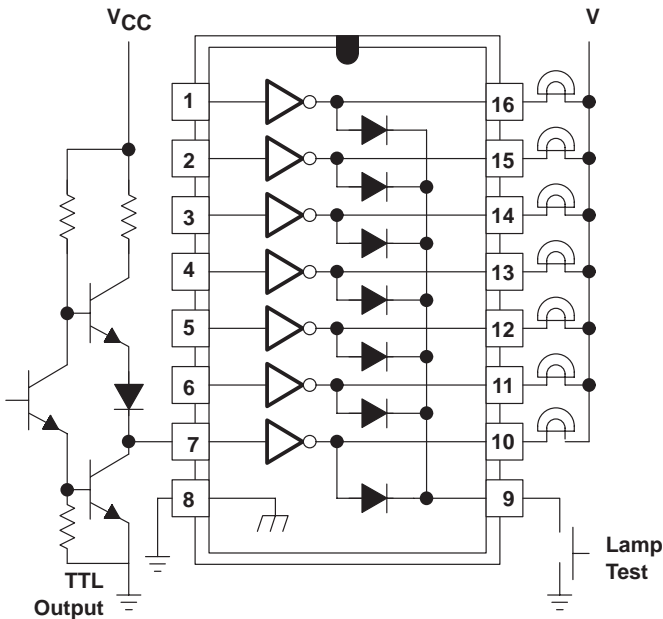


Figure 15. TTL to Load

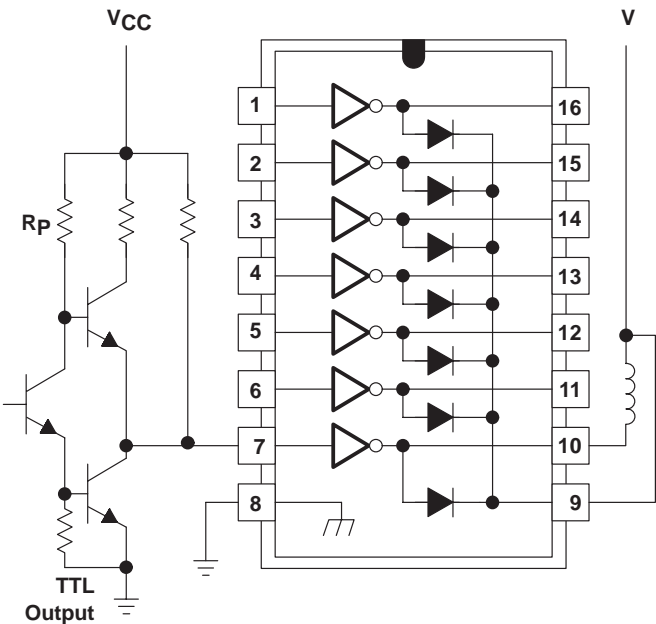


Figure 16. Use of Pullup Resistors to Increase Drive Current

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