Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring 2022-2023

Lab 1

Due date: 31 March 2023, Friday, 23:55
No late submissions

1 Introduction

This laboratory aims to get you familiar with basic logic gates and combinational circuit design. You will simplify the circuit that is explained below and draw the circuit using the Logisim tool with the given gates.

2 IC Pool

In this LAB, you will use the following gates to build the circuit:

- 74LS04 (Inverter)
- 74LS08 (AND)
- 74LS32 (OR)

Note that you can use **only** the gates mentioned above. Usage of other gates is **NOT** allowed.

3 Lab Work

In this assignment, you are expected to perform the operations described in the following section.

3.1 Specifications

Suppose A and B are 2-bit binary **input** numbers and X, Y, Z, and Q are 1-bit binary **output** numbers. A and B are represented with A_1, A_0, B_1 and B_0 bits respectively where A_1 and B_1 are the most significant bits and A_0 and B_0 are the least significant bits of the relevant number. Your circuit will take A and B

as inputs and generate the outputs X, Y, Z, and Q with the following behavior:

$$\mathbf{X} = \begin{cases} 1 & 1 < value < 2.5 \text{ where } value = ((\mathrm{A}+4)\%2) + ((\mathrm{B}+1)/2) - (\mathrm{A}/2) * (\mathrm{B}\%2) \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Y} = \begin{cases} 1 & (\mathrm{A}+5)/(\mathrm{B}+3) * (\mathrm{B} \ll 5) > (\mathrm{A}+3)/(\mathrm{B}+3) * (\mathrm{A} \ll 5) \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Z} = \begin{cases} 1 & \frac{\mathrm{A}+\mathrm{B}}{\mathrm{A}-\mathrm{B}} > -2 \text{ and } \mathrm{A}-\mathrm{B} \neq 0 \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Q} = \begin{cases} 1 & \mathrm{A}-\mathrm{B} > -1 \\ 0 & \text{otherwise} \end{cases}$$

You have to use "input pins" and "output pins" for your inputs and outputs, respectively, from the Toolbar at the top of Logisim. Please set their labels correctly using the following names:

Input pins: A1, A0, B1, B0
Output pins: X, Y, Z, Q

Please, only set "label" property of the "pin" objects, do not add a "label object" onto the Logisim canvas.

Each pin corresponds to a digit in a 2-bit binary number. If it is set, then the value of the digit is 1 if reset, then the value of the digit is 0. Note that '$\ll$' denotes the left shift operator. For instance (4=0b100, 2=0b10) $4 \ll 1$ corresponds to shifting the bits of value 4 one step to the left and results in 8=0b1000. Similarly, $2 \ll 2$ shifts the bits of value 2 two steps to left, which yields 8=0b1000 (shifting 0 times corresponds to not shifting at all, $4 \ll 0 = 4$). In addition, the '%' operator performs the modulo operation.

We highly recommend you simplify your circuitry as much as possible (via the techniques covered in the lectures) for ease of implementation. If our course weren't conducted in an online fashion, you would be supposed to implement your design on breadboards, and the number of ICs that you'd employ would be limited, hence it would be inevitable to simplify your circuits/designs.

3.2 Input Output Examples

1. Suppose $A_1A_0 = 10$ and $B_1B_0 = 01$. In this case, A=2 and B=1 in decimal.
   $value = ((2+4)\%2)+((1+1)/2)-(2/2)*(1\%2) = ((6)\%2)+((2)/2)-(1.0)*(1) = 0+1.0-1.0*1 = 0.0$
   Since $1 < 0.0 < 2.5$ does not hold, the output X is 0.

2. Suppose $A_1A_0 = 11$ and $B_1B_0 = 11$. In this case, A=3 and B=3 in decimal.
   $value = ((3+4)\%2)+((3+1)/2)-(3/2)*(3\%2) = ((7)\%2)+((4)/2)-(1.5)*(1) = 1+2.0-1.5*1 = 1.5$
   Since $1 < 1.5 < 2.5$ holds, the output X is 1.

3. Suppose $A_1A_0 = 00$ and $B_1B_0 = 01$. In this case, A=0 and B=1 in decimal.
   $(0+5)/(1+3) * (1 << 5) > (0+3)/(1+3) * (0 << 5) = 5/4 * 32 > 3/4 * 0 = 1.25 * 32 > 0.75 * 0$
   Since $40.0 > 0.0$ holds, the output Y is 1.

4. Suppose $A_1A_0 = 11$ and $B_1B_0 = 10$. In this case, A=3 and B=2 in decimal.
   $(3+5)/(2+3) * (2 << 5) > (3+3)/(2+3) * (3 << 5) = 8/5 * 64 > 6/5 * 96 = 1.6 * 64 > 1.2 * 96$
   Since $102.4 > 115.2$ does not hold, the output Y is 0.

5. Suppose $A_1A_0 = 01$ and $B_1B_0 = 11$. In this case, A=1 and B=3 in decimal.
   $\frac{1+3}{1-3} > -2 = \frac{4}{-2} > -2 = -2.0 > -2$
   Since $-2.0 > -2$ does not hold, the output Z is 0.

6. Suppose $A_1A_0 = 10$ and $B_1B_0 = 00$. In this case, A=2 and B=0 in decimal.
   $\frac{2+0}{2-0} > -2 = \frac{2}{2} > -2 = 1.0 > -2$
   Since $1.0 > -2$ holds, the output Z is 1.

7. Suppose $A_1A_0 = 11$ and $B_1B_0 = 11$. In this case, A=3 and B=3 in decimal.
   $\frac{3+3}{3-3} > -2 = \frac{6}{0} > -2$
   Since the denominator is 0, the output Z is 0.

8. Suppose $A_1A_0 = 01$ and $B_1B_0 = 00$. In this case, A=1 and B=0 in decimal.
   $1 - 0 > -1 = 1 > -1$
   Since $1 > -1$ holds, the output Q is 1.

9. Suppose $A_1A_0 = 00$ and $B_1B_0 = 11$. In this case, A=0 and B=3 in decimal.
   $0 - 3 > -1 = -3 > -1$
   Since $-3 > -1$ does not hold, the output Q is 0.

4 Deliverables

1. Please submit the circuit prepared in Logisim with the name `e1234567.circ`, by the specified deadline. Please do not forget to replace `e1234567` with your 7-digit student ID. The evaluation of the submission will be carried out with a black-box test. **You should use the CENG version of Logisim which is available on the ODTUClass course page. Circuits designed with other Logisim versions, other tools, or not named properly will not be graded!**

5 Cheating Policy

All the lab work should be **individual** and there is a policy of zero tolerance for cheating. Please see the course website for further information about the cheating policy.

6 References

CENG Logism Version.