Mahshid Shahmohammadian

CONTACT

ms4323@drexel.edu

Drexel College of Computing and Informatics, Research Room 1143
www.cs.drexel.edu/~ms4323

TECHNICAL SKILLS

Engineering Software:

- Vivado/ISE Xilinx
- MATLAB/Simulink/System Generator Xilinx
- ModelSim/Xcelium Simulator/SimVision
- Genus Synthesis/Joules RTL Power/Virtuso/Calibre
- Design Compiler/SoC Encounter
- PSpice/OrCAD

Programming Languages:

- VHDL/Verilog/SystemVerilog
- C/C++
- Python
- Haskell
- TCL/Shell

Operating Systems:

- Linux/macOS/Windows

HONORS AND AWARDS

Member of Drexel Upsilon Pi Epsilon of International Honor Society for Computing and Information Disciplines

Travel Awards:

- Drexel University College of Computing and Informatics, 2019
- IEEE Circuits and Systems (CAS), 2020
- International Conference on Electronics Circuits and Systems (ICECS), 2019
- Grad-Cohort Workshop CRA-W'17, 19

Grace Hopper Celebration: GHC'17 AnitaB. Scholar, GHC'19 and vGHC'20 Speaker in Computer Architecture and Hardware Engineering poster session

CAREER OBJECTIVE

Seeking Hardware Software Co-Design, FPGA or ASIC Design Engineering positions in the field of digital signal processing and digital communication systems which will leverage my experiences and contributions in collaborative projects.

EXPERIENCE

Maxlinear Inc., Carlsbad, CA

ASIC Design Intern: Power consumption optimization of optical receiver equalizer feed-forward filters, Summer 2019

- Designing a generic FIR filter in Verilog and SystemVerilog tested against an equivalent reference model in C
- Gate-level post-synthesis simulation of several inputs/coefficients number representations and clock rate scenarios
- Estimating power consumption with certain stimulus window for different scenarios
- Power consumption reduction by about 20 percent based on the estimated power numbers gathered from different cases of input/coefficients number representation affecting multiplication and accumulation operations in FIR filters
- Input and coefficient data generated randomly, sinusoid, and using real OFDM data with 500MHZ clock rate

Drexel University, Philadelphia, PA

Graduate Research Assistant, Sep 2016-July 2021

- IP generation of DSP algorithms such as FFT, Viterbi Decoder, and CORDIC from functional domain-specific languages such as Haskell SPIRAL and Ziria with efficient performance
- Efficient synthesis of OFDM PHY pipeline components implementations to Virtex 7 Xilinx FPGA from high-level functional language Kansas Lava, an embedded language in Haskell

Teaching Assistant of System Architecture Course, Fall 2016

Iran Telecommunication Company, Tehran, Iran

Full-time Intern, Summer 2015

EDUCATION

Drexel University — Philadelphia, PA

Ph.D. in Computer Science, GPA 3.87, 2021

Amirkabir University of Technology (Tehran Polytechnic) — Tehran, Iran

Bachelor of Science in Computer Engineering, GPA 16.47/20, 2015

Relevant Courses: Logic Design, Advanced Computer Architecture, VLSI Design, Electronic Circuits, Signals and Systems, Collaborative Intelligent Radio Networks, Artificial Intelligence, Machine Learning

Certificates: Digital Signal Processing (EPFL), Static Timing Analysis (VSD)