Stable high-order delta-sigma DACs

Peter Kiss, Jesus Arias, Dandan Li, and Vito Boccuzzi

***Abstract*— Stability analysis of high-order delta-sigma loops is a challenge. In this brief, a sufficient design criterion is presented for high-order multibit error-feedback DACs which are especially suitable for high-speed operation. This analytical criterion might be too conservative, but it allows the design of stable, robust, and high-resolution delta-sigma DACs. Both analytical and numerical analysis are performed for verification. Also, experimental results of a discrete-component multiplier-free prototype demonstrate 10-bit operation at a very low oversampling ratio of 4.**

***Index Terms*— data conversion, DAC, delta sigma, sigma delta, stable, stability, error feedback, high order, high speed.**

I. High-order delta-sigma modulators

Since a delta-sigma ($\Delta\Sigma$) modulator uses oversampling and quantization error shaping, it trades speed for resolution, and analog-circuit accuracy for digital-circuit complexity. A possible way to obtain a high-resolution and high-speed delta-sigma analog-to-digital converter (ADC) or digital-to-analog converter (DAC) is to use a high-order or/and multibit modulator. High-order quantization error shaping can be achieved by either single-loop or multi-loop (i.e., cascaded or MASH) architectures [1].

The choice of the quantization error or quantization noise transfer function (NTF) plays a significant role in the achievable performance of the modulator. While the in-band attenuation of the NTF is provided by its zeros, the out-of-band gain (OBG) of the NTF is controlled by its poles. Reducing the OBG improves the loop's stability, but it increases the inband noise, thus deteriorating the signal-to-noise ratio (SNR) of the modulator. For high-order loops (i.e., larger than one) it is possible to gain more performance by moving out the zeros of the NTF from DC, and arranging them in the signal band to provide maximal noise suppression for a given oversampling ratio (OSR) [2]. Also, high-order modulators are prone to become unstable for large input signals [1, Chaps. 4–5].

Due to the presence of a nonlinear truncator or quantizer[1] in the system, the stability analysis of high-order loops (i.e., larger than two) is a challenge. "Unstable" means that the modulator exhibits large, although not necessarily unbounded, states and a poor SNR compared to those predicted by linear models [1, Sec. 4.1]. Many excellent papers deal with the issue of stability, e.g., [1–11].

The chain of integrators or accumulators with feedback or feedforward summation are popular topologies for delta-sigma ADCs (Fig. 1(a)) and DACs (Fig. 1(b)), respectively. Let us refer to these as *output-feedback* (OF) modulators. To ensure stability, a conservative empirical rule of Lee [4] or/and the root-locus method [5] along with extensive simulations must be used. Lee's rule applies for single-bit modulators and it requires an OBG of the NTF less than 1.5. Several functional ICs [12], [13] demonstrate that using Lee's rule yields to stable modulators. For multibit high-order designs a more relaxed value, e.g., of 3.5 [14], is sufficient for stability. In any case, while this requirement empirically ensures stability, it drastically limits the achievable performance of single-loop high-order modulators; moreover, precaution and lengthy simulations are necessary in their design.

The *error-feedback* (EF) topology (Fig. 1(c)) is not suitable for delta-sigma ADCs since the imperfections of the analog loop filter $H(z)$ would enter the critical input node and adversely affect the output. However, this drawback does not exist in digital modulator loops. Therefore, it is widely used in delta-sigma DACs [1], [15], [16] and fractional-N PLLs [17]. For high-order loop filters internal limiters are often used which protect the overflow of the internal signals [16]; also, the stability of the design needs to be carefully verified by extensive simulations.

A sufficient stability test for EF modulators based on the $\mathcal{L}$-norm of the impulse response of the loop filter $h(t)$ was proposed by Schreier, which determined just how many quantization levels are needed to keep the delta-sigma loop stable [6]. Norsworthy extended this $\mathcal{L}$-norm test [6] to include dither signal as well [7], [1, Sec. 3.14.1]. Here, another sufficient analytical stability criterion is proposed in Sec. II based on a trivial analysis [18]. Practical considerations are presented in Sec. III. Finally, supporting simulation and experimental results are shown in Secs. IV and V, respectively.

II. Analytical stability analysis

The block diagram of an EF $\Delta\Sigma$ DAC is shown in Fig. 1(c). The truncator (TRUNC) provides the most-significant bits (MSBs) for the following DAC, and feeds the least-significant bits (LSBs) to the digital loop filter $H(z)$. Using the additive white-noise model [1, Sec. 2.3] for the truncator, which replaces a deterministic nonlinearity with a stochastic linear system, we have

$$\begin{aligned} Y_d(z) &= X_d(z) + (1 - H(z))\, E_t(z) \\ &= STF(z)\, X_d(z) + NTF(z)\, E_t(z), \end{aligned} \tag{1}$$

where $STF(z) = 1$ is the signal transfer function and $NTF(z) = 1 - H(z)$ is the truncation error (or truncation noise) transfer function.

In order to achieve low truncation error energy in the low-frequency signal band, $NTF(z)$ should have high-pass characteristics. For example, an Lth-order differentiator $(1 - z^{-1})^L$ may be chosen as $NTF(z)$. L also determines the order of the delta-sigma loop. All the zeros of this FIR $NTF(z)$ sit at DC. Therefore, OBG is 2^L, which is the maximum possible OBG value for an Lth-order modulator. When optimized zeros are used in an FIR $NTF(z)$, the OBG stays about 2^L, only slightly smaller. However, OF modulators require a much smaller OBG value, e.g., 3.5 [14], for stability. Therefore, finite-valued poles should be added to $NTF(z)$, transforming it into an IIR filter.

A. Analysis of EF modulators

When $NTF(z)$ is an FIR transfer function, $H(z)$ is also an FIR function for EF modulators (eq. (1)). Therefore, there is no accumulation in $H(z)$ as opposed to the case of OF topologies. The only accumulation occurs during the addition at the input node, but this is directly followed by the truncation operation. Therefore, the bit length of *every* internal signal can be accurately predicted analytically without the need of numerical analysis.

Let us assume that the FIR loop filter $H(z)$ adds m bits to the bit length. The input summation adds one more bit at most. In order to keep all internal signals bounded, whatever enters the loop also needs to exit, so y_d should have $m+1$ bits at least (i.e., 'm' due to $H(z)$, and '1' due to the input summation). By notation the input x_d has k_x bits and the feedback e_h has k_e bits (Fig. 2). If $k_e \le k_x$ holds, which is a valid initial condition, and y_d is kept to its minimal value of $m+1$, then e_i will have $k_x + 1$ bits at most, and $k_x - m$ LSBs will be fed back to the loop. This leads to e_h of k_x bits. Therefore,

Manuscript received January 15, 2003; revised September 15, 2003. This paper was published in the *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 51, no. 1, pp. 200–205, January 2004.

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[1]"Quantizers" and "truncators," and "integrators" and "accumulators" are used in delta-sigma ADCs and DACs, respectively.

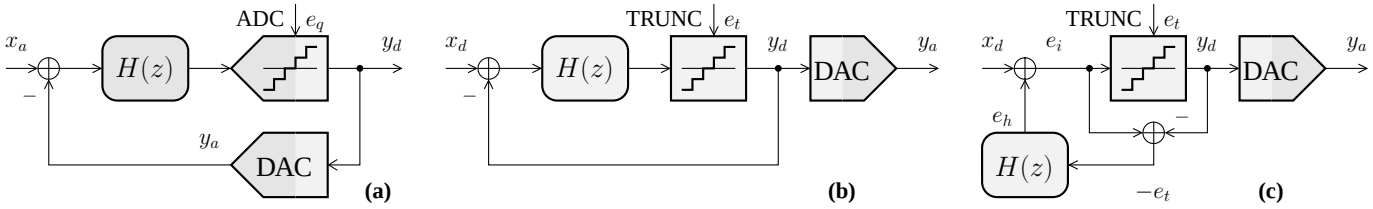

Fig. 1. Single-loop delta-sigma modulator topologies: **(a)** output-feedback ADC; **(b)** output-feedback DAC; **(c)** error-feedback DAC.

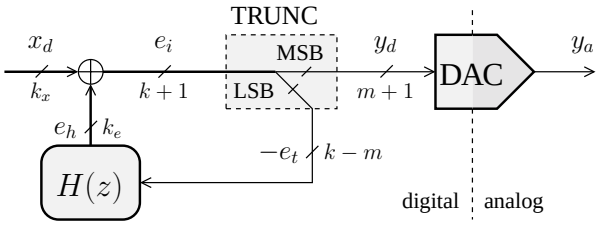

Fig. 2. Error-feedback digital-to-analog converter (details).

$k_x = k_e = k$ holds for steady state, and all internal signals are bounded indeed, as shown in Fig. 2. Note that $k > m$ for practical reasons, so $k - m$ will not become negative.

In other words, a **sufficient stability criterion** can be formulated as follows: an error-feedback modulator with a truncator of $m+1$ bits and an FIR loop filter $H(z)$, which contributes to a m-bit increase in the dataflow, is stable.

B. Examples of stable modulators

Example #1: Let us consider a Lth-order EF loop with $NTF(z) = (1 - z^{-1})^L$ and $H(z) = 1 - NTF(z)$. In the worst-case scenario, a ± 1 alternating sequence applied to $(1 - z^{-1})^L$ leads to 2^L, that is, to L-bit output. Therefore, $H(z)$ contributes less than L bits to the dataflow. In other words, the lowest value for m is L, so if y_d has $m + 1 = L + 1$ bits, then all internal signals are bounded, i.e., the Lth-order loop is stable. In case of a 4th-order loop with $NTF(z) = (1 - z^{-1})^4$ and $H(z) = z^{-1}(4 - 6z^{-1} + 4z^{-2} - z^{-3})$, it turns out that m is 4, and y_d has 5 bits according to the criterion described above (summarized in Fig. 3).

Example #2: Let us consider a Lth-order EF loop with optimized-zeroed FIR $NTF(z)$. Since the zeroes stay inside the unit circle, the contribution of $H(z) = 1 - NTF(z)$ does not exceed L bits. In case of a 4th-order loop and $OSR = 8$, a $NTF(z)$ of $(1 - 1.98z^{-1} + z^{-2}) \cdot (1 - 1.88z^{-1} + z^{-2})$ results [2]. Again, m is 4 and if y_d has 5 bits, the modulator is stable based on the criterion describe above.

C. Discussion

The **sufficient stability criterion** eliminates the need of reducing the OBG of the Lth-order FIR NTF and guarantees stability if the number of bits in the truncator are at least $L+1$. Using this criterion one can design EF modulators with aggressive noise shaping without sacrificing stability, and this leads to high SNR.

Note that the rational described in Sec. II-A treats the truncator as a nonlinear circuit, so it does not rely on the additive white-noise model used in eq. (1). Also, note that this brief proposes a sufficient analytical criterion, not a both necessary *and* sufficient criterion. In other words, using $L+1$ bits in the truncator is sufficient to keep all internal signals bounded, thus to keep the high-order loop stable. However, it is too conservative. To find a general necessary and sufficient stability criterion for high-order delta-sigma modulators is far beyond the scope of this brief. Some excellent discussions on stability boundaries can be found in, e.g., [1, Chap. 4–5].

Hardware-efficient example:

- DC-zeroed FIR $NTF(z) = (1 - z^{-1})^L$ and $H(z) = 1 - NTF(z)$
  $m \le L \quad \Rightarrow \quad$ if y_d has $L+1$ bits $\quad \rightarrow \quad$ stable $\Delta\Sigma$.
- For $L = 4$:
  $NTF(z) = (1 - z^{-1})^4 = (1 - 2\,z^{-1} + z^{-2}) \cdot (1 - 2\,z^{-1} + z^{-2})$
  and $H(z) = z^{-1}\,(4 - 6\,z^{-1} + 4\,z^{-2} - z^{-3})$
  $m \le 4 \quad \Rightarrow \quad$ if y_d has 5 bits $\quad \rightarrow \quad$ stable $\Delta\Sigma$.

Best-performance example:

- optimized-zeroed FIR $NTF(z)$ and $H(z) = 1 - NTF(z)$
  $m < L \quad \Rightarrow \quad$ if y_d has $L+1$ bits $\quad \rightarrow \quad$ stable $\Delta\Sigma$.
- For $L = 4$ and $OSR = 8$:
  $NTF(z) = (1 - 1.98\,z^{-1} + z^{-2}) \cdot (1 - 1.88\,z^{-1} + z^{-2})$
  and $H(z) = z^{-1}\,(3.86 - 5.72\,z^{-1} + 3.86\,z^{-2} - z^{-3})$
  $m < 4 \quad \Rightarrow \quad$ if y_d has 5 bits $\quad \rightarrow \quad$ stable $\Delta\Sigma$.

Fig. 3. Two examples of stable EF modulators (summary of Sec. II-B).

Again, an EF modulator with $(1-z^{-1})^L$ FIR $NTF(z)$ and $L+1$ bits is stable. This stable EF modulator has and OBG of 2^L. In general, reducing OBG *improves* stability [1, Sec. 5.5]. Therefore, it is plausible to assume that reducing OBG of this modulator by adding finite-valued poles to its $NTF(z)$ (i.e., turning the initially FIR NTF into an IIR filter) does not worsen its stability. In other words, one expects a stable Lth-order $(L+1)$-bit EF modulator for *all* possible OBG values. This last statement is an intuitive extension of the sufficient stability criterion; however, the authors cannot provide an analytical proof for it.

III. Practical considerations

Criterion-based EF modulators require multibit digital-to-analog conversion. Since 1-bit DACs are inherently linear, it is usually desired to obtain a single-bit dataflow at the digital output y_d. However, highly-linear multibit DACs are available [1, Chap. 8], which can make the circuit practical and useful. Another possibility is to use such a high-order modulator in a cascade configuration [15].

Both the criterion-based high-order EF modulator and the MASH topology [19–21] are stable, and generate high-order noise-shaped, multibit output. Compared to the MASH, the criterion-based high-order EF modulator is implemented within a single loop and can be made more hardware efficient and to draw less power.

Due to the use of aggressive NTF, the amount of out-of-band truncation error of a criterion-based EF modulator is larger than the OF modulator. This imposes slightly more stringent linearity requirements on the analog DAC circuitry. Also, the analog reconstruction low-pass filter, which follows the DAC, may need to provide increased selectivity.

Finally, the use of optimized zeroes may necessitate expensive multipliers in the digital circuit implementation of $H(z)$, while implementing pure differentiator NTFs are free of multipliers. However,

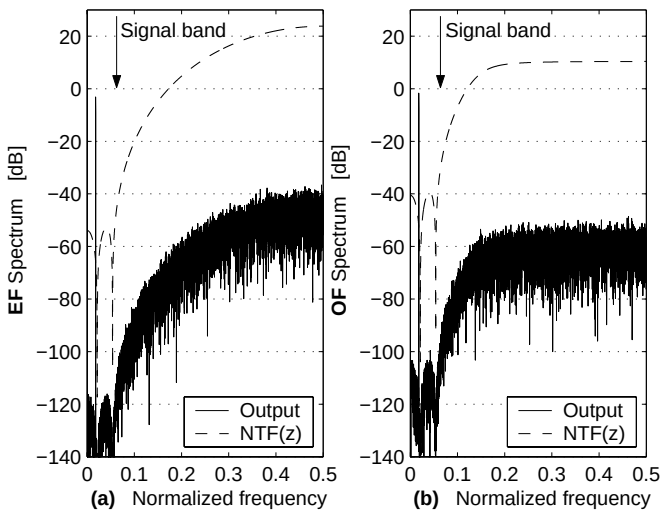

Fig. 4. Simulated FFTs of 4th-order 5-bit modulators for $OSR = 8$, **(a)** EF modulator: $SNR = 93.1$ dB; **(b)** OF modulator: $SNR = 81.2$ dB.

the design example presented in Sec. V demonstrates that even optimized-zeroed NTFs can be effectively implemented by simple, multiplier-free digital circuits.

IV. Simulation results

To illustrate the behavior of the criterion-based high-order EF DAC (Fig. 2), first a 4th-order modulator was simulated in Matlab. The optimized zeroes of the NTF were designed using Schreier's toolbox [22]. As expected, it remained stable for several million samples. A 2^{14}-point Hann-windowed FFT of the 5-bit output data stream y_d is shown in Fig. 4(a). The digital input x_d was quantized to $k_x = 24$ bits. Since the 5-bit truncation error was aggressively pushed out of band with the 4th-order FIR NTF, a peak SNR of 93.1 dB was obtained even for a low value of the OSR of 8.

Fig. 4(b) shows the output spectrum of a similar 4th-order 5-bit DAC, but designed using an OF topology (Fig. 1(b)). The OBG of the NTF had to be limited to 3.3 in order to keep the loop stable. This modulator achieved 81.2 dB peak SNR, about 12 dB lower than the EF architecture. The z-domain expressions of the EF and OF $NTF(z)$-s are given by:

$$\begin{cases} \text{EF:}\ NTF(z) &= \frac{(1-1.98\,z^{-1}+1.00\,z^{-2})\,(1-1.88\,z^{-1}+1.00\,z^{-2})}{1} \\ \text{OF:}\ NTF(z) &= \frac{(1-1.98\,z^{-1}+1.00\,z^{-2})\,(1-1.88\,z^{-1}+1.00\,z^{-2})}{(1-0.82\,z^{-1}+0.19\,z^{-2})\,(1-0.88\,z^{-1}+0.46\,z^{-2})} \end{cases}$$

Fig. 5 compares the achievable performance of two 4th-order 5-bit optimized-zeroed EF and OF modulators. It shows the peak SNR and the corresponding input-signal amplitude A_u in function of OBG (similar type of graphs can be found in [2]). The OF modulator's performance abruptly drops when $OBG > 3.6$; such OF system cannot sustain stable operation for $OBG > 4.1$ at all. Note that high-OBG OF modulators become unstable if the input signal includes sharp transitions. Even if the input signal is band limited, the OF modulator can become unstable during start-up and it never recovers. On the other hand, the EF modulator remains stable for the whole possible range of OBG with a small decrease of the available input range to about 0.7 $\frac{V}{V}$ (normalized to full scale) as shown in Fig. 5. EF modulators are insensitive to sharp transitions in the input signal and to start-up conditions. The best SNR scenarios for these two 4th-order 5-bit optimized-zeroed EF and OF modulators were shown in Figs. 4(a) and (b), respectively.

The above described stability experiment was performed for a wide range of OSRs, loop orders (L), and corresponding number

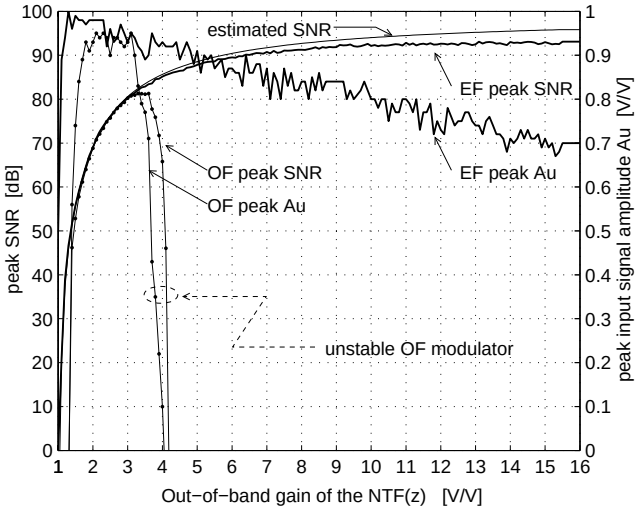

Fig. 5. Stability "test" for EF *versus* OF modulators.

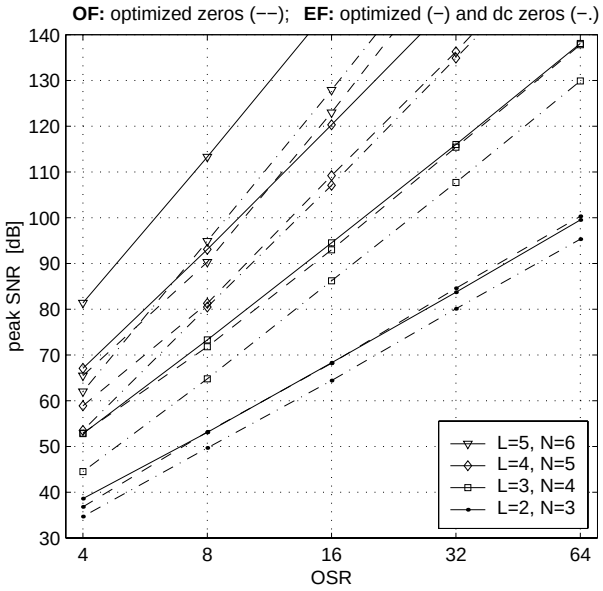

Fig. 6. Achievable performance by various modulators.

TABLE I
Approximative SNR comparison (data from Fig. 6).

ΔSNR [dB]	$L=2$ $N=3$	$L=3$ $N=4$	$L=4$ $N=5$	$L=5$ $N=6$
EF_{opt} *vs.* OF_{opt}	± 0	$+1$	$+10$	$+20$
EF_{dc} *vs.* OF_{opt}	-4	-7	-2	$+4$

of bits ($N = L + 1$). It was confirmed that the EF modulator remains stable for large input signals (i.e., $A_u > 0.5\ \frac{V}{V}$ [2]) for the whole range of $OBG = 1 \ldots 2^L$. It achieved the best performance for $OBG \simeq 2^L$, when the NTF is an FIR transfer function. The comparative peak SNR values are shown in Fig. 6 for EF and OF modulators with optimized zeros. A DC-zeroed EF modulator with $NTF(z) = (1 - z^{-1})^L$ might be attractive, since it can be implemented with simple digital circuitry, so it was also plotted on Fig. 6. For $L = 2$ the OF modulator is also stable, so using an EF modulator cannot improve the performance. For $L \geq 3$, however, the EF modulator clearly outperforms the OF modulator, since the latter's performance is limited by the loop's fragile stability.

A coarse quantitative comparison is shown in Tab. I. It shows the SNR-gain of the optimized-zeroed EF modulator (EF_{opt}) *versus* the optimized-zeroed OF modulator (OF_{opt}) for $L = 2 \ldots 5$ and

$N = 3 \ldots 6$. Also, DC-zeroed EF modulators (EF_{dc}) were included into the comparison. Since ΔSNR varies with OSR, an average rounded value was included into Tab. I. For example, a 4th-order 5-bit EF_{dc} modulator lacks only about 2 dB of SNR compared to OF_{opt}, but EF_{dc} is significantly simpler to implement than OF_{opt}. Again, when a 4th-order 5-bit modulator is implemented by EF_{opt} topology, about 10 dB of SNR can be gained over OF_{opt} based on Tab. I (Figs. 4 and 6 indicate the "precise" value of $\Delta SNR = 11.9$ dB).

Due to the nonlinear behavior of the modulators and, also, numerical errors affect the results, the given values are approximations. However, Fig. 6 and Tab. I show a dramatic improvement in the SNR by using the proposed criterion-based EF modulators.

V. Design example

A 4th-order 5-bit criterion-based EF DAC prototype was built from discrete components. This design example aims to address experimentally the stability of the proposed high-order loop and to investigate the detrimental effects of analog circuit imperfections in the multibit DAC. The design and analysis of an appropriate integrated analog reconstruction low-pass filter is beyond the scope of this brief.

A. Experimental setup

The core of this EF DAC is the digital delta-sigma modulator. Its 24-bit input x_d is provided by a digital sinusoidal generator and its 5-bit output y_d is scrambled before being converted into an analog signal y_a by a 32-element (i.e., 5-bit) DAC (Fig. 7(a)).

The digital implementation of the proposed optimized-zeroed [2] 4th-order 5-bit EF modulator is shown on Fig. 7(b). A very low OSR of 4 is targeted aiming to demonstrate 10-bit accuracy for high-speed applications. Therefore, the loop filter is given by $H(z) = 3.4883\,z^{-1} - 5.0071\,z^{-2} + 3.4883\,z^{-3} - z^{-4}$ (from eq. (1) and using [22]). Expensive multipliers can be avoided since these coefficients are easy to implement by shifting and adding/subtracting binary operations, i.e., $3.4883 \approx 4 - 1/2 - 1/64$ and $-5.0071 \approx -4 - 1$ (Fig. 7(b)). The approximation error of the coefficients is small enough to avoid a significant change of the resulting $NTF(z)$; this approximation leads to about 0.1 dB SNR penalty.

The truncator is a mere splitting of bits. The five MSBs constitutes the modulator's output y_d, while the 19-LSB truncation error $-e_t$ is fed back into the loop filter $H(z)$ (Fig. 7(b)).

To handle the nonlinearities of the multibit DAC due to mismatch between its elements [1], implemented by resistors of 1% tolerance, data-weighted averaging (DWA) [23] was used. Since 10-bit of accuracy was targeted, the first-order mismatch shaping offered by DWA was sufficient. To achieve a higher signal-to-noise-and-distortion ratio ($SNDR$) when $OSR > 4$, e.g., second-order mismatch shaping [1, Sec. 8.3] can be used.

The DWA scrambler rotates the thermometer-coded word using a barrel shifter (ROT in Fig. 7(c)). A 5-bit register (REG_1) holds the rotation index and this index is incremented by the output value of each sample y_d. Due to the circular nature of the rotator, the index adder truncates its output to 5 bits. The last register (REG_2) of the scrambler avoids data-dependent delays in the signal path.

The digital logic (i.e., generator, modulator and scrambler) was implemented using integer arithmetic on a x86 processor. The 32-line thermometer-coded digital output y_s was interfaced with the 32-resistor "analog" DAC using the parallel port of a personal computer (PC) and eight 8-bit buffers (Fig. 7(d)). The common node of the resistors provides the analog output y_a of the $\Delta\Sigma$ DAC. The timing of the circuit is controlled by an accurate external clock (CLK).

The discrete-component experimental setup mimics an integrated IC scenario. Currently, the sampling rate of the DAC is limited to

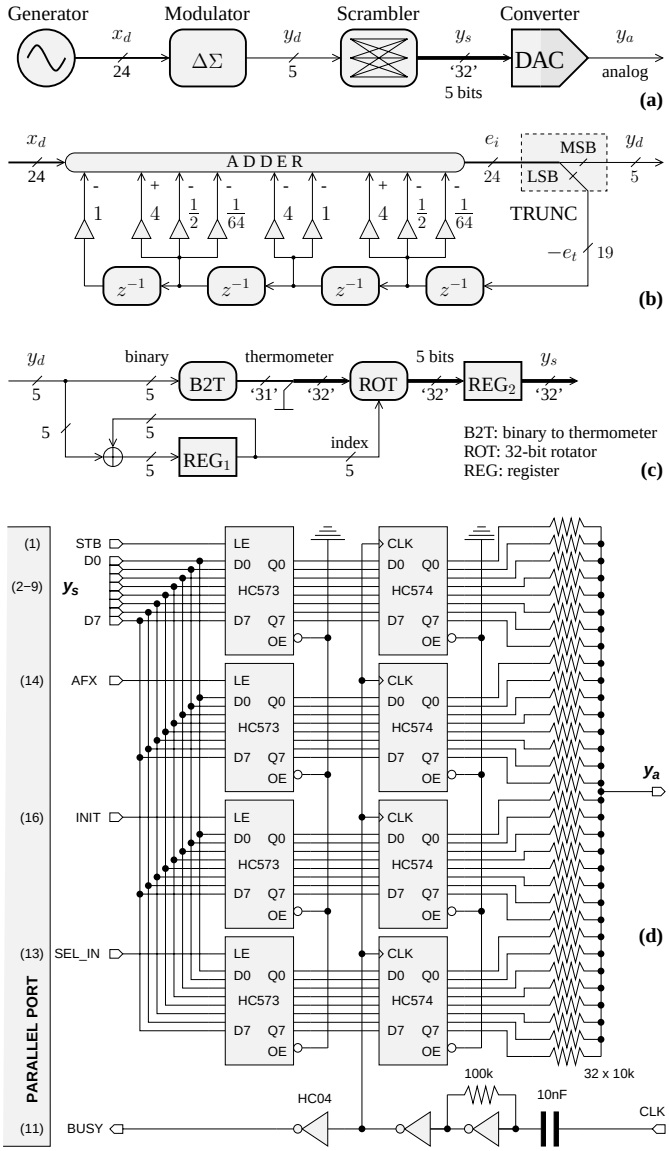

Fig. 7. Implementation of a criterion-based 4th-order 5-bit EF DAC: **(a)** block diagram; **(b)** digital EF modulator; **(c)** DWA scrambler; **(d)** 32-element resistive DAC interfaced to the PC's parallel port.

64 kHz by the parallel port of the PC used in the experiment. To increase the sampling rate, the digital logic is also implemented on a Xilinx Virtex 300 FPGA using *A Stream Compiler* (ASC) developed at Bell Laboratories, based on [24]. The maximum clock rate supported by the FPGA card is 100 MHz. Due to the simplicity of the digital logic (Fig. 7) and the optimizations performed by ASC [24], a 70 MHz output sampling rate is obtained running on the Xilinx Virtex 300 FPGA. The analog part of the FPGA setup is still under development, and analog measurements are expected to confirm the feasibility of the proposed approach.

B. Experimental results

This section presents the experimental results of the proposed 4th-order 5-bit EF DAC with optimized zeroes (Fig. 7). The effective sampling rate was 64 kHz. The high-order loop remained stable after several hours of operation. The analog output y_a of the multibit DAC was captured by a Rohde&Schwarz FSEA spectrum analyzer. The acquired spectra were post processed in a PC to obtain the $SNDR$ values in a 8-kHz (i.e., $OSR = 4$) bandwidth.

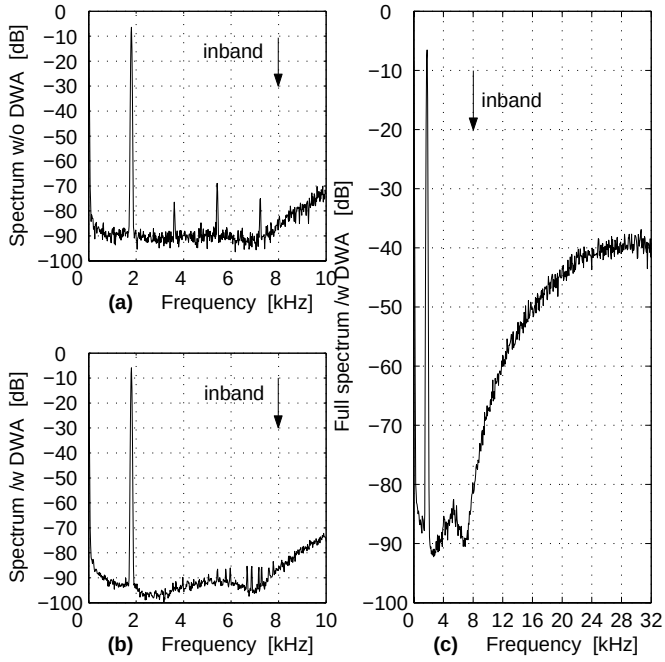

Fig. 8. Measured spectra of a criterion-based 4th-order 5-bit EF modulator for $OSR = 4$, **(a)** without DWA: $SNDR = 58.7$ dB; **(b)** with DWA: $SNDR = 64.1$ dB; **(c)** full spectrum with DWA.

Fig. 8(a) shows the in-band output spectrum without using the DWA scrambler (resolution bandwidth RBW: 30 Hz). Large harmonics and increased noise floor can be observed, which limit the $SNDR$ to 58.7 dB. By activating the DWA scrambler [23] the harmonic content becomes negligible and the noise floor is significantly lower (Fig. 8(b), RBW: 30 Hz). The two $NTF(z)$ minima can be clearly seen. A few small in-band spurious tones are present around the second $NTF(z)$ zero due to idle tones of first-order mismatch shaping. These spurs can be reduced by, e.g., using second-order mismatch shaping [1, Sec. 8.3]. A $SNDR$ of 64.1 dB was obtained. This measured value is only 1.8 dB less than the SNR obtained by simulations assuming floating point arithmetic and ideal analog DAC (Fig. 6). Finally, Fig. 8(c) shows the full $0 \ldots 32$-kHz 4th-order noise-shaped spectrum of the DWA-scrambled DAC, but with an increased RBW of 100 Hz.

VI. Conclusion

In this brief stable high-order error-feedback delta-sigma DACs were designed based on the proposed sufficient stability criterion. This analytical criterion claims that an error-feedback modulator with Lth-order FIR noise transfer function and $L + 1$ bits is stable. Such error-feedback DACs are robust and achieve better performance than output-feedback architectures. Due to aggressive noise shaping and multibit truncation, as simulations showed, they can achieve high resolution even for low oversampling ratios.

A discrete-component 4th-order 5-bit prototype was built for further verification. It was implemented by simple, multiplier-free digital circuits connected to 32 parallel resistors. The high-order loop remained stable after several hours of operation. 64.1 dB of $SNDR$ was measured for a very low oversampling ratio of 4.

Acknowledgement

The authors would like to acknowledge M. Banu, P. Kroon, J. Markus, O. Mencer, U. Moon, B. Petryna, V. Prodanov, S. Ramprashad, G. C. Temes, and L. Toth for useful discussions and support.

References

[1] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. NY: IEEE Press, 1996.

[2] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 40, no. 8, pp. 461–466, August 1993.

[3] S. H. Ardalan and J. J. Paulos, "An analysis of nonlinear behavior in delta-sigma modulators," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 6, pp. 593–603, June 1987.

[4] W. L. Lee, "A novel higher-order interpolative modulator topology for high resolution oversampling A/D converters," Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, June 1987.

[5] T. Ritoniemi, T. Karema, and H. Tenhunen, "The design of stable high order 1-bit sigma-delta modulators," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 3267–3270.

[6] R. Schreier and Y. Yang, "Stability tests for single-bit sigma-delta modulators with second-order FIR noise transfer functions," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1992, pp. 1316–1319.

[7] S. R. Norsworthy, "Optimal nonrecursive noise shaping filters for oversampling data converters. Part 1: Theory," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1993, pp. 1353–1356.

[8] B. Zhang, M. Goodson, and R. Schreier, "Invariant sets for general second-order low-pass delta-sigma modulators with DC inputs," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1994, pp. VI.1–VI.6.

[9] L. Risbo, "On the design of tone-free sigma-delta modulators," *IEEE Trans. Circuits Syst. II*, vol. 42, no. 1, pp. 52–55, January 1995.

[10] J. A. E. P. van Engelen, R. J. van de Plassche, E. Stikvoort, and A. G. Venes, "A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1753–1764, December 1999.

[11] T. Zourntos and D. A. Johns, "Variable-structure compensation of delta-sigma modulators: Stability and performance," *IEEE Trans. Circuits Syst. I*, vol. 49, no. 1, pp. 41–53, January 2002.

[12] C. D. Thompson and S. R. Bernadas, "A digitally-corrected 20b delta-sigma modulator," in *Dig. IEEE Int. Solid-State Circuits Conf.*, February 1994, pp. 194–195.

[13] D. A. Kerth, D. B. Kasha, T. G. Mellissionos, D. S. Piasecki, and E. J. Swanson, "A 120dB linear switched-capacitor delta-sigma modulator," in *Dig. IEEE Int. Solid-State Circuits Conf.*, Febr. 1994, pp. 196–197.

[14] W. Rhee, A. Ali, and B. Song, "A 1.1GHz CMOS fractional-N frequency synthesizer with a 3b 3rd-order delta-sigma modulator," in *Dig. IEEE Int. Solid-State Circuits Conf.*, February 2000, pp. 198–199.

[15] H. G. Musmann and W. Korte, "Generalized interpolative method for digital/analog conversion of PCM signals," U.S. Patent 4,467,316, August 21, 1984.

[16] P. J. Naus, E. C. Dijkmans, E. F. Stikvoort, A. J. McKnight, D. J. Holland, and W. Bradinal, "A CMOS stereo 16-bit D/A converter for digital audio," *IEEE J. Solid-State Circuits*, vol. 22, no. 3, pp. 390–395, June 1987.

[17] S. Willingham, M. Perrott, B. Setterberg, A. Grzegorek, and B. McFarland, "An integrated 2.5GHz delta-sigma frequency synthesizer with 5μs settling and 2Mb/s closed loop modulation," in *Dig. IEEE Int. Solid-State Circuits Conf.*, February 2000, pp. 200–201.

[18] P. Kiss, J. Arias, and D. Li, "Stable high-order delta-sigma DACs," in *Proc. IEEE Int. Symp. Circuits Syst.*, 27 May 2003, pp. I.985–I.988.

[19] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, and T. Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping," *IEEE J. Solid-State Circuits*, vol. 22, no. 12, pp. 929–934, December 1987.

[20] M. H. Perrott, T. L. Tewksbury, and C. G. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2048–2060, December 1997.

[21] N. M. Filiol, T. A. D. Riley, C. Plett, and M. A. Copeland, "An agile ISM band frequency synthesizer with built-in GMSK data modulation," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 998–1008, July 1998.

[22] R. Schreier, "The delta-sigma toolbox for Matlab," Matlab code and documentation, 1997–2003, [Online]. Available: <http://www.mathworks.com/matlabcentral/fileexchange>.

[23] R. T. Baird and T. S. Fiez, "Improved delta-sigma DAC linearity using data weighted averaging," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, May 1995, pp. 13–16.

[24] O. Mencer, M. Platzner, M. Morf, and M. Flynn, "Object-oriented domain-specific compilers for programming FPGAs," *IEEE Trans. VLSI Syst.*, vol. 9, no. 1, pp. 205–210, February 2001.

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A PUBLICATION OF THE IEEE CIRCUITS AND SYSTEMS SOCIETY

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JANUARY 2004 VOLUME 51 NUMBER 1 ITCSCH (ISSN 1057-7122)

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TRANSACTIONS BRIEFS

CALLS FOR PAPERS

IEEE TRANSACTIONS ON
CIRCUITS AND SYSTEMS
I: FUNDAMENTAL THEORY AND APPLICATION

SPECIAL ISSUE

ADVANCES ON ANALOG-to-DIGITAL and DIGITAL-to-ANALOG CONVERTERS

Call for Papers

Data converters are fundamental building blocks for mixed-signal chips. During the last few years significant advances have been made on the design of embedded data converters; i.e. converters which are designed to be integrated on a semiconductor substrate together with other analog and digital circuitry. The final goal of such embedding is the realization of complete systems on chip. These advances have been linked to the proposal of new architectures which are better suited for the applications targeted by these systems on-chip; examples include the use of sigma-delta converters for wireline communications and radio, or the recent progress on successive approximation converters, just to mention a few. Some of these architectures are based on heuristic considerations, and fundamental studies are needed to fully understand their operation and hence enable their optimum design. Also, new circuit strategies have been devised to cope with the challenge of reducing the power consumption, while at the same time increasing the resolution and the frequency of operation. These strategies have to be fully compatible with modern sub-micron technologies, and capable to track the technology road-map towards deeper sub-micron. In many cases, this involves using rather hostile technologies, with poorly characterized and prone to error circuit primitives. This has prompted the proposal of clever strategies for error correction and calibration. Last but no least, the co-existence with digital circuits have challenged researchers to develop techniques and strategies to model and alleviate the problem of cross-coupling through the substrate.

This special issue aims to collect papers dealing with recent advances on data converters, covering both the theory underlying their operation and modeling, as well as all issues associated to their implementation and practical usage. Examples of topics qualifying for the special issue include the following:

- New Architectures for Data Converters
- Analysis of Errors in Data Converter Operation
- Modeling of Data Converters
- Design Methodologies for Data Converters
- Error Correction and Calibration Techniques
- Trade-Offs in Data Converter Design
- Advances on Nyquist-Rate Data Converters
- High-Speed High-Resolution Sigma-Delta
- Design of Converters on Standard, Digital CMOS
- Electrical and Physical Design for Performance
- Strategies to Deal with Substrate Coupling
- Digital Design for Embedded Data Converters

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Manuscripts should be sent electronically (pdf) to Prof. Angel Rodriguez-Vázquez by the deadline below. All manuscripts are subject to peer review and should conform to the standard formats as indicated in the “Information for Authors” of IEEE Transactions on Circuits and Systems.

Schedule:

Deadline for Reception of Manuscripts (pdf):	15 January 2003
Notification of Acceptance:	31 April 2003
Tentative publication date:	August 2003

Guest Editorial for January 2004 Special Issue

DATA CONVERTERS are fundamental building blocks for mixed-signal chips. During the last few years, significant advances have been made in the design of embedded data converters, i.e., converters which are designed to be integrated on a semiconductor substrate together with other analog and digital circuits. The final goal of such embedding is the realization of complete systems on chip. These advances have been linked to the proposal of new architectures, which are better suited for the applications targeted by these systems on-chip. Examples include the use of Sigma–Delta converters for wireline communications and radio, or the recent progress on successive approximation converters, just to mention a few. Some of these architectures are based on heuristic considerations, and fundamental studies are needed to fully understand their operation, and hence, enable their optimum design. Also, new circuit strategies have been devised to cope with the challenge of reducing the power consumption, while at the same time increasing the resolution and the frequency of operation. These strategies have to be fully compatible with modern submicron technologies, and capable of tracking the technology roadmap towards deeper submicron resolution. In many cases, this involves using rather hostile technologies, with poorly characterized and prone to error circuit primitives. This has prompted the proposal of clever strategies for error correction and calibration. Last but not the least, the coexistence with digital circuits has challenged researchers to develop techniques and strategies to model and alleviate the problem of mixed-signal coupling.

The January 2004 Special Issue aimed at collecting papers dealing with recent advances on data converters. There was an excellent response to the call for papers, with 67 submissions received. The Guest Editors would like to thank all contributing authors for their favorable response to the call, which significantly contributed to enrich the Special Issue.

The 67 manuscripts received reflected the breadth and depth of research in this area worldwide, covering topics from theory, architecture, and modeling implementation and test of analog–digital converters (ADCs) and digital–analog converters (DACs). All submissions were subjected to peer review, with five reviewers assigned per manuscript. Unfortunately, due to severe constraints on the number of pages available for the issue, only a fraction of the submitted papers could be published, and many high-quality papers had to be discarded.

The category that received the largest number of manuscripts was Sigma–Delta modulation, reflecting the ongoing analytical and design challenges in this area. From these submissions, five papers were selected. A number of the contributions deal with challenges in moving to broadband applications and deep submicron processes. Two of these (*Markus and Temes* and *Hamoui and Martin*), present architectures for low oversampling ratios, while the paper by *del Rio et al.* presents the design of a modulator for ADSL+ applications, and reviews many of the considerations involved in a design of this nature. Design considerations at the architecture level are the subject of the paper by *Bajdechi et al.*, which presents an algorithm for searching for the design space for the optimum modulator from a range of architectures. Finally, in this section, the paper by *Tille et al.*considers low-voltage MOSFET-only modulators, focusing in particular on the use of compensated depletion-mode MOSFET capacitors.

A cyclic ADC for biomedical applications is presented in the work by *Bonfini et al.*. Two further papers consider pipelined ADCs. *Wu and Liow* present new current-mode wave-pipelined architectures, while *Chiu et al.* deal with digital background calibration. Also in the category of Nyquist converters, *Pan and Abidi*, in their paper, present a theoretical overview of signal folding as a unifying concept which allows them to compare classes of converters. A new folding ADCs architecture is presented in the brief by *Genov and Cauwenberghs*.

Three papers presented in the January Special Issue (*Jamal et al.*, *Elbornsson et al.*, and *Leger et al.*) deal with time-interleaved ADCs, examining how the mismatch and sample-time errors associated with these structures can be analyzed, detected and corrected.

Calibration is the focus of the work by *Eduri and Maloberti*, which uses output code-density histograms in the calibration of Nyquist-rate ADCs, and that of *Gandolfi et al.*, which studies calibration algorithms for bandpass Sigma–Delta modulators.

DACs are also covered in four contributions: *González-Jiménez et al.* presents a design procedure for current steering DACs which accounts for mismatch and dynamic errors. The brief by *Deveugele et al.* addresses the issue of switching for the design of high-accuracy DACs. The brief by *Kiss et al.* focuses on the design of stable sigma-delta DACs. The brief by *Starzyk et al.* presents practical considerations for the design and layout of current steering DAC. From another perspective, layout considerations also constitute the topic of the brief by *Paul et al.*

Companion blocks of data-conversion systems are addressed in the paper by *Sugimoto*, and in the brief by *Rahkonen and Aikkila*. *Sugimoto* presents a sample-and-hold circuit for low-voltage environments. From a theoretical perspective, the subject of sampling is also considered by *Poberezhskiy and Poberezhskiy*, who present in their paper, a technique for combining filtering with the sampling and reconstruction process.

Digital Object Identifier 10.1109/TCSI.2004.825595

Last but not the least, the Special Issue also addresses data converter testing. The brief by *Ong et al.*presents a new architecture for testing using digital stimuli, while the brief by *Wegener and Kennedy* discusses how to test ADC nonlinearities by using linear models.

The Guest Editors would like to thank the past Editor-in-Chief of the Transactions, Prof. Tamás Roska, for his warm support to the Special Issue proposal. We are also indebted to many of the reviewers (whose names must remain anonymous) for their punctual, careful, and detailed reviews. Their many constructive suggestions have contributed to improve the overall quality of the papers published in the issue.

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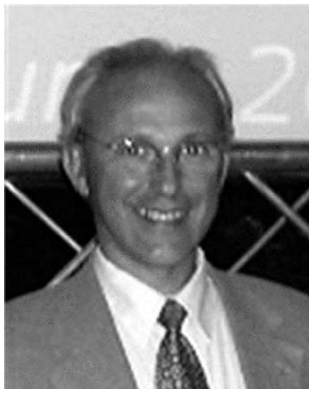

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