Explanation of DAC interface via SPI protocol

One of the task in HW-4 is interfacing external DAC (MCP4921) with a microcontroller using SPI channel. Make it sure you properly read the datasheet available here:

http://ww1.microchip.com/downloads/en/devicedoc/21897b.pdf

In the above DAC, the following four pins need to be controlled from MSP.

3.2 Chip Select ($\overline{CS}$)

$\overline{CS}$ is the chip select input, which requires an active-low signal to enable serial clock and data functions.

3.3 Serial Clock Input (SCK)

SCK is the SPI compatible serial clock input.

3.4 Serial Data Input (SDI)

SDI is the SPI compatible serial data input.

3.5 Latch DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ (the latch DAC syncronization input) transfers the input latch registers to the DAC registers (output latches) when low. Can also be tied low if transfer on the rising edge of $\overline{CS}$ is desired.

The timing of above signals must meet the following specs,

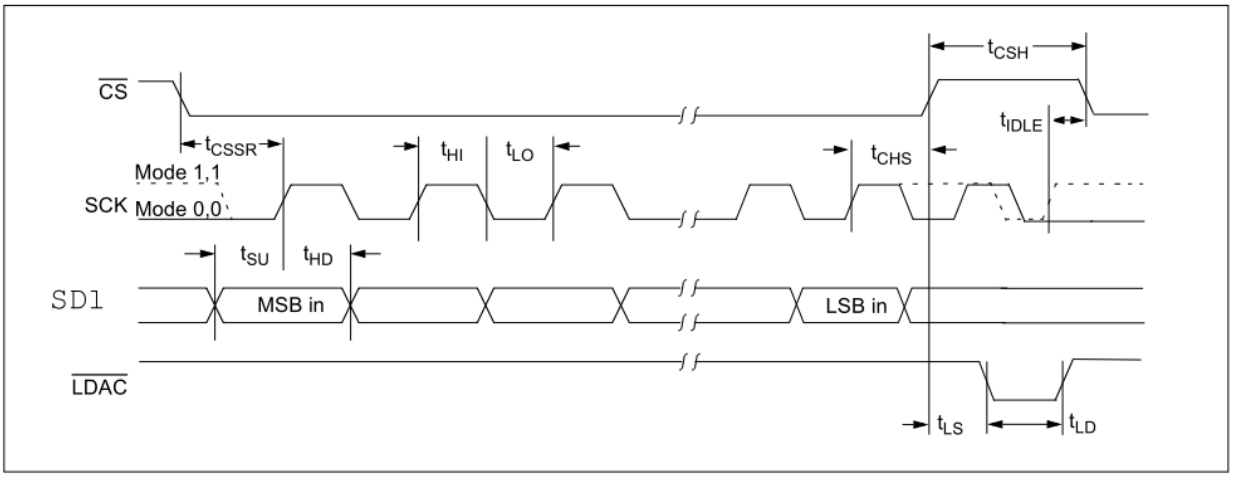

FIGURE 1-1: *SPI™ Input Timing.*

If you see above in Figure 1-1, the MSB is the first bit and LSB is the last bit to transmit. During data transmission of 12-bits, $\overline{CS}$ is low (enabled). After the transmission is done $\overline{CS}$ goes high (disabled state). During that state, $\overline{LDAC}$ is enabled for one clock cycle. Keep in mind that both $\overline{CS}$ and $\overline{LDAC}$ are active low signals.

Reference Voltage

The V_{ref} input pin of DAC must be tied to a 2.048V. This voltage can be easily created using voltage divider.

5V AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, output buffer gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values at +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**

Writing to DAC:

Here is the write command format.

REGISTER 5-1: WRITE COMMAND REGISTER

Upper Half:							
W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x
$\overline{A}$/B	BUF	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8
bit 15							bit 8

Lower Half:							
W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
D7	D6	D5	D4	D3	D2	D1	D0
bit 7							bit 0

If you observe, the lower 12 bits could be the ADC data received from the other microcontroller. The higher 4-bits are commands.

Make it sure $\overline{SHDN}$ is disabled. If it is enabled ($\overline{SHDN}$=0), then DAC output buffer will be in shut-down state.

bit 15 **$\overline{A}$/B:** DAC_A or DAC_B Select bit
1 = Write to DAC_B
0 = Write to DAC_A

bit 14 **BUF:** V_{REF} Input Buffer Control bit
1 = Buffered
0 = Unbuffered

bit 13 **$\overline{GA}$:** Output Gain Select bit
1 = 1x (V_{OUT} = V_{REF} * D/4096)
0 = 2x (V_{OUT} = 2 * V_{REF} * D/4096)

bit 12 **$\overline{SHDN}$:** Output Power Down Control bit
1 = Output Power Down Control bit
0 = Output buffer disabled, Output is high impedance

bit 11-0 **D11:D0:** DAC Data bits
12 bit number "D" which sets the output value. Contains a value between 0 and 4095.