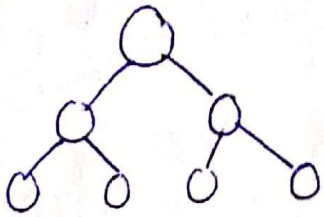
12/9/19

Tree Interconn^n n/w

→ It is static.

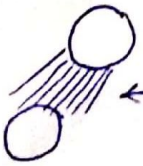


nodes - processors/ memory modules/ I/O devices.

If many nodes of left subtree wants to connect with node of right tree than root has is congested with all the messages.

To handle this complexity, root node has multiple channel to next node. ∴ if multiple nodes wants to communicate they can pass through various channels.

Fat tree.



← multiple channel.

$2 \times \log_2 \lceil \frac{n}{2} \rceil - 1 \times 1$

n	h
1	0
2	1
3	1
4	2
15	4

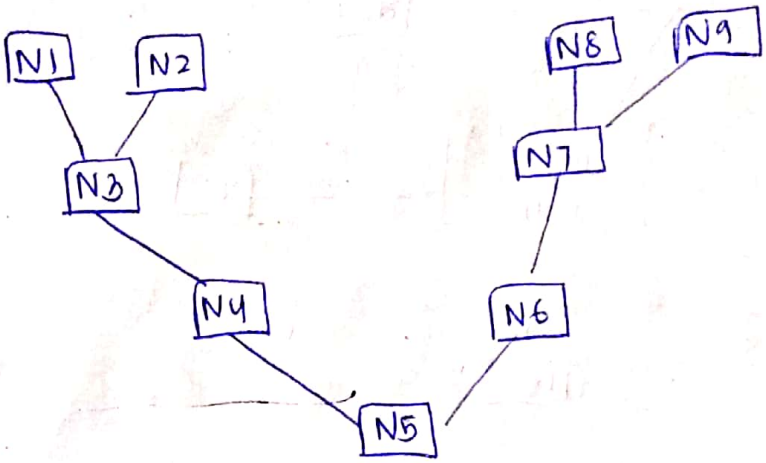
$n = 2^h - 1$

$h \lceil \log_2 n \rceil$

diameter of tree = $2h$ or $2\lceil \log_2 n \rceil$ } assuming complete binary tree.

$2^h, n+1$

$h = \log_2(n+1)$

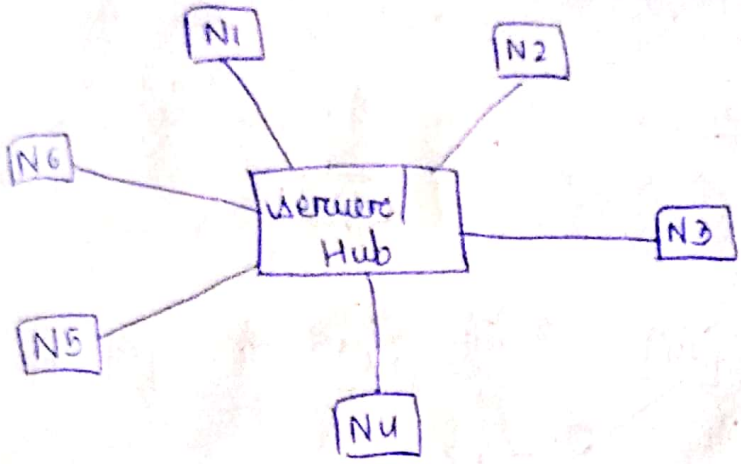


Adv:

→ existing Nlw can be easily expanded
→ It is point to point wiring for individual segments. This implies easiere installation & maintenance.
→ It is well suited for temporary nlw. (bcz insertion or removal of node is easy.)

Disadv

→ Technical expertise required to configure a wired tree topology lnlw.
→ failure of backbone cable brings down entire nlw
→ It is insecure nlw
→ Maintenance is difficult for a large nlw.



Adv:

→ Troubleshooting is easy as faulty node can be detected from the central node immediately bcz each individual node is connected to hub.

→ Failure of one node doesn't affect the n/w.

→ It is simple access protocol ~~required~~ referred as one of the comm nodes is always the central node.

Disadv

→ ~~Long~~ one cables may be require to connect each node to server.

→ Failures of central node bring down the whole n/w.

Tree N/w

It has group of star n/w connected to a linear bus backbone cable and it incorporates features of both star & bus n/w.

Tree n/w is also called hierarchical n/w.

Advantage of ring N/w

→ small cable segments are needed to connect 2 nodes
→ It is idle for optical fibre as data travels in one direction.
→ very high transmission speed is possible.

Disadv. of ring N/w

→ Failure of single node brings down whole N/w
→ Trouble shooting is difficult in as many nodes may have to be inspected before faulty one is identified.
→ Difficult to remove one or node nodes while keeping the rest of the N/w.

13/8/19

Star N/w

Here, servere is connected to each node individually & here servere is called as the central node or hub.

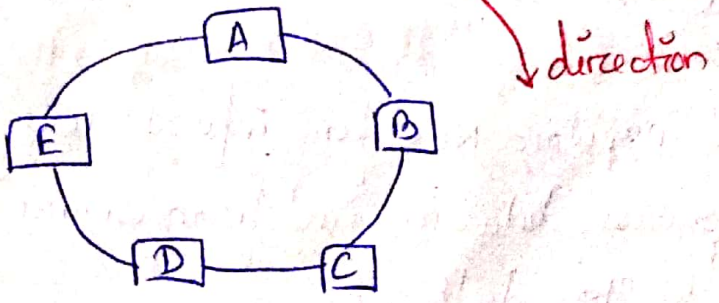
Any exchange of data b/w 2 nodes must take place through servere.

It is most popular N/w for info. & voice n/w as central node can process data received from source node before sending it to the desti. node

- In the worst case, when node 1 has to send msg to node N, the msg has to traversed to a total no. of (n-1) nodes before it can reach the destn.
- Linear arrays are simple in their architech & have simple routing mechanism & linear arrays are slow when no. of nodes, N is large.
- The Nlw complexity of linear array is O(N).
- The time " " " " O(N).
- If 2 nodes at the extreme ends of the linear array are connected, the resultant Nlw will be ring architech / topology.

Ring Nlw

Each terminal is connected to exactly two nodes & giving Nlw a circular shape.
Data travels in one direction which is predefined.



b) They doesn't provide a direct link from every node to every other node in Nlw instead of comm blw some nodes have to be routed through other nodes in the Nlw.

⇒ The length of the path blw nodes measured in terms of # links that has to be traversed is expected to be longer compared to the case of CCNS.

⇒ Here, two other conds seems to have been imposed by the existence of limited interconnectivity in LCNS and these are

a) need for a pattern of interconn among nodes.

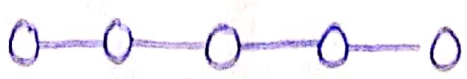
b) " " " mechanism for routing messages around the Nlw until they reach their destination.

eg of LCNS

linear array, ring Nlw, 2D-array, 3 Nlw, cube Nlw.

Linear array Nlw

- Here each node is connected to its 2 intermediate neighbouring nodes.



- Here, if each node i need to comm node j, $j > i$, then the msg from node i has to be traversed node is

$i+1, i+2, \ldots, j-i$.

A)→ Here, each nodes is connected to all other nodes in the N/w.

→ fast delivery of msgs from any source node to any desti node.

→ only one link has to be traversed.

→ every node is connected to every other node in the n/w. ∴, routing of msg b/w nodes becomes a straight forward tasks.

CCNS Characteristics

→ It is used for fast delivery of msg from any source node to any desti node.

→ only one link has to be traversed.

→ CCNS are expensive in terms of the # links needed

→ for their construc, # links in CCNS is given by formula, $\frac{N(N-1)}{2}$

→ Delay complexity of CCNS measured in terms of # links traversed.

→ As msg are routed from any source to any desti, is constants i.e. complexity is O(1).

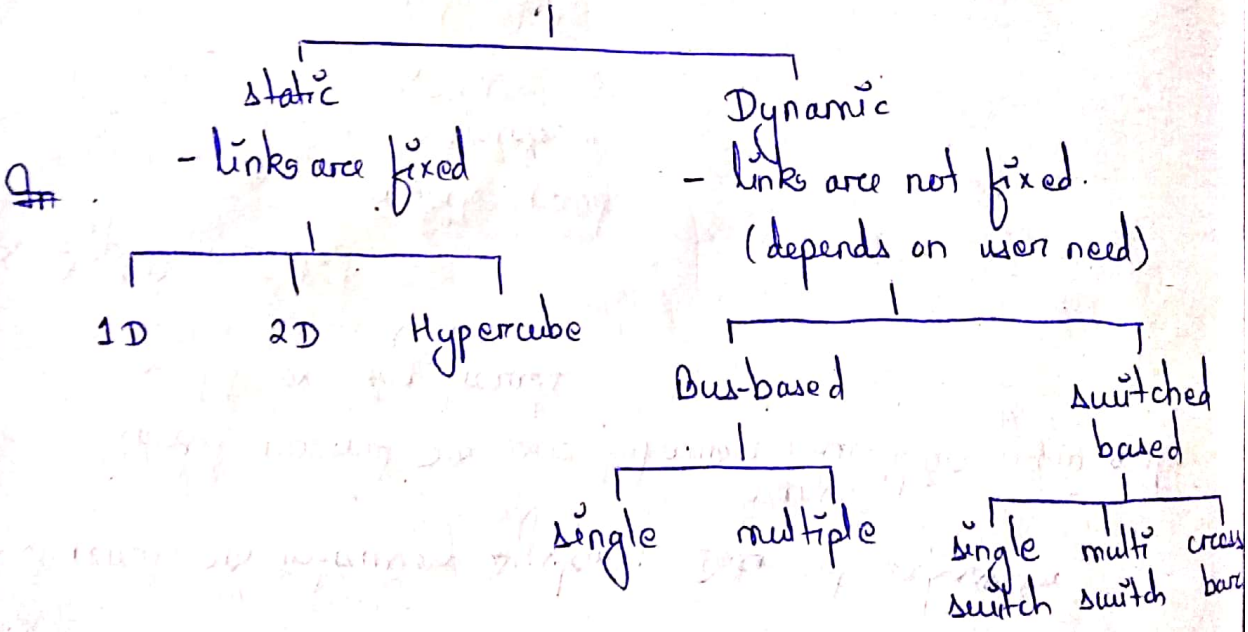
Module-2

Parallel Interconnection Network

aim - ↑ performance by ↓ comm^n latency.

Set of devices interconnected to each other - interconnection N/w.

An interconnec^n N/w in a parallel m/c transfers info from any source node to any dest^n node.



Static Interconnection N/w (SIN)

- unidirec or bidirec. b/w the processors.
- fixed path

Two types of static N/w are

a) Completely connected N/w (CCNS)
b) Limited connected N/w (LCNS)

22/8/19

Pipelining

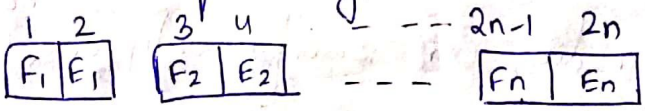
eg → assembly pipeline (various parts of cars are constructed simultaneously)
→ laundry section.

To increase throughput of a system, pipelining is used.

Let an instruction has 2 operations

Fetch (F) & execute (E) } let them take 1 CPU cycle.

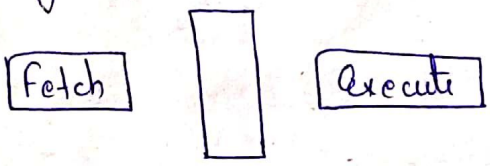
a) If we execute sequentially,



Let there are n instructions.

∴ no. of clk cycles needed = 2n.

b) In pipelining.

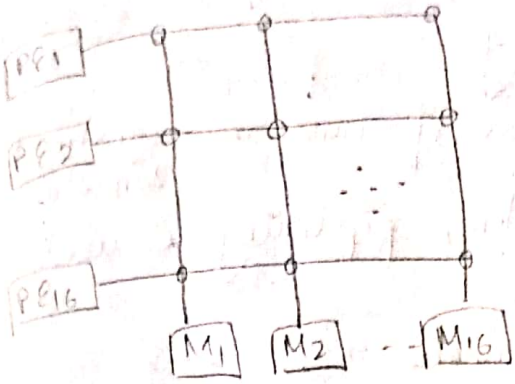


↑ interstage buffers
↓
used to synchronise b/w the 2 operations so that no conflict occurs.

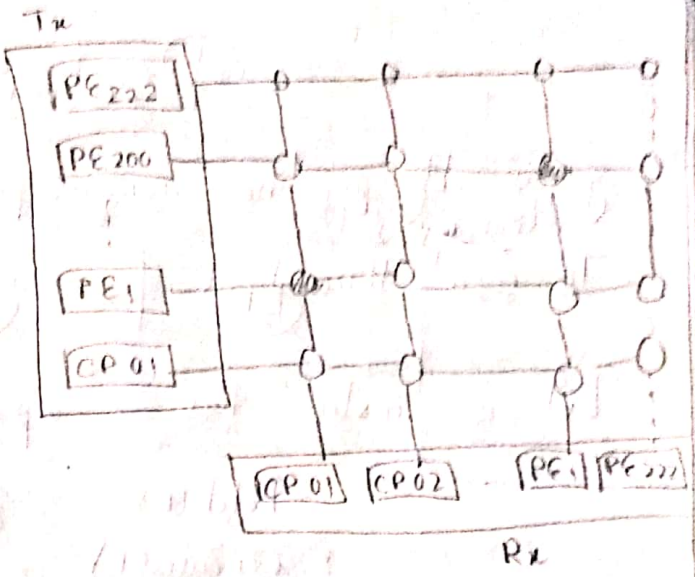
Let n = 4

	1	2	3	4	5	6	7
I_1	F_1	E_1					
I_2	-	F_2	E_2				
I_3	-	-	F_3	E_3			
I_4	-	-	-	F_4	E_4		

clk cycles needed = 5.



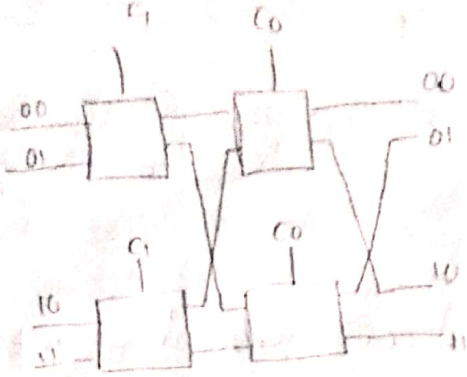
Type I



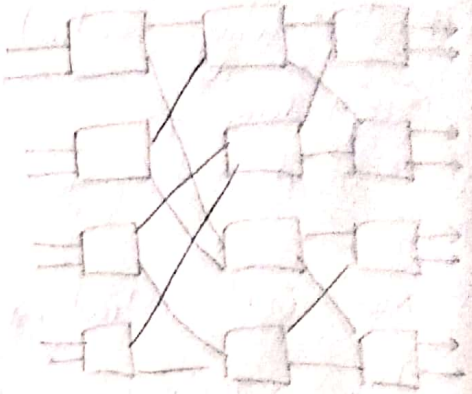
Type - II.

- Each memory module can satisfy only one PE rqst at one time
- When multiple rqst arrive at same memory module simultaneously, crossbar must resolve conflicts.

Seen
22/08/19



(4x4 Butterfly n/w)



(8x8 baseline n/w)

Baseline N/w

- blocking multistage n/w generated recursively.
- first stage contains N×N block & 2nd stage contains two $(\frac{n}{2}) \times (\frac{n}{2})$ subblocks.

Crossbar N/w

- single stage n/w which provides highest bw & highest interconn capability.
- each crossbar switch has a crosspoint switch which can provide dedicated path b/w pair.
- there are 2 types of crossbar N/w confi.

  Type-I: an interprocessor memory crossbar n/w for multiprocessors.

  Type-II: an interprocessor crossbar n/w for vector processors.

(c) 3 types of control strucc. used in nlw construction are :-

a) Partial stage Control
b) Individual " "
c) Individual box "

(a) has $(i+1)$ control signals which are used at stage-i for $0 \le i \le n-1$

(b) same control signal is used to set all switch boxes in same stage.

n control signals required to set up all n stages

(c) - separate control signal is used to set state of each switch box.

- offers more flexibility in setting up conn path.
- requires $n^2/2$ control signals which will ↑ complexity of control circuitry.

Omega Nlw

- It is nlw build using $\log_2 N$ cascaded switch boxes using shuffle connⁿ.
- Ilp label of switches of i^{th} stage is obtained by shuffle transforming olp labels of corresponding $(i-1)^{th}$ stage switch.
- this nlw was used in experimental multicomp.
- Another ~~commercial com~~ multistage Nlw used in many commercial stw comp is **butterfly nlw**.
- back-to-back butterfly nlw is called **benes nlw**.

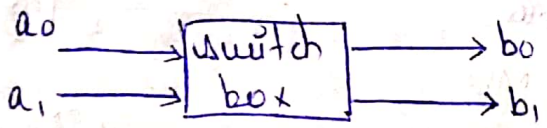
- These n/w are characterized by 3 features :-

a) switch box
b) n/w topology
c) Control structure

many switch boxes are used in MINs.

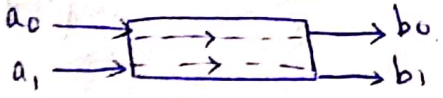
(a) Switch box :

Each box is an interchange device with 2 I/P, 2 O/P.

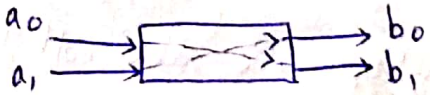


Switch box can be any 4 states.

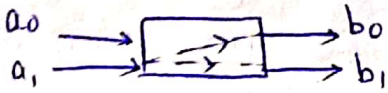
i) Straight.



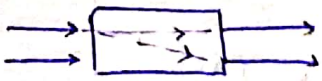
ii) Exchange



iii) Upper broadcast



iv) Lower broadcast



(b) On basis of arbitrary conn of I/P & O/P.