9.30 - 11.30

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY (VSSUT), ODISHA
Mid Semester Examination November - 2019

COURSE NAME:B.Tech SEMESTER:7th

BRANCH NAME: Computer Science and Engineering

SUBJECT NAME:Advanced Computer Architecture

FULL MARKS:**20** *TIME:**2 Hours***

Answer **All** Questions.

The figures in the right hand margin indicate Marks. *Symbols carry usual meaning.*

Q1. Answer all Questions. **[1×5]**

a) What do you mean by parallel inter-connection network? Explain about Torus and Barrel shifter network. - CO1

b) What is the difference between instruction pipeline and arithmetic pipeline? - CO1

c) Explain the Flyn's classification using suitable examples. - CO2

d) What is bisection width and diameter of a d-dimensional hypercube network. - CO2

e) What is the difference between Synchronous and Asynchronous pipelining? - CO3

Q2. **[5]**

a) Differentiate between CPI and IPC? The following Table give the frequencies of bench mark A and the number of cycle taken for different class of instruction is as follows: - CO1

Instruction type	Frequency	Cycles
Load and Store	30%	6cc
Arithmetic	50%	4cc
All other	20%	3cc

Calculate the CPI for the Benchmark A.

OR

b) What do you mean by pipeline hazard? Explain the Data, control and structural hazard with suitable example? Explain the pipeline hazard condition where data hazard may occur. - CO1

Q3. **[5]**

a) Consider a pipeline processor with the four stages: IF, ID, EX and WB. The IF, ID and WB stages takes two clock cycle to complete the operation. The number of clock cycle required depends on the instruction. The ADD and SUB instruction takes three clock cycle and the MUL instruction takes five clock cycles in EX stages. Operand forwarding is used in pipeline processor. What is the number of clock cycle required to execute the following instructions? - CO2

ADD R2,R1,R0
MUL R4,R3,R2
SUB R6, R5, R4

OR

b) Suppose Instruction execution in a processor is divided into 5 stages. *Instruction Fetch(IF), Instruction Decode (ID), Operand Fetch(OF),Execute(EX), and Write Back(WB),* These stages take **5,4,20, 10** and **3** nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of - CO2

consecutive stages with a delay of **2 ns**. Two pipelined implementations of the processor are contemplated:

(i) a naïve pipeline implementation (NP) with 5 stages and
(ii) an efficient pipeline (EP) where the OF stage id divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.
Find out the following

1. Execution time in NP for 100 instructions.
2. Execution Time in EP for 100 instruction
3. Efficiency of the EP
4. The speedup achieved by EP over NP in executing 100 independent instructions with no hazards is

Q4. **[5]**

a) Write short notes on the following: - CO3
   1. Perfect Shuffle exchange
   2. Chordal Ring

OR

b) What is Multi-stage interconnected network? Explain the types of multi stage interconnection network. Design the topology for a Omega network. - CO3