Graphically Transforming Mueller–Schulz Percolation Criteria to Random Telegraph Signal Magnitudes in Scaled FETs

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***Abstract*— We propose a novel graphic method to enable the analysis of the field-effect transistor (FET) threshold voltage variation ΔV_{th} due to random telegraph signals in a percolative channel. First, through technology computer-aided design simulation with no percolation, both a minimum ΔV_{th} and a critical curve in a $m_{\mathrm{loc}} - \sigma_{\mathrm{loc}}$ plot are produced. The former constitutes a statistical distribution far away from the conventional log-normal one. In the latter, m_{loc} and σ_{loc} are the mean and the standard deviation, respectively, of a well-known normal variable in Mueller–Schulz's percolation theory. The critical $m_{\mathrm{loc}} - \sigma_{\mathrm{loc}}$ curve divides the plot into the allowed region and the forbidden region and will go down with increasing gate size. Then, ΔV_{th} contours in the allowed region are graphically created. While applying to existing experimental ΔV_{th} statistical distributions of SiON- and high-k metal gate (HKMG)-scaled FETs, resulting paired m_{loc} and σ_{loc} at high ΔV_{th} remain intact, regardless of gate size or gate stack type. This means that the underlying percolation patterns resemble each other, due to the same manufacturing process used. However, if these paired m_{loc} and σ_{loc} fall in the forbidden region, it is the critical $m_{\mathrm{loc}} - \sigma_{\mathrm{loc}}$ curve dominating. Application to bias and temperature instability statistical data in literature is straightforwardly well done.**

***Index Terms*— Bias and temperature instability (BTI), field-effect transistors (FETs), fluctuations, percolation, random telegraph signals (RTSs), technology computer-aided design (TCAD), trap.**

I. Introduction

RANDOM telegraph signal (RTS) magnitudes (i.e., RTS induced threshold voltage variation ΔV_{th} or equivalently the current change between levels $\Delta I/I$) have currently been widely recognized to be a big issue, especially for scaled FETs in the presence of the percolation in the channel [1]–[8]. To effectively treat the issue, one may favor the use of a percolation theory by Mueller and Schulz [9]. The core of the theory lies in the local current I_{loc} around the RTS responsible trap divided by the total current I, which can have a relation with $\Delta I/I$ [9]:

$$\frac{\Delta I}{I} = (\frac{I_{loc}}{I})^2 \tag{1}$$

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The ratio I_{loc}/I had experimentally exhibited a normal distribution [9]. Thus, the theory can be featured by two criteria, namely, the mean m_{loc} and standard deviation σ_{loc} of the distribution. To put forward the practical application of the theory, recently, we conducted a percolation-free TCAD simulation, leading to a lower limit $(I_{loc}/I)_{(\min)}$ and a critical curve in a plot of m_{loc} versus σ_{loc} [10]. The critical $m_{loc} - \sigma_{loc}$ curve divides the region into two distinct ones, allowed and forbidden. As a consequence, two distribution functions $g(\Delta I/I)$ and $f(\Delta V_{th})$ can be calculated [10]:

$$g(\frac{\Delta I}{I}) = \frac{n_0(\frac{I_{loc}}{I})}{\int\limits_{(I_{loc}/I)_{\min}}^{(I_{loc}/I)_{\max}} n_0(\frac{I_{loc}}{I}) d\frac{I_{loc}}{I}} \frac{1}{2\sqrt{\frac{\Delta I}{I}}} \tag{2}$$

$$f(\Delta V_{th}) = g(\frac{\Delta I}{I}) \frac{\ln 10}{SS} \exp(-\frac{\Delta V_{th}}{SS} \ln 10) \tag{3}$$

These two equations, as well as their upper and lower limits, can be transformed to each other via the relationship: $\Delta V_{th} = -(SS/\ln 10)\ln(1 - \Delta I/I)$ [11]. Here, SS is the subthreshold swing, valid for the subthreshold and transition region of operation [11]; and $n_0(I_{loc}/I)$ is the *standard* (unlimited) normal distribution function with the mean m_{loc} and standard deviation σ_{loc} in the allowed region. With $(I_{loc}/I)_{(\max)}$ and $(I_{loc}/I)_{(\min)}$ separately approaching infinite and zero, (2) exactly reduces to that of Mueller and Schulz [9].

In this letter, we propose a new graphic method dedicated to the allowed region where (2) and (3) hold. This method can serve as a useful tool to analyze both RTS and BTI statistical data. We will show the ability of the method to experimentally probe both the process induced percolation and the BTI induced multiple traps. In addition, we will point out that a non-zero $(I_{loc}/I)_{(\min)}$ constitutes a *new* statistical distribution, which differs from the conventional log-normal one [2]–[4].

II. Criteria and ΔV_{th} Contours

We conducted the same percolation-free TCAD simulation task [10] with the same gate oxide thickness of 2 nm. The trap is located at the SiO_2/Si interface, unless otherwise stated. Resulting distributions of $\Delta I/I$ are headed distributions and their interceptions with those calculated using (2) can determine the critical $m_{loc} - \sigma_{loc}$ curves, as schematically explained in Fig. 1(a). We found that increasing gate size will produce a shift of the headed distribution toward lower $\Delta I/I$ and higher probability. This gives rise to both the decreased

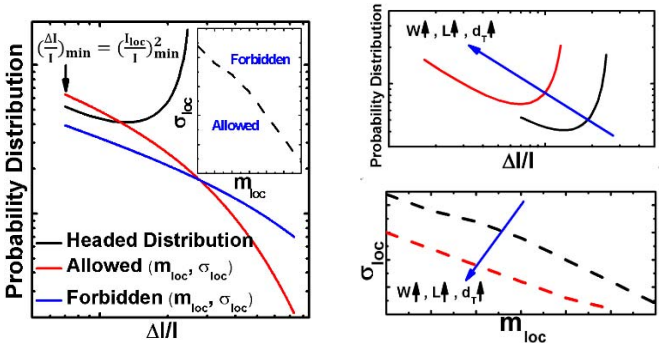

Fig. 1. (a) Schematic demonstration of how to create a minimum I_{loc}/I and a critical $m_{loc} - \sigma_{loc}$ curve from a TCAD simulated headed distribution of $\Delta I/I$. Only sets of m_{loc} and σ_{loc} in allowed region can have crossover with headed distribution. (b) Schematic demonstration of the effects of increasing gate width W, gate length L, and trap depth d_T in oxide on the resulting headed distribution and critical curve.

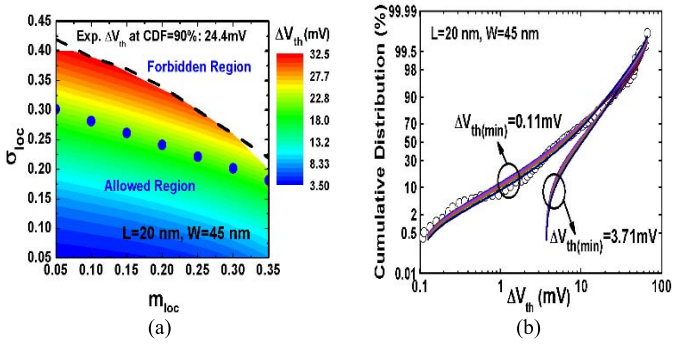

Fig. 2. (a) Created ΔV_{th} contours for W/L = 45 nm/20 nm. Gate oxide thickness = 2 nm. Simulated SS = 122 mV/dec, $\Delta I/I_{(\min)}$ = 0.068, $I_{loc}/I_{(\min)}$ = 0.260, and $\Delta V_{th(\min)}$ = 3.71 mV. The $I_{loc}/I_{(\max)}$ is transformed from the experimental ΔV_{th} maximum and the $I_{loc}/I_{(\min)}$ stems from the percolation-free TCAD simulation. (b) Calculated distributions (lines) from blue dots in Fig. 2(a) with $\Delta V_{th(\min)}$ = 3.71 and 0.11 mV. Also shown is the experimental distribution (open circles) for comparison [5].

$(I_{loc}/I)_{\min}$ and the allowed region narrowing, as schematically shown in Fig. 1(b).

To create ΔV_{th} contours in the region of interest, one may first calculate the cumulative distribution function (CDF) of ΔV_{th} by means of (3) for a set of m_{loc} and σ_{loc}. The experimental ΔV_{th} maximum was adopted for the upper limit $\Delta V_{th(\max)}$. Then, the work was repeated until all m_{loc} and σ_{loc} in the allowed region have been counted. This leads to the contours of ΔV_{th}, as depicted in Fig. 2(a). These contours were obtained at a certain CDF as high as 90%, which lies in the upper tail and is determined from the reliability point of view [2]. We found that changing this specific CDF does not change the conclusion in this letter, as long as the changed CDF (that of $\Delta V_{th(\max)}$, for instance) is situated in the high ΔV_{th} region. Created contours are apparently parallel to each other. This makes the subsequent work easy.

III. Experimental Application and Discussion

Experimental ΔV_{th} statistical distributions of SiON gate stack FETs [5], whose EOT is comparable to our TCAD

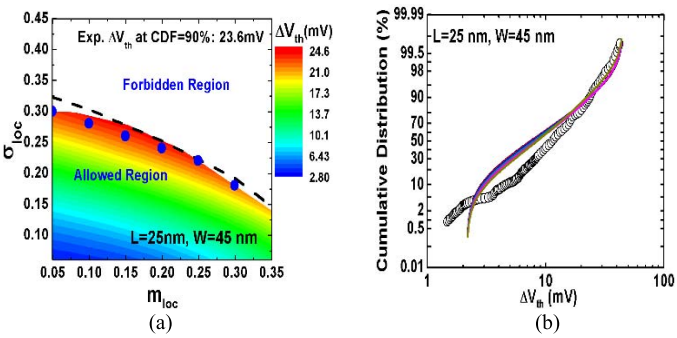

Fig. 3. (a) Created ΔV_{th} contours for W/L = 45nm/25nm. HKMG EOT = 1.16nm. Simulated SS = 137 mV/dec, $\Delta I/I_{(\min)}$ = 0.035, $I_{loc}/I_{(\min)}$ = 0.187, and $\Delta V_{th(\min)}$ = 2.11 mV. (b) Comparison with the experimental distribution [6].

structure, are quoted as shown in Fig. 2(b). Experimental ΔV_{th} at CDF = 90% is labeled in Fig. 2(a). Then, from the contour having the same experimental ΔV_{th} at that CDF, we extract paired m_{loc} and σ_{loc}, as highlighted (blue dots) in the same contour in Fig. 2(a). We found that the calculated CDF with these extracted m_{loc} and σ_{loc} as input parameters can reasonably reproduce the experimental distribution in the high ΔV_{th} region, achieved without adjusting any parameters. Note that the calculated distribution does not appear to be a log-normal one [2]–[4]. A huge discrepancy appears in the low ΔV_{th} region. This can be attributed to the effect of the bulk trap, not the interface trap. We found, through extra TCAD simulation, that increasing the depth of the trap in oxide can move the headed distribution toward lower ΔV_{th}, as schematically displayed in Fig. 1(b). Indeed, simulated lower limit $(\Delta V_{th})_{(\min)}$ was found to be in close proximity of experimental one (0.11 mV). As a consequence of changing $\Delta V_{th(\min)}$ to 0.11 mV, the reproduction quality is substantially improved over ΔV_{th} as shown in Fig. 2(b), with the other parameters kept unchanged.

Next, we cite from the same team the experimental ΔV_{th} statistical distributions of HKMG FETs [6]. To make the application as practical as possible, we modified the TCAD structure by changing the gate stack parameters to those as follows: Thicknesses of high-k and interfacial layer (IL) = 2.71 and 0.677 nm and their dielectric constants = 22 and 3.9, respectively. Resulting EOT of 1.16 nm is reasonable compared to that of the citation [6]. Simulated critical $m_{loc} - \sigma_{loc}$ curves are shown in Fig. 3(a) and 4(a) for two W/L ratios. Also shown are ΔV_{th} contours with the experimental values of ΔV_{th} at CDF = 90%. Paired m_{loc} and σ_{loc} extracted for W/L = 45 nm/25 nm differ from those of W/L = 90 nm/45 nm. Surprisingly, they can produce fairly good agreements, as in Fig. 3(b) and 4(b).

These experimentally determined paired m_{loc} and σ_{loc} remain intact, regardless of gate length, gate width, or gate stack type. The only exception is the maximum gate area case (W/L = 90 nm/45 nm for HKMG stack). This can be reasonably explained. First, we found that paired m_{loc} and σ_{loc} extracted (not shown here) for other W/L in Ref. [5] are comparable with those demonstrated above. This means that the underlying percolation patterns resemble each other,

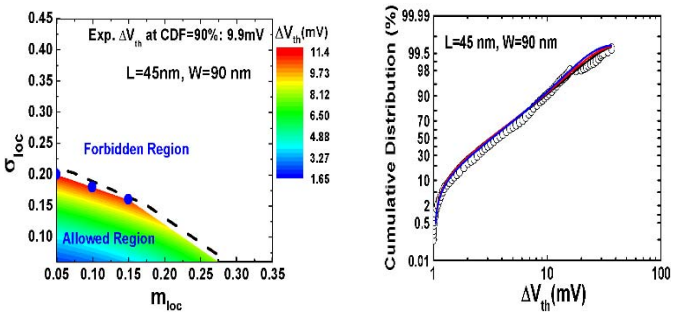

Fig. 4. (a) Created ΔV_{th} contours for W/L = 90 nm/45 nm. HKMG EOT = 1.16nm. Simulated SS = 112 mV/dec, $\Delta I/I_{(\min)} = 0.021$, $I_{loc}/I_{(\min)} = 0.145$, and $\Delta V_{th(\min)} = 1.03$ mV. (b) Comparison with the experimental distribution [6].

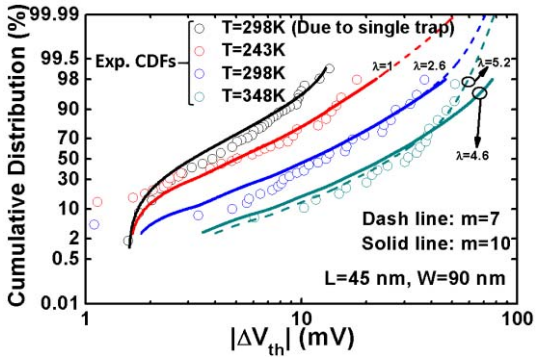

Fig. 5. Comparisons with experimental pFET ΔV_{th} distributions (open circles) under BTI conditions [12]. W/L = 90 nm/45 nm and HKMG EOT = 1.12 nm as drawn from [12]. The black solid line is from (3) with a single trap. Other lines are from (4) for $m = 7$ and 10. It can be seen that the expected trap number λ increases with the stressing. $\sigma_{loc} = 0.22$ and $m_{loc} = 0.05$ are used for all lines. Simulated SS = 87 mV/dec, $\Delta I/I_{(\min)} = 0.042$, $I_{loc}/I_{(\min)} = 0.205$, and $\Delta V_{th(\min)} = 1.62$ mV.

due to the same manufacturing process used [5]. Second, HKMG paired m_{loc} and σ_{loc} for W/L = 45 nm/25 nm are close to those of SiON, indicating that the HKMG formation [6] did not affect the underlying percolation patterns too much. Finally, in the largest area condition (W/L = 90 nm/45 nm), the same paired m_{loc} and σ_{loc} will fall into the forbidden region and hence cannot be actually detected. The plausible origin is the effect of large gate size, which will make the critical $m_{loc} - \sigma_{loc}$ curve go down and hence reduce the paired m_{loc} and σ_{loc} while narrowing the allowed region. As a consequence, paired m_{loc} and σ_{loc} situated on or close to the critical curve dominate, as clearly evidenced in Fig. 4(a). *In this situation, the percolation effect is significantly suppressed.*

To fit bias and temperature instability (BTI) statistical ΔV_{th} data [12] as shown in Fig. 5, we made use of the RTS amplitude model [13], with some slight modifications:

$$l(\Delta V_{th}) = \sum_{N=1}^{N=m} \alpha_N f_N(\Delta V_{th}) \tag{4}$$

$$f_N(\Delta V_{th}) = \int_{\Delta V_{th}(\min)}^{\Delta V_{th}(\max)} f_{N-1}(\Delta V_{th} - t) f_1(t) dt \tag{5}$$

$$\alpha_N = P_\lambda(N) / \left(\sum_{j=1}^{j=m} P_\lambda(j)\right) \tag{6}$$

where $l(\Delta V_{th})$ is the total probability distribution, m is the maximum number of traps per device, α_N is the normalized coefficient associated with Poisson distribution, $f_N(\Delta V_{th})$ is the probability distribution of ΔV_{th} due to N traps, and $P_\lambda(N)$ is the Poisson distribution with the expectation value λ. Eq.(5) reduces to (3) for $N = 1$. Good fitting is straightforwardly achieved, as depicted in Fig. 5 for $m = 7$ and 10. The sum of $P_{5.2}(N)$ and $P_{4.6}(N)$ at 348 K for $N = 1$ to m is 84.4% and 99.2%, respectively. Evidently, the larger the m value, the better the practical application.

IV. Conclusion

Experimental application of the proposed graphic method has been demonstrated. Both the process induced percolation and the stress induced multiple traps have been witnessed. The absence of the conventional log-normal distribution has been demonstrated due to non-zero $(\Delta V_{th})_{\min}$. Therefore, the graphic method is a useful tool to analyze RTS and BTI statistical data and even predict their impacts on the next-generation devices.

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