# Lesson 2

## Digital Electronics Review Part 2

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# Sequential Logic

- When we think about Sequential Logic (SL), we should first consider that the output of Sequential logic are depends on both current and previous input state values.

- Where previous input contains smaller amount of information known as the State of the system.

- For the digital sequential, state is a set of bits also known as State Variables.

- Let's try to learn about simple sequential circuits which store one bit of state such as Latches and Flip-flops.

- If we simplify SL than we found combinational logic and also banks of flip-flops containing the state of the circuit.
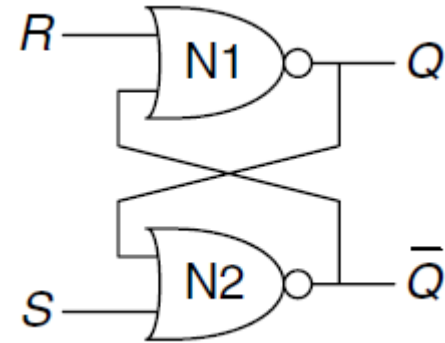
# Latch

- Latch is a bi-stable storage element where pair of inverter connected in a loop.

- Here, bi-stable means two stable states in the circuit.

- In the figure we shows the inverters are cross coupled that means output of one inverter is connected to other inverter input.

- For Q=0 I2 receives 0, so it produces 1 at Q(bar), on the other hand I1 receives 1 from Q(bar) and it produces 0 on Q. So this is stable.

- For Q=1 I2 receives 1, so it produces 0 at Q(bar) and vice-versa on Q.
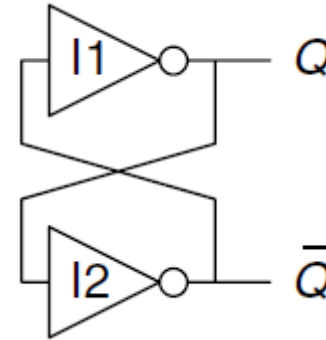
# SR-latch

- An example of S-R latch composed of two NOR gate is given below.

- The operation of this circuit can be cleared by the truth table.

| Case | $S$ | $R$ | $Q$ | $\bar{Q}$ |
|------|-----|-----|-----|-----|
| IV | 0 | 0 | $Q_{prev}$ | $\bar{Q}_{prev}$ |
| I | 0 | 1 | 0 | 1 |
| II | 1 | 0 | 1 | 0 |
| III | 1 | 1 | 0 | 0 |

# D-Latch

- In order to solving the strength behaves of simultaneous asserting in the set S and reset R of the SR latch we introduce D Latch where asserting of one of inputs determines what state and when would be changed.

- However, D latch contains two inputs one data input D that controls what would be the next state and other input is clock that controls when the state would be changed.

- If we analysis the truth table of the D latch we found that when CLK = 0 and data is any input 0 or 1 (D = X) then both S and R are 0. However, when CLK = 1 then at least one AND gate will produce output 1 and other AND gate will produce 0 depending on the input of data input D.
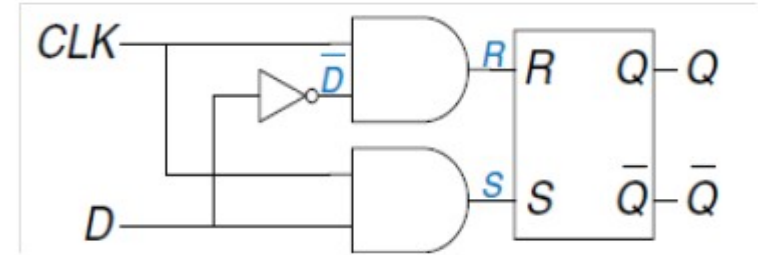


| CLK | D | $\bar{D}$ | S | R | Q | $\bar{Q}$ |
|-----|---|-----------|---|---|---|-----------|
| 0 | X | $\bar{X}$ | 0 | 0 | $Q_{prev}$ | $\bar{Q}_{prev}$ |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |

# Flip-Flop

- A flip-flop is a bi-stable element with a clock input where a state of the flip-flop changes with respect to a clock edge for example clock rises from 0 to 1.

- Flip-flop also is known as the edges-triggers flip-flop or positive edges-triggers flip-flop or master-slave flip-flop that having two states and a feedback path that allows it to store a bit of information.

- However, bi-stable elements without an edge-triggered clock known as latches.

- The difference between a latch and a flip-flop is that a latch is asynchronous, and the outputs can change as soon as the inputs do.

- A flip-flop, on the other hand, is edge-triggered and only changes state when a control signal goes from high to low or low to high.

- This triggering function is done by a clock(Clk)/enabler(E).
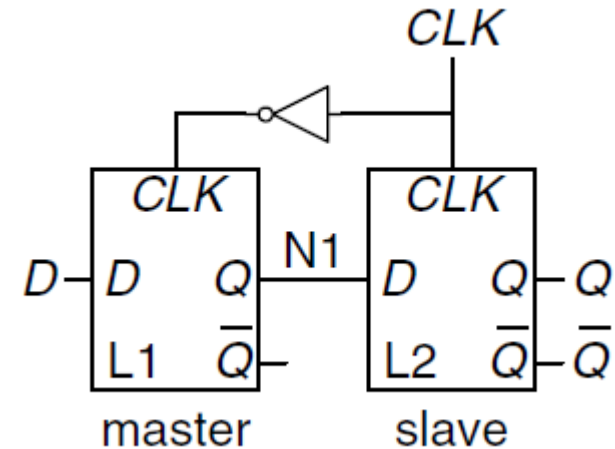
# S-R Flip Flop

- The diagram is shown below.

- Depending on the state of Clock/Enabler there are eight possible combination in the input is possible.

- The following truth table is for the above s-r flip flop.
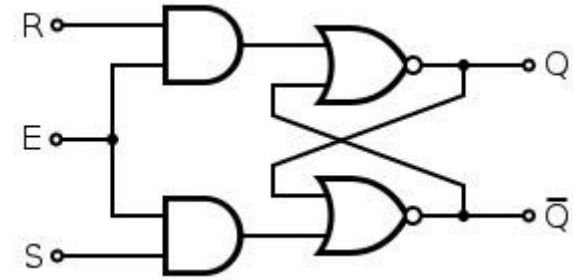


| E or Clk | S | R | Q | Q' |
|----------|---|---|---------|---------|
| 0 | 0 | 0 | Latch | |
| 0 | 0 | 1 | Latch | |
| 0 | 1 | 0 | Latch | |
| 0 | 1 | 1 | Latch | |
| 1 | 0 | 0 | Latch | |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | Not allowed | |

# D Flip-Flop

- A D-flip flop is built from two back to back D latches controlled by complementary clocks.

- The first latch L1 is called the Master & the second one L2 is called the Slave.

- The node between the latches is named as N1 as the below figure.

- A D flip-flop copies D to Q on the rising edge of the clock, and remembers its state at all other times.

- The D input specifies what the new state will be.

- The clock edge indicates when the state should be updated.

# Latch vs Flip Flop

- Latch is bi-stable memory elements to store one bit data. It is also asynchronous and transparent because when the clock is high the input is directly follow to the output.

- We are preface latch to circuit design due to shorter path delay for longer combinational path.

- However, one of the major disadvantage of latch design it complexity analysis.

- Flip-flop is a synchronous bi-stable memory elements that consist of pair of latches (master and slave) where output is edges-triggered and changed with respect to a clock edge such as when the clock rises from 0 to 1.

- Flip-flop circuit analysis is comparatively easy and robust.

- Moreover, flip-flop circuit design timing are checked using static timing analysis (STA) tools.

- However, flip-flop consume more power and required much space compare to latch.

- Latches are very similar to flip-flops, but are not synchronous devices, and do not operate on clock edges as flip-flops do.
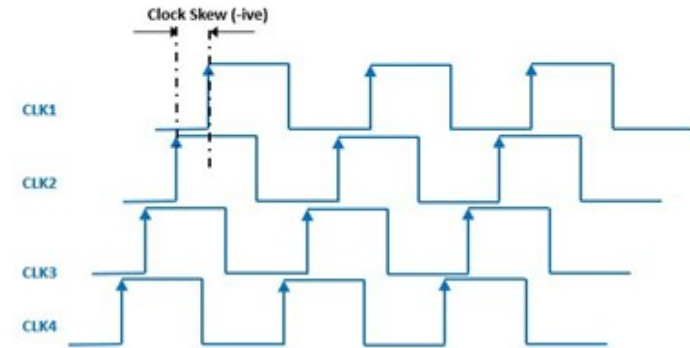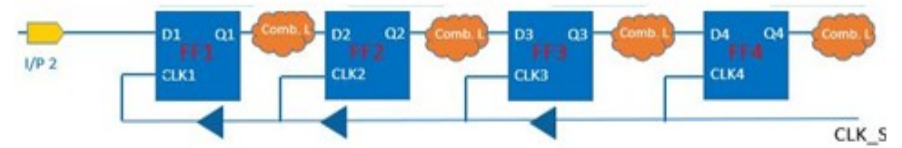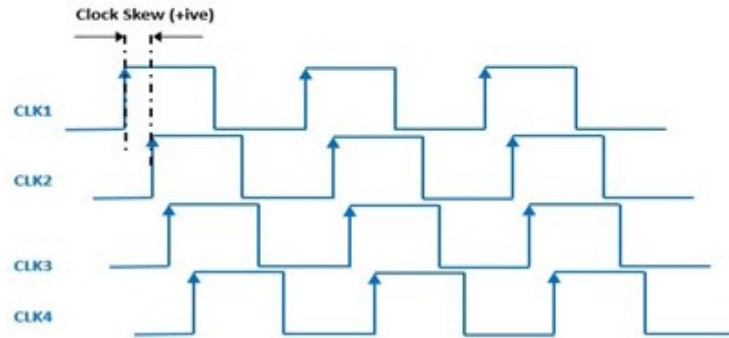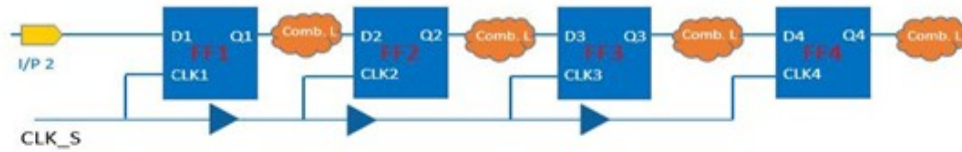
# Clock

- In electronics and especially synchronous digital circuits, a clock signal is a particular type of signal that oscillates between a high and a low state and is utilized like a metronome to coordinate actions of digital circuits.

- A clock signal is produced by a clock generator.

- Although more complex arrangements are used, the most common clock signal is in the form of a square wave with a 50% duty cycle, usually with a fixed, constant frequency.

- Circuits using the clock signal for synchronization may become active at either the rising edge, falling edge.

# Clock Skew

- In the synchronous circuit the difference between the arrival time of two sequentially registers known as Clock skew.

- If the destination register is closer to clock generation circuitry then the clock will arrived at the destination register before source register occurring a leading or positive clock skew.

- However, if the destination register arrived the edge of the clock after the source register resulting negative or lagging clock skew.

# Clock Skew

# Setup Time and Hold Time

- Setup time is the interval where synchronous input must be show and be stable before the capturing edge of the clock.

- In addition, this is the amount of time data will be stored successfully in the storage device.

- Hold time is the interval where synchronous input must be show and be stable after the capturing edge of the clock therefore the data can be store successfully in the storage device.
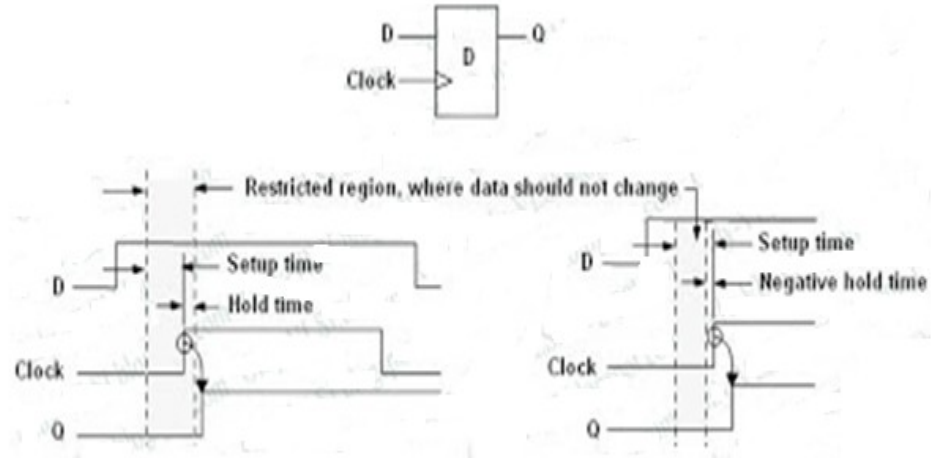
# Metastability

- When the setup and hold time violation occurs in the flip-flop then it enters a state where the its output is unpredictable known as metastable state.

- This whole process called metastability.
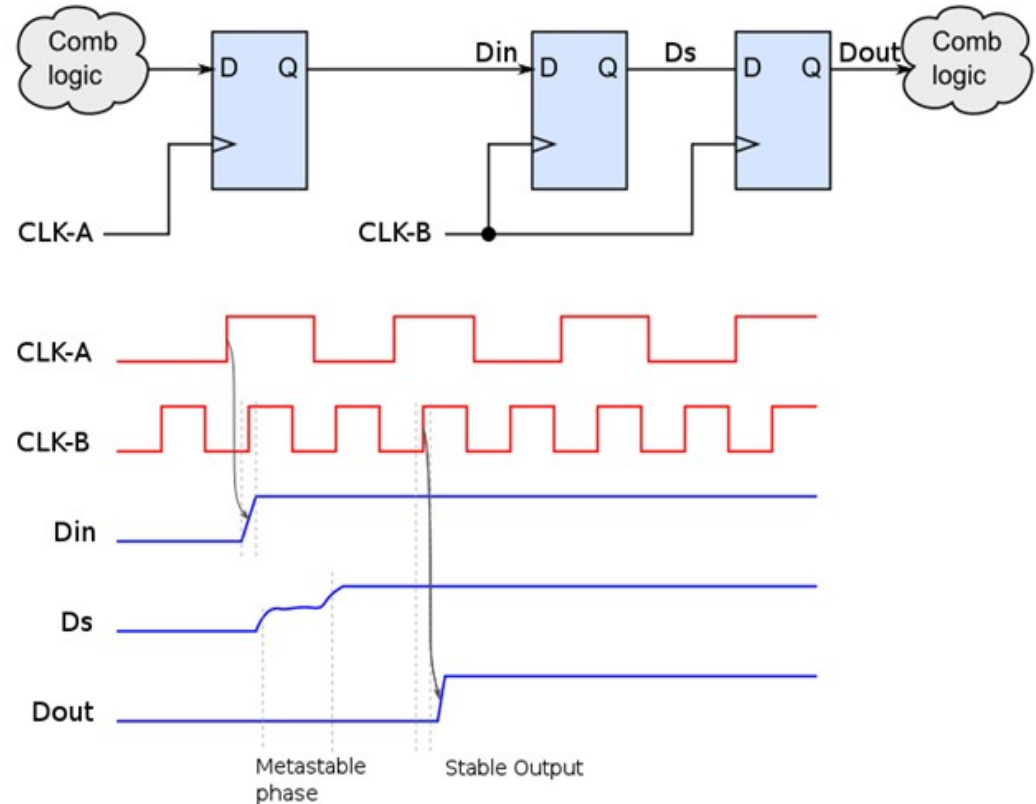
# Synchronous vs Asynchronous Circuit

- These are the class of sequential circuits which are governed by a global clock signal generated by an oscillator.

- The state of all elements of a synchronous circuit changes only by an application of a distributed clock signal.

- So, this makes the state of a synchronous circuit predictable.

- Also, synchronous clock signals are less susceptible to noise, circuit anomalies and hence safer to design and operate.

- But they are limited in operation of speed by the propagation delay of the clock signal in reaching all the elements of the clock signal.

- The time period of a clock signal should be long enough to accommodate longest propagation delay.

# Synchronous vs Asynchronous Circuit

- Practically all the circuits today are synchronous circuits, except the part where speed of the circuit operation is crucial.

- Asyncronous circuits change state only through the inputs received by them.

- So, the operation is quite instantaneous since they don't have to wait for a clock pulse.

- They are limited by propagation delay of logic gates only.

- But asynchronous circuits can transition into a wrong state due to incorrect arrival time of 2 inputs.

- This is called a race condition.

- Asynchronous circuits are quite difficult to design for a reliable operation.

# Register

- Register is also a sequential device which can hold larger quantities of data than individual flip flop.

- These are commonly used as temporary storage in a processor.

- They are faster than main memory.

- An N bit register is a bank of N flip-flop that share a common Clk input, so that all bits of the register are updated at the same time.

CLK

$D_3$ — D    Q — $Q_3$

$D_2$ — D    Q — $Q_2$

$D_1$ — D    Q — $Q_1$

$D_0$ — D    Q — $Q_0$
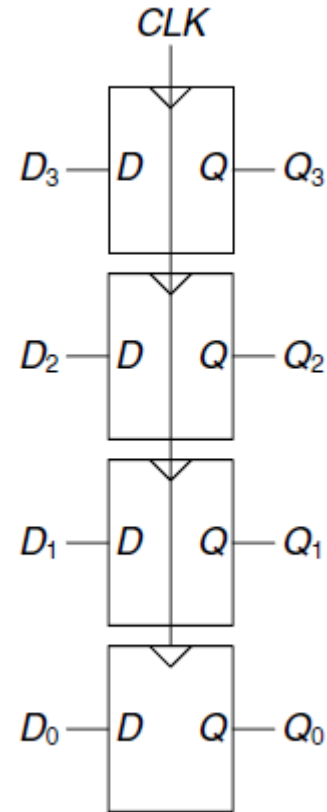
# Counter

- A device which store the number of times of a particular process with respect to clock signal called counter.

- For example, in Up counter is a counter that count the rising edges of the clock signal.

- However, N-bit binary counter consist of clock and reset input and N-bit output.

- After reset means initializes the output 0 the counter advance 2^N possible output by incrementing the rising edge of the clock.

- In the figure we see the N-bit counter composed of an adder and a resettable register.

- For every cycle the counter adds 1 to the value stored in the register.
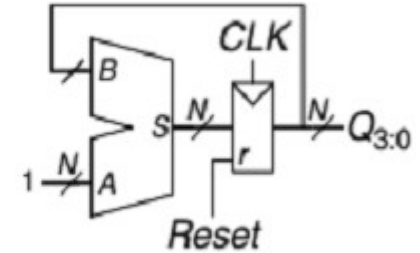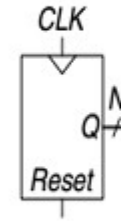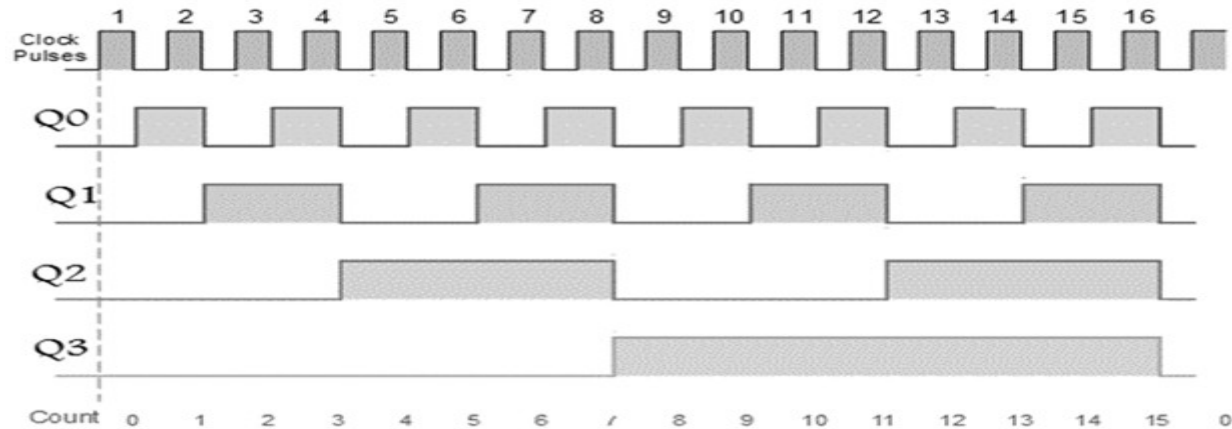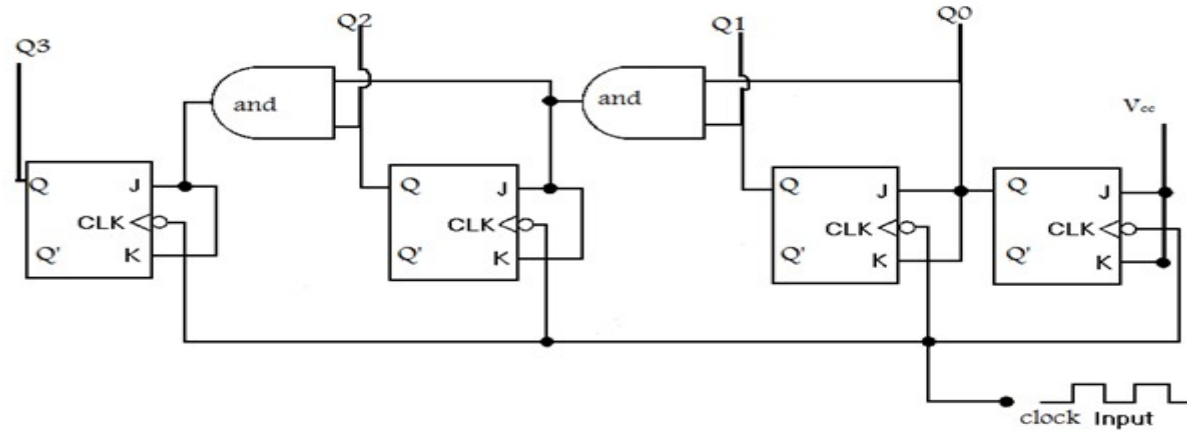
# Asynchronous Couter
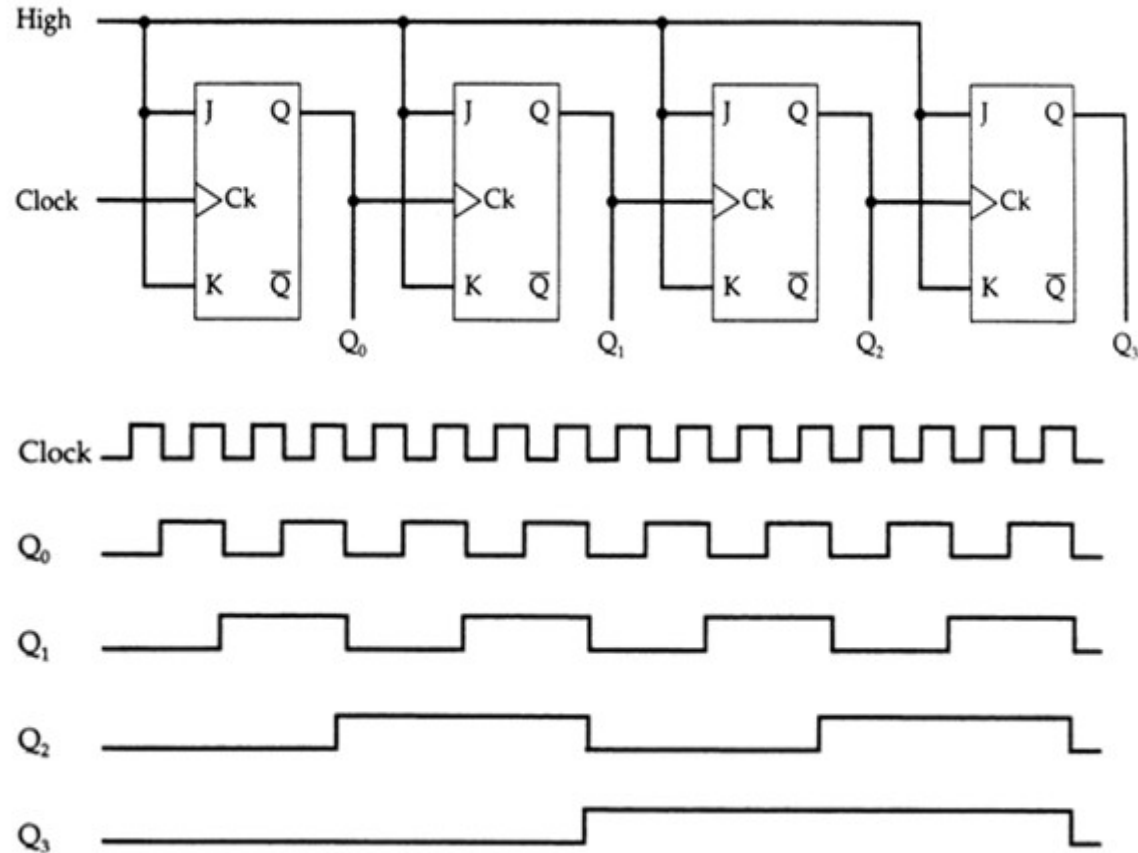
# Asynchronous Counter

- In the timing diagram of asynchronous counter illustrates that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered because Q0 is like clock pulse for second flip flop and so on.

- In this way ripples are generated through Q0,Q1,Q2,Q3 hence it is also called RIPPLE counter.

# Synchronous Counter

# Synchronous Counter

- In the synchronous counter has one global clock that drives each flip-flop so output changes in parallel.

- The advantage is it does not have cumulative delay because of same clock for each flip-flop.

- From circuit diagram, we see that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0, Q3 is dependent on Q2, Q1 and Q0.