Lesson 9

Structural, Behavioral and RTL

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Structural, Behavioral and RTL

- To put it simply, Behavioral VHDL code just shows you the behavior how the desired circuit might work.

- In other words, it mimics the behavior of how the actual circuit might work.

- So you cant synthesize a behavioral block.

- The behavioral block might be used to represent an analog block, a place holder code (when RTL is not ready of that part) and testbench code.

- For example, the following code,

Example

```
always begin

  if (!clk_en && clk==1'b1) begin

    wait (clk_en);

  end

  #5 clk = ~clk;

end
```

Behavioral Modelling

- Behavioral VHDL codes give the timings directly, such as, #5 clk = ~clk; or alarm_siren <= '1' after 5ns; directly where the periods of the clock pulses are given in the code itself.

- These type of behavior are very important for testing a synthesizable VHDL block.

- Thats why we will see this type of codes in the testbench.

RTL Modeling

- We have already seen RTL modeling in lesson 4. It is called the register transfer level.

- The term "RTL" is doenst only represent the abstraction level here, it also represents a synthesizable code unlike the Behavioral modeling.

- In short,

- We design our digital circuit with RTL VHDL and test it with Behavioral VHDL.

Structural Modeling

- It describes how the components are connected.

- They are assumed to exist in local working directory or in a library.

- Structural modeling facilitate the use of hierarchy and abstraction in modeling complex systems.

- This model can be integrated into models that also use processes.

- Example: Let's consider a structural model of 2:1 multiplexer as the following figure.

Structural Modeling
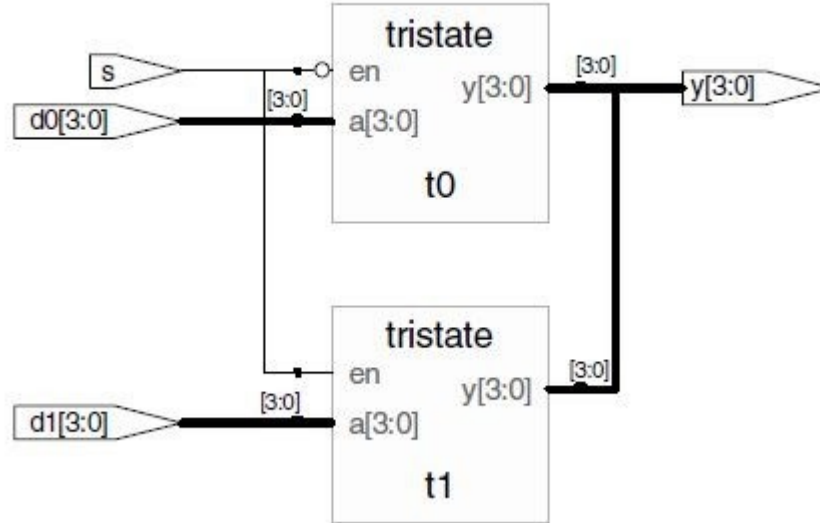
We can represent the VHDL structural code as below.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity mux2 is

port (d0, d1: in STD_LOGIC_VECTOR (3 downto 0);
s: in STD_LOGIC;
y: out STD_LOGIC_VECTOR (3 downto 0));
end;

architecture struct of mux2 is

component tristate

port (a: in STD_LOGIC_VECTOR (3 downto 0);
en: in STD_LOGIC;
y: out STD_LOGIC_VECTOR (3 downto 0));
end component;

signal sbar: STD_LOGIC;

begin
sbar <= not s;
t0: tristate port map (d0, sbar, y);
t1: tristate port map (d1, s, y);
end;
```

Structural

- In general, the topmost synthesizable entity is normally written with structural modeling.

- The structural model at the top includes all the entities that are written with RTL and connected together with port mappings.

Thank You