Lesson 12

Testbench (Combinational Logic)

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Testbench

- A major part of digital design is testing with simulation.
- A designer should never be satisfied if a VHDL code doesnt show any compilation or synthesis error.
- The design needs to be simulated with different inputs to see whether we are getting the correct output.
- The question is, how to simulate a circuit written in VHDL?
- There comes the testbenches.
- A testbench is another entity that takes the design under test (DUT) as a component.
- In this lesson, we will talk about testbenches written for combinational logics.
- We wrote an 8-bit adder in lesson 5. The entity was written as:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity adder_8bitc is
port (
 A,B: in unsigned(7 downto 0);
 C : out unsigned(8 downto 0) );
end adder_8bitc;

architecture adder_8bitc_arch of adder_8bitc is
begin
C  <= resize(A+B,9);
end adder_8bitc_arch;
```

Testbench

- We want to test this circuit.
- So we need a testbench.
- We create an entity testbench_tb that doesnt have any input or output ports.
- This entity contains the adder_8bitc entity as a component.
- The input and output ports are connected to a few signals instantiated in the testbench_tb entity.
- We can feed these signals with different input values at different time instances and check the output.
- The code of the testbench is given below,

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity testbench_tb is
end testbench_tb;
architecture testbench_arch of testbench_tb is
component adder_8bitc is
port (
A,B: in unsigned(7 downto 0);
C : out unsigned(8 downto 0) );
end component;
signal A: unsigned(7 downto 0) := (others=>'0');
signal B: unsigned(7 downto 0) := (others=>'0');
signal C: unsigned(8 downto 0) := (others=>'0');
```

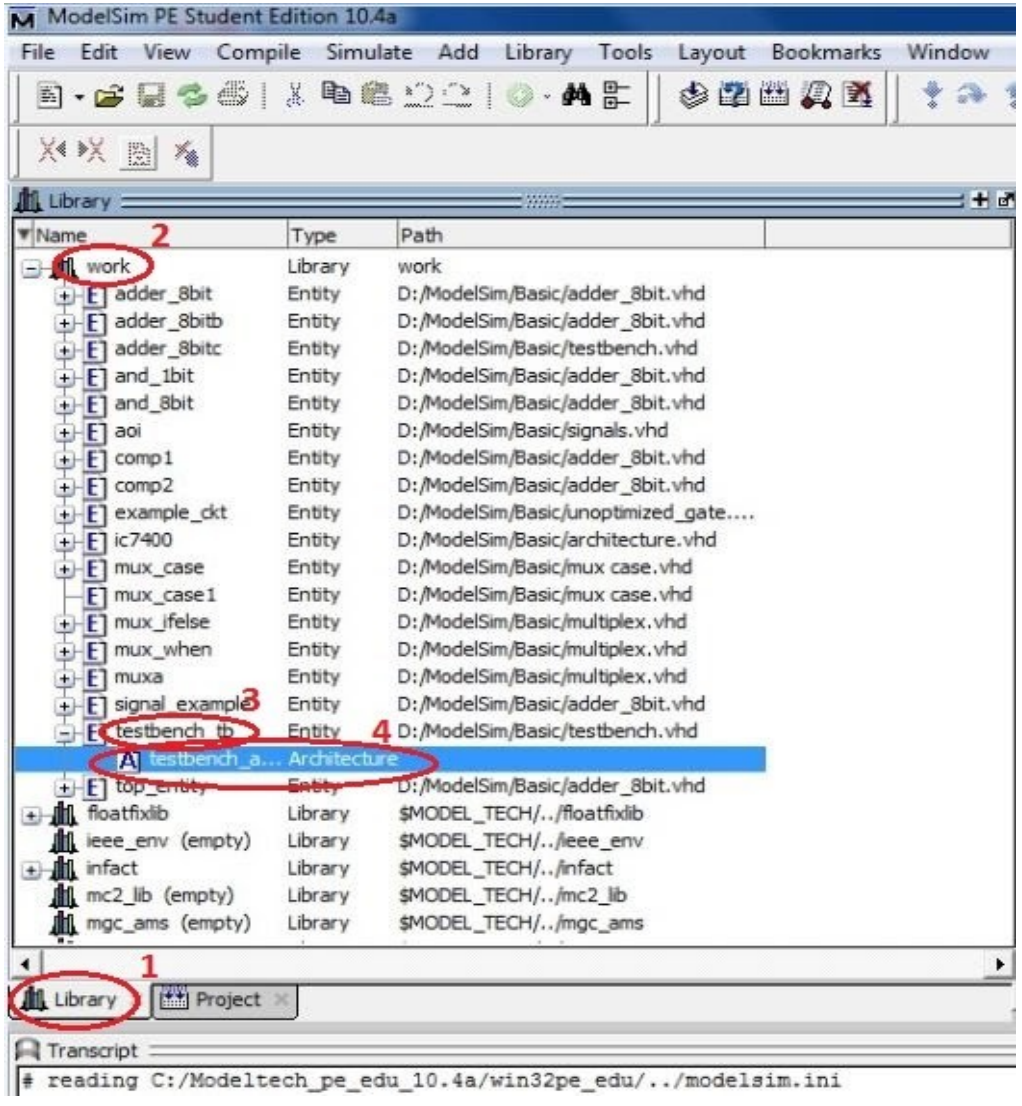
```
begin
adder_8bi: adder_8bitc port map(

A => A,
B => B,
C => C);
process
begin
wait for 100 ns;
A <= "00000010";
B <= "00000011";
wait for 10 ns;
A <= "00000110";
B <= "00000101";
wait;
end process;
end testbench_arch;
```

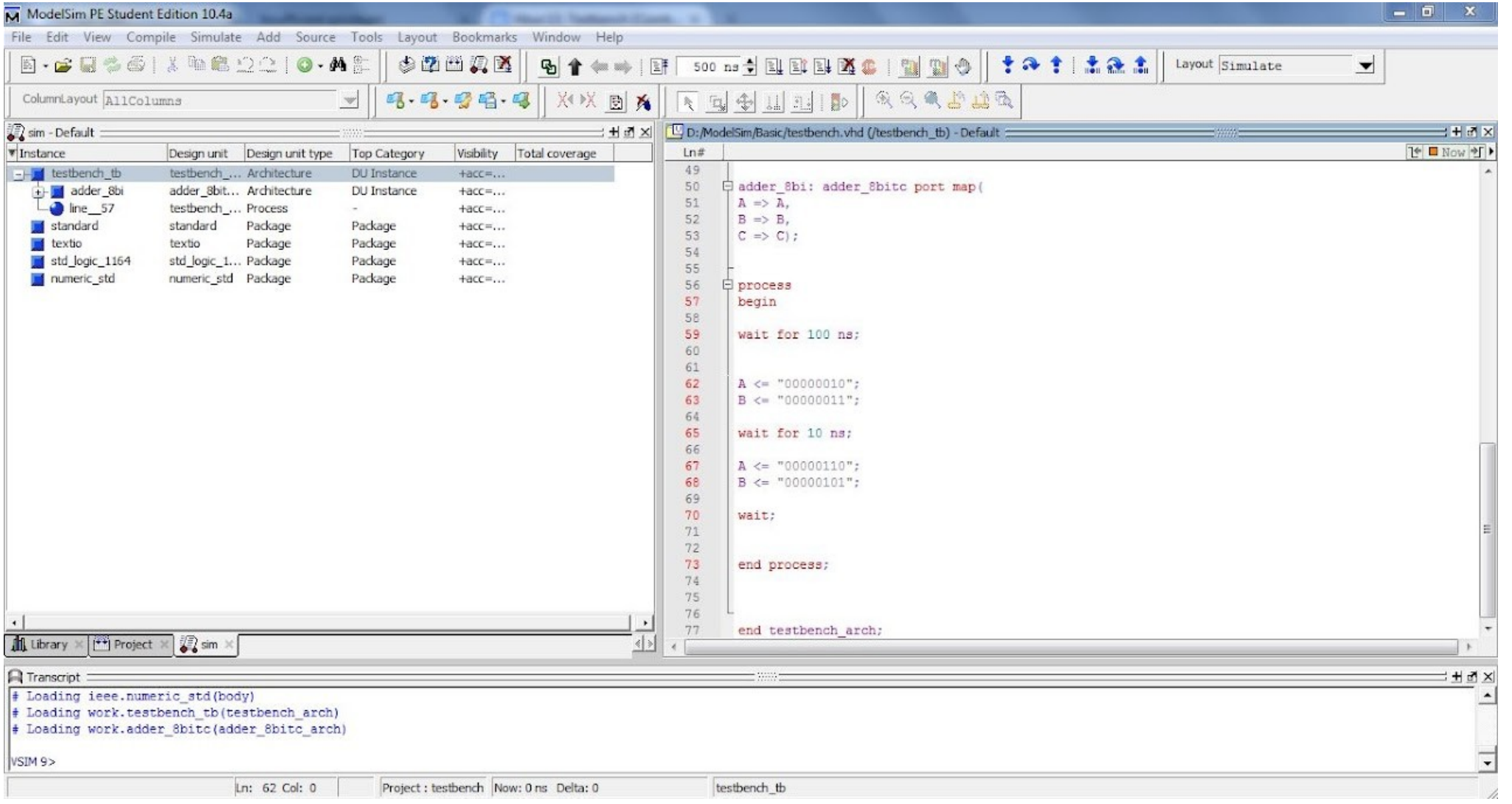
Testbench

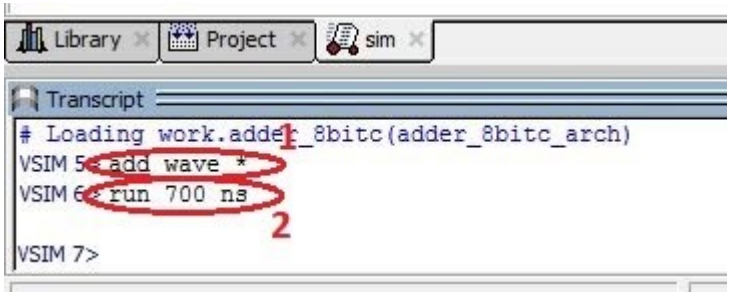
- In this case, we fed the inputs of adder_8bi with some values after 100ns.
- Then we wait for 10ns and feed next input values again.
- Afterwards, we wait indefinitely.
- Recall lesson 10, where we stated how behavioral codes use some extra features of VHDL language that are not supported for synthesis.
- The wait statements are not synthesizable.
- However, we don’t also want to synthesize the testbench.
- We just want to use this part of the code for testing.

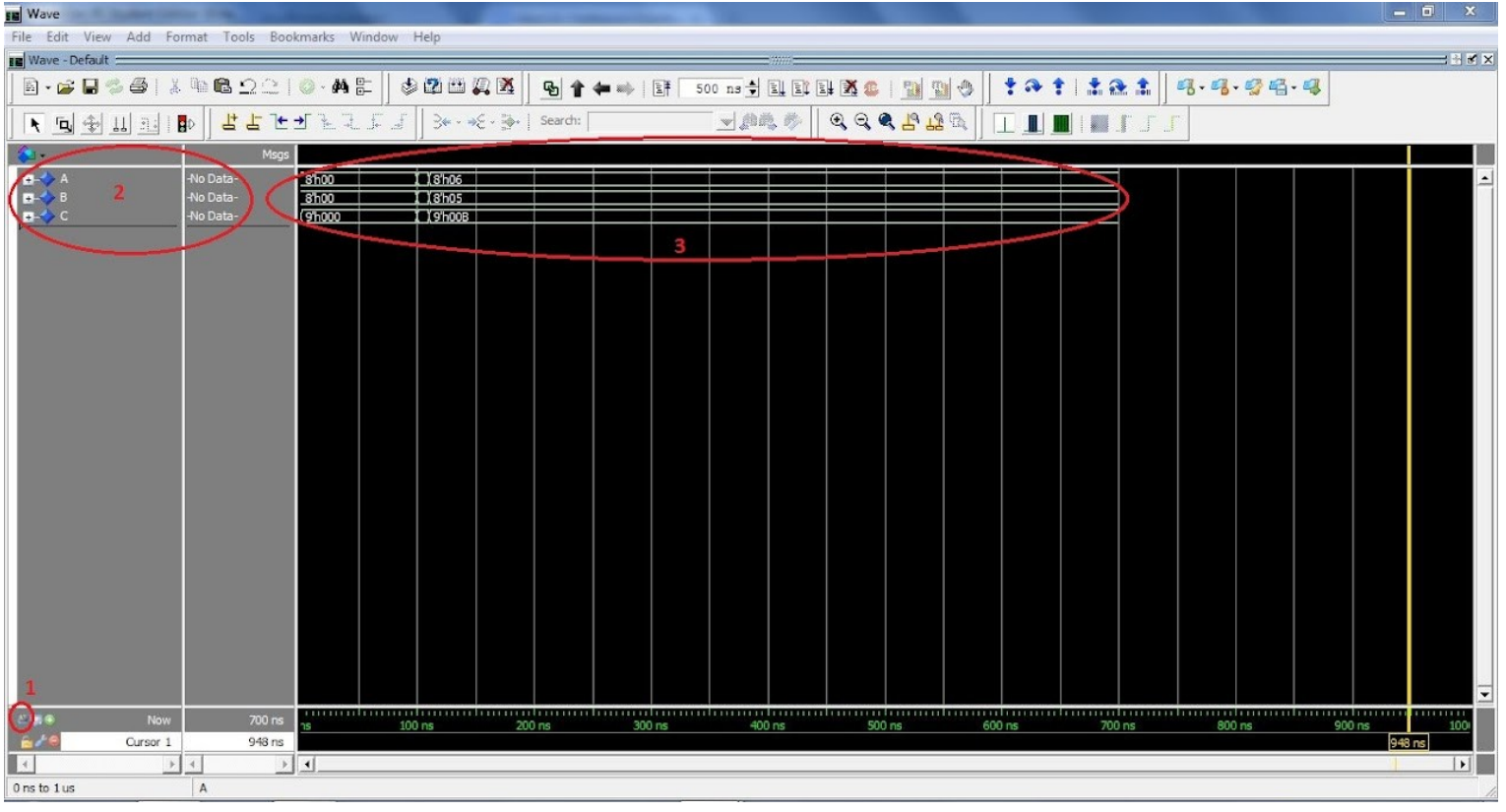
Run on ModelSim

- After compiling the above code click on the "library" (circle 1)>click on "work" (circle 2)>click "testbench_tb" (circle 3) as the project name was that. Then you will find the architecture file. Right click on that and select "Simulate".


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window
Library
Name
Type
Path
work
Library
work
adder_8bit
Entity
D:/ModelSim/Basic/adder_8bit.vhd
adder_8bitb
Entity
D:/ModelSim/Basic/adder_8bit.vhd
adder_8bitc
Entity
D:/ModelSim/Basic/testbench.vhd
and_1bit
Entity
D:/ModelSim/Basic/adder_8bit.vhd
and_8bit
Entity
D:/ModelSim/Basic/adder_8bit.vhd
aoi
Entity
D:/ModelSim/Basic/signals.vhd
comp1
Entity
D:/ModelSim/Basic/adder_8bit.vhd
comp2
Entity
D:/ModelSim/Basic/adder_8bit.vhd
example_ckt
Entity
D:/ModelSim/Basic/unoptimized_gate....
ic7400
Entity
D:/ModelSim/Basic/architecture.vhd
mux_case
Entity
D:/ModelSim/Basic/mux case.vhd
mux_case1
Entity
D:/ModelSim/Basic/mux case.vhd
mux_ifelse
Entity
D:/ModelSim/Basic/multiplex.vhd
mux_when
Entity
D:/ModelSim/Basic/multiplex.vhd
muxa
Entity
D:/ModelSim/Basic/multiplex.vhd
signal_example
Entity
D:/ModelSim/Basic/adder_8bit.vhd
testbench_tb
Entity
D:/ModelSim/Basic/testbench.vhd
testbench_a...
Architecture
top_entity
Entity
D:/ModelSim/Basic/adder_8bit.vhd
floatfixlib
Library
$MODEL_TECH/../floatfixlib
ieee_env (empty)
Library
$MODEL_TECH/../ieee_env
infact
Library
$MODEL_TECH/../infact
mc2_lib (empty)
Library
$MODEL_TECH/../mc2_lib
mgc_ams (empty)
Library
$MODEL_TECH/../mgc_ams
1
2
3
4
Library
Project
Transcript
reading C:/Modeltech_pe_edu_10.4a/win32pe_edu/../modelsim.ini


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Top Category Visibility Total coverage
testbench_tb testbench_... Architecture DU Instance +acc=...
adder_8bi adder_8bit... Architecture DU Instance +acc=...
line__57 testbench_... Process - +acc=...
standard standard Package Package +acc=...
textio textio Package Package +acc=...
std_logic_1164 std_logic_1... Package Package +acc=...
numeric_std numeric_std Package Package +acc=...
Library Project sim
D:/ModelSim/Basic/testbench.vhd (/testbench_tb) - Default
Ln#
49
50 adder_8bi: adder_8bitc port map(
51 A => A,
52 B => B,
53 C => C);
54
55
56 process
57 begin
58
59 wait for 100 ns;
60
61
62 A <= "00000010";
63 B <= "00000011";
64
65 wait for 10 ns;
66
67 A <= "00000110";
68 B <= "00000101";
69
70 wait;
71
72
73 end process;
74
75
76
77 end testbench_arch;
Transcript
Loading ieee.numeric_std(body)
Loading work.testbench_tb(testbench_arch)
Loading work.adder_8bitc(adder_8bitc_arch)
VSIM 9>
Ln: 62 Col: 0
Project : testbench
Now: 0 ns Delta: 0
testbench_tb


Library
Project
sim
Transcript
Loading work.adder_8bitc(adder_8bitc_arch)
VSIM 5> add wave *
VSIM 6> run 700 ns
VSIM 7>
1
2


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
A
B
C
-No Data-
-No Data-
-No Data-
8'h00
8'h00
9'h000
8'h06
8'h05
9'h006
2
3
1
Now
700 ns
Cursor 1
948 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
948 ns
0 ns to 1 us

Thank You