

# Lesson 23

## **FPGA and VHDL**

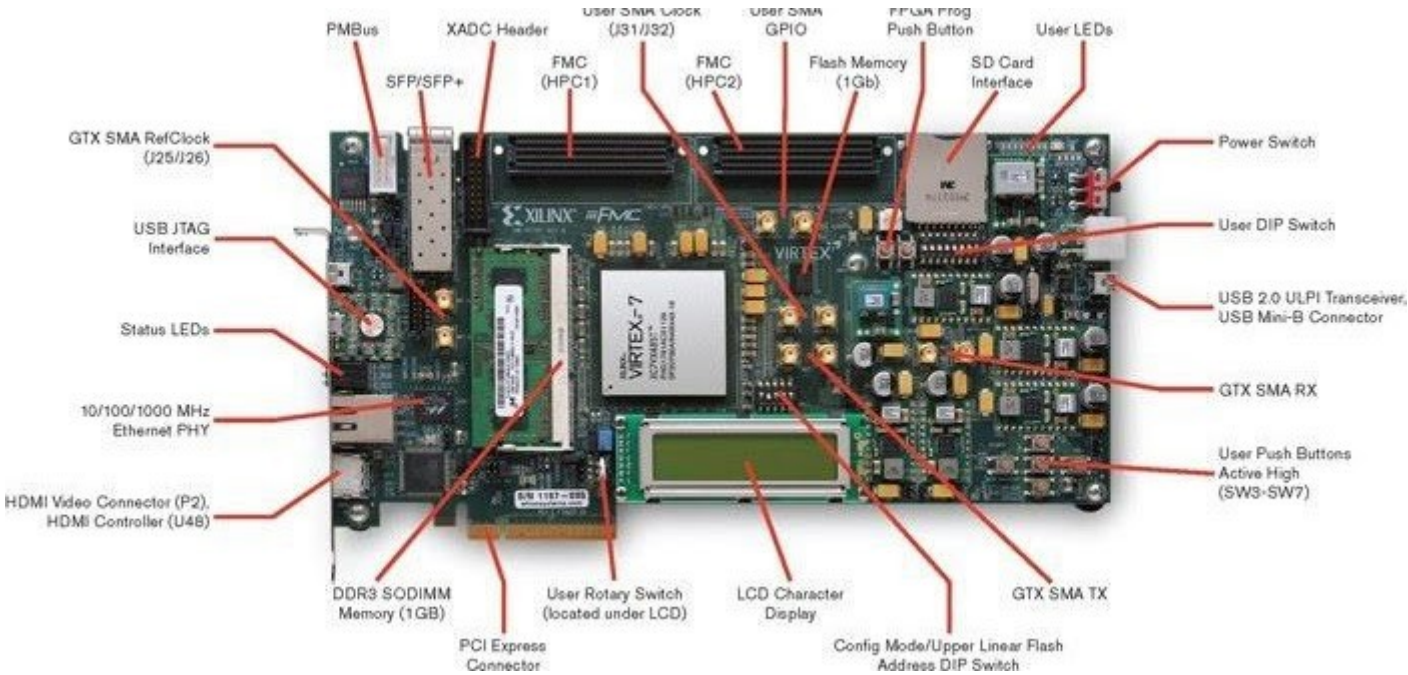
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# FPGA Basics

- # FPGA stands for field programmable gate array.
- # The FPGA chip is configurable or programmable. It is built with programmable logic blocks (PLB) and interconnects
- # The FPGA chip comes in a circuit board which also includes memory chips, external connectors and displays.
- # Most recent FPGA boards comes with ARM processors also making it a complete system-on-chip (SoC).
- # The word "field" is used because the device function can be modified "in the field"/at site where device is installed
- This is how a real life FPGA looks now-a-days. The main FPGA chip is in the middle with VIRTEX-7 written on it.

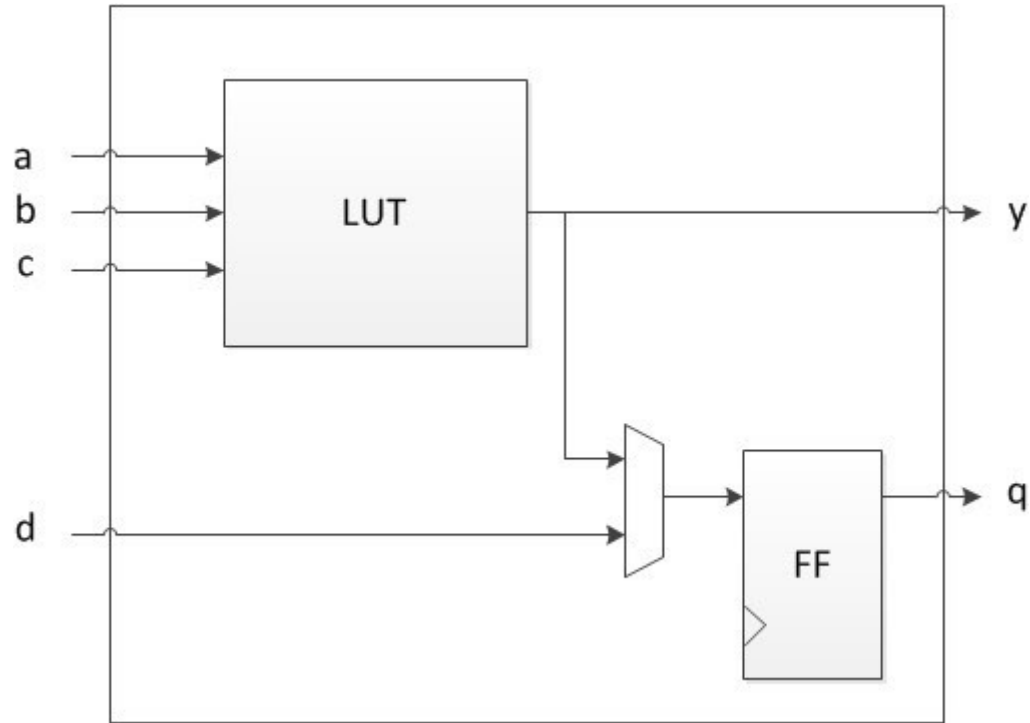
# FPGA



# FPGA

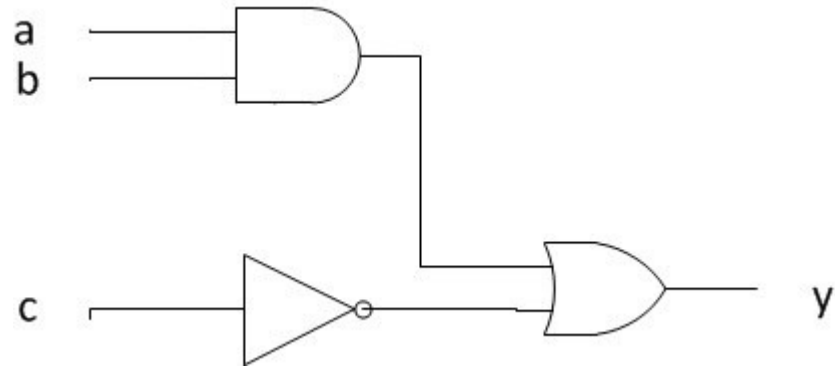
- The question is, how can a FPGA implement any circuits written with VHDL code?
- Lets take a look at an example. Lets assume, we have to implement the following circuit given in this figure.

# FPGA

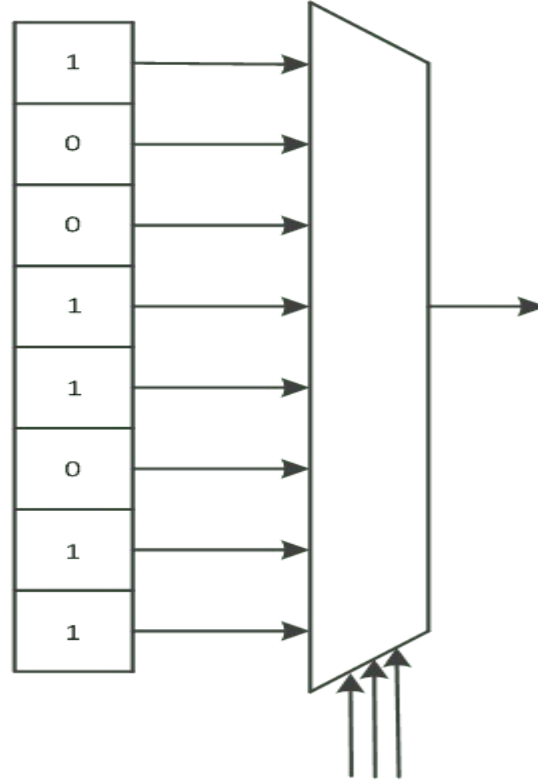


$$\# y = (a \& b) \mid !c$$

# FPGA

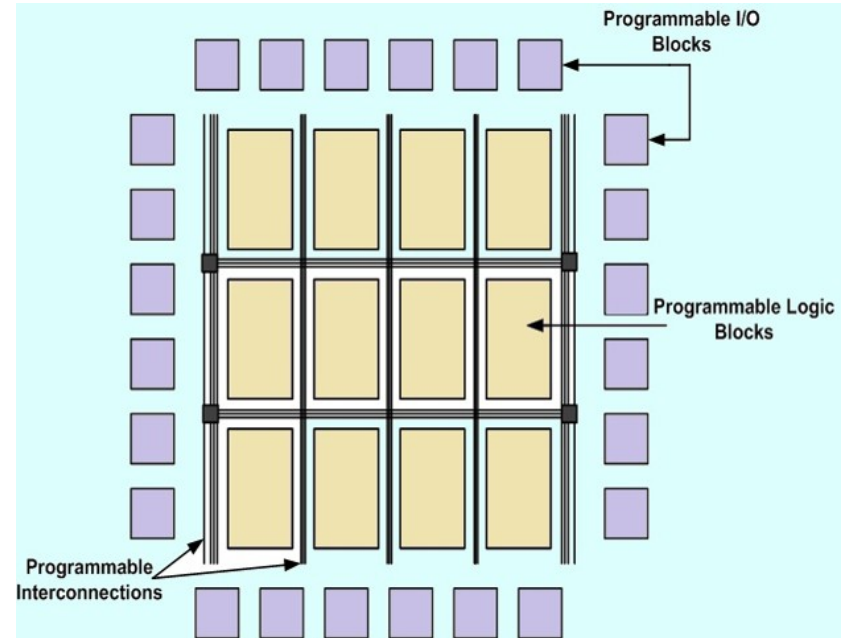


# FPGA



# FPGA

- Basic FPGA Architecture
- # Programmable I/O
- # Programmable Logic Blocks
- # Programmable Interconnect





# FPGA

- If one PLB doesn't have enough capacity, several of PLBs will work together to implement a logic.
- A very useful educational material is provided by Xilinx about how to code VHDL for a Xilinx FPGAs.
- I will summarize only the points that you need to know after finishing the earlier lessons of this site.

# FPGA

1. Use only active-high signals in HDL.
2. Use only synchronous resets for Xilinx FPGAs. For Altera, you might use asynchronous resets.
3. Avoid latches. FPGA tools have more accurate timing analysis for flop-based designs.

# FPGA

Rules for memory interface:

- a) For single- or dual-port RAM implemented in LUTs, describe the behavior of a synchronous write and an asynchronous read operation.
- b) For ROM inference in LUTs, create an array of constants.
- c) Single-port block RAM is inferred by having a synchronous write and a registered read address.
- d) For other configurations of the Xilinx block RAM, use the CORE Generator™ system.

Thank You