Lesson 16

Loop and Generate

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Loop

- VHDL supports while and for loop.
- Only the for loop is supported for synthesis.
- The for loops can be used to access the elements of arrays.
- We recommend to avoid while loops for RTL modeling
- We provide a code snippet here to show how VHDL for loops work.

Loop

```
..
...
when 6 =>
loop_7a: for i in 1 to 7 loop
Result_in(8,i) <= signed(Ltemp(i));
end loop;
when 7 =>
loop_8a: for i in 1 to 8 loop
Result_in(9,i) <= signed(Ltemp(i));
end loop;
...
...
```

Loop

- In this code snippet, we can see two for loops for two different conditions of case statement.
- This same code could be written in unrolled fashion like,

```
when 6 =>
Result_in(8,1) <= signed(L_temp(1));
Result_in(8,2) <= signed(L_temp(2));
Result_in(8,3) <= signed(L_temp(3));
Result_in(8,4) <= signed(L_temp(4));
Result_in(8,5) <= signed(L_temp(5));
Result_in(8,6) <= signed(L_temp(6));
Result_in(8,7) <= signed(L_temp(7));
when 7 =>
Result_in(9,1) <= signed(L_temp(1));
Result_in(9,2) <= signed(L_temp(2));
Result_in(9,3) <= signed(L_temp(3));
Result_in(9,4) <= signed(L_temp(4));
Result_in(9,5) <= signed(L_temp(5));
Result_in(9,6) <= signed(L_temp(6));
Result_in(9,7) <= signed(L_temp(7));
Result_in(9,8) <= signed(L_temp(8));
```

Loop

- It can be clearly seen how the loop reduced the VHDL code size.
- The syntax of for loop is

```
loop_label: for index in range loop
  statements
end loop;
```

Generate

- We didn’t create any signal in the for loop section, we just connected signals to one another.
- We can replicate a component several times with a for-generate statement.
- An example is given here,

```
architecture BEH of COUNTER_BIN_N is
component D_FF
  port(D, CLK_S : in BIT; Q, NQ : out BIT);
end component D_FF;
signal S : BIT_VECTOR(0 to N);
begin
   S(0) <= IN_1;
   G_1 : for I in 0 to N-1 generate
         D_Flip_Flop :
         D_FF port map
              (S(I+1), S(I), Q(I), S(I+1));
         end generate;
end architecture;
```

Generate

- The component to be replicated is D_FF. We use a generate statement to create N of this D-FFs.
- The syntax of for generate is,

  label: for parameter in range generate

  statements

  end generate;

Thank You