Lesson 24

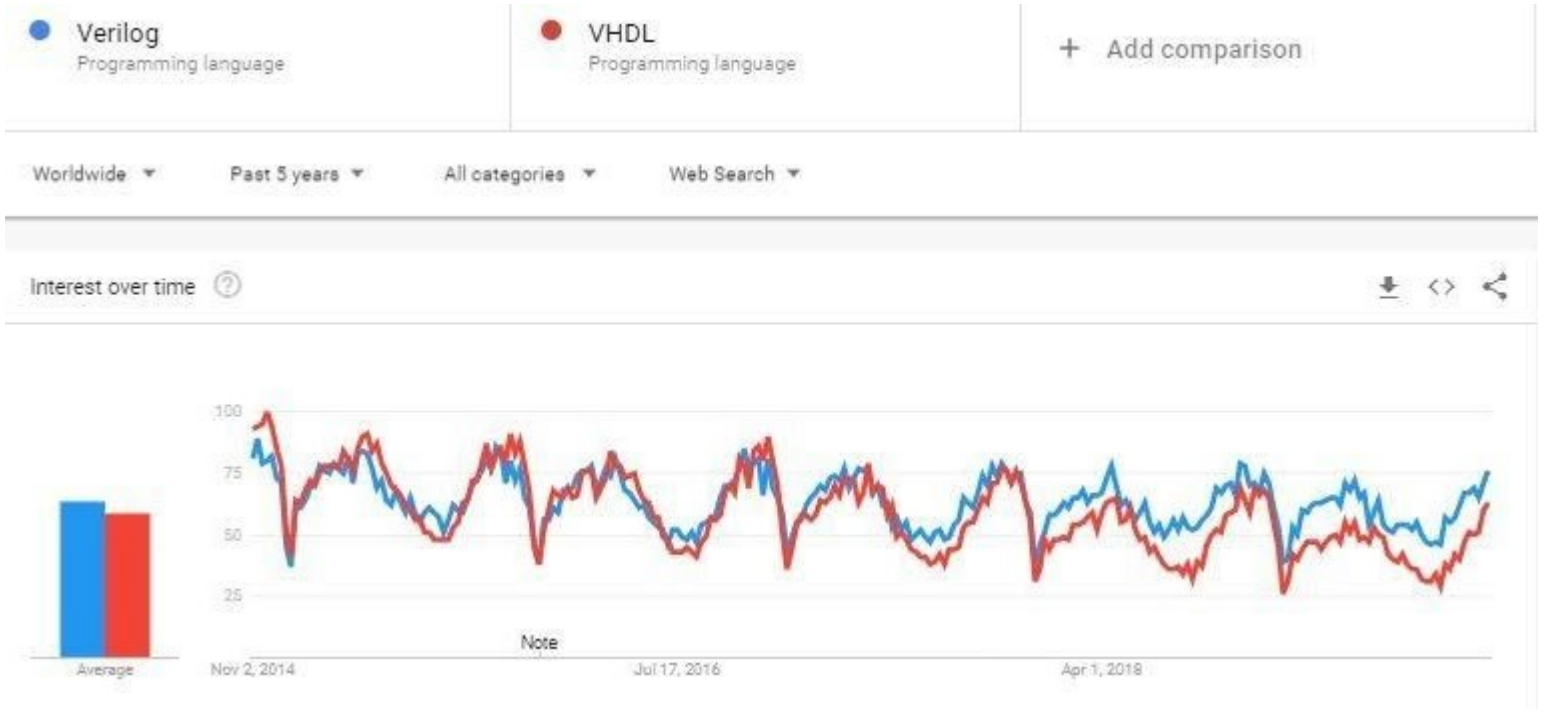
Conclusion

Mohd Saufy Rohmad
Technical Trainer and Consultant

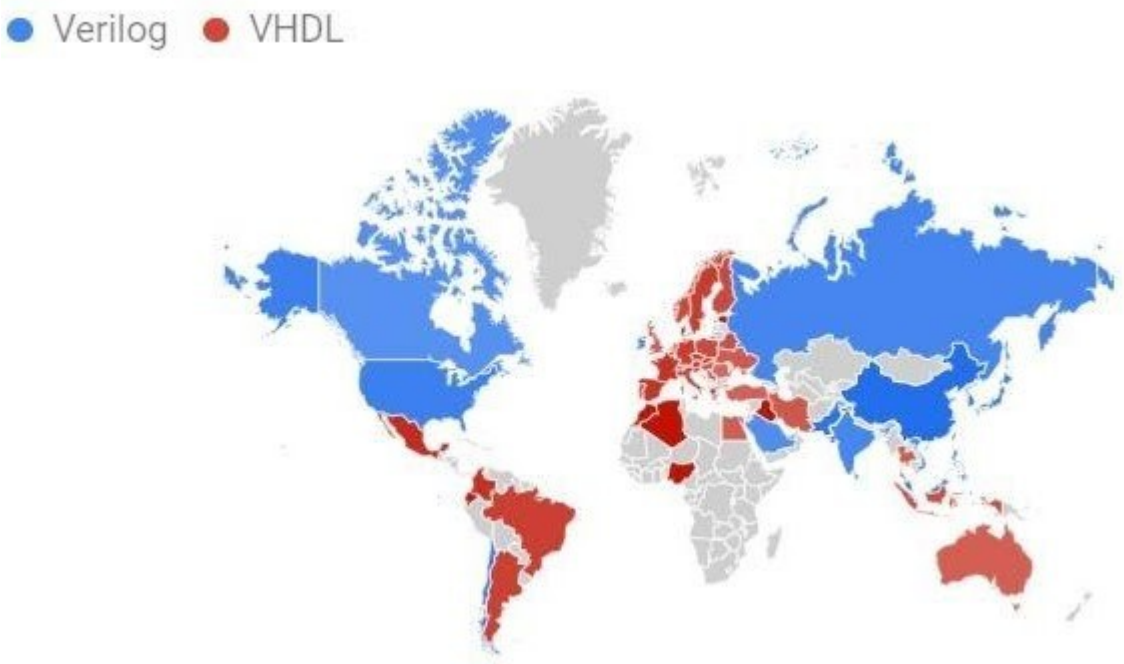
VHDL or Verilog?

- This is a very common question, should I learn VHDL or verilog?
- Verilog is more widely used for design in VLSI industries now-a-days.
- Nearly all industry use SystemVerilog for verification.
- Therefore, many industries choose verilog because they can be better integrated with SystemVerilog.
- VHDL is still very popular in Europe and in defense industries throughout the world.
- We can see in the google trends a comparison of popularity between the two languages in last 5 years

VHDL or Verilog?



VHDL or Verilog?



VHDL or Verilog?

- Verilog became popular because most software engineers with no hardware knowledge finds it easy to learn.
- However, there are two main advantages of VHDL in my opinion:

  (1) VHDL is a bit more difficult to learn than verilog. So, its easy for a VHDL designer to switch to verilog than the other way round.

  (2) VHDL is more strict and verbose. Therefore, less chance of errors. The designer has to know what he is trying to do.

Further Reading Materials

1. Tocci, Ronald J. Digital Systems: principles and applications. Pearson Education India, 1991.

2. Harris, David Money, and Sarah L. Harris. "Digital Design and Computer Architecture." (2019).

3. Kaeslin, Hubert. Top-down digital VLSI design: from architectures to gate-level circuits and FPGAs. Morgan Kaufmann, 2014.

4. Ashenden, Peter J. The designer's guide to VHDL. Vol. 3. Morgan Kaufmann, 2010.

5. Xilinx, Coding Style Guidelines

Thank You