A New Concept for Computing using Interconnect Crosstalks

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***Abstract*— Device, interconnect scaling and interconnection bottleneck are among the major challenges for CMOS scaling. Furhtermore, signal integrity issues like crosstalk—leakage of charge between capacitively coupled nets among neighboring signal lines—is becoming inexorable. We propose to astutely turn this detrimental effect into an advantage by engineering the interference among signal lines. Our proposal can potentially solve scaling challenges by reducing device and interconnect scaling requirements while complying with existing manufacturing paradigm. Central to our approach is the deterministic emulation of aggressor-victim scenarios in metal lines to achieve logic computation. The metal lines that carry inputs are called aggressor nets (number of aggressor nets is proportional to fan-in of the logic gate), and output signal carrying metal lines are called victim nets; aggressor nets are coupled to victim net through virtual lateral capacitance. As a result of input transitions on the aggressor nets, summation of aggressor nets charges is introduced on the victim net. The summation signal on victim net serve as outputs for logic gate, or used to control a pass transistor to get desired logic output. Depending on the boolean logic being computed, this sum of charges seen by victim net is controlled primarily by engineering the capacitance between aggressors and victims and by synchronous clocking. We have implemented basic gates including AND, OR and XOR, and compound logic circuits following this principle. Our results indicate huge potentials for compact and low-power computing using the proposed approach.**

Index Terms*— Signal Integrity, *Crosstalk, Capacitive Coupling, Crosstalk Logic(CL), Aggressor-Victim, 3-D CMOS.

Dense placement of devices with advancing technology nodes in 2D and 3-D CMOS approaches result in adverse close proximity effects among signal lines, which leads to increasing interference among neighboring signal lines due to strong capacitive coupling [1]. Also, with advancing nodes, increasing the vertical thickness of metal lines has been the solution to maintain the contradictory requirement of lateral shrinkage lines and low sheet resistance. But increasing vertical thickness of metal lines increases the lateral capacitances hence exacerbating the cross-talk noise. To address the issue, techniques in design, metal layer architecture, and material choices have been the approaches to damp the crosstalk, however, crosstalk is becoming incrementally inevitable in sub-10nm nodes[2]. In this short paper we show an approach to astutely turn the crosstalk interferences phenomena to compute logic. Fig. 2- Fig. 5 shows several examples. As shown in the Fig. 1, signal transition on Ag1 and Ag2 nets induce effective summation signal on Vi net through coupling capacitances C_C. The magnitude of signal induced depends on coupling capacitanc[3] value. Coupling capacitance is inversely proportional to the distance of separation of metal lines and directly proportional to the permittivity of the dielectric and lateral area of metal lines (which is length x vertical thickness of metal lines). Tuning the coupling capacitance values using its variables discussed above provides the engineering freedom to tailor the induced summation signal to specific logic implementation or as an intermediate control signal for further circuitry. We have implemented the basic gates using cross-talk mechanism. Our logic contains three states: Input State (IS) when Inputs are fed through aggressor nets (Ag1 and Ag2); Logic State (LS) when logic is evaluated; and Discharge State (DS) when floating nodes in the circuit are periodically discharged to ground hence gaining control over the floating nodes. We have achieved deterministic outputs in all CT (CrossTalk) circuit implementations which provide further improvement and development opportunities. Fig.2 show the CT-OR gate implementation, Fig.2a depict schematic, and Fig.2b hspice simulation of OR gate designed. It can be noticed from the figure that inputs A and B transition on aggressor nets during IS state while logic is evaluated during LS state, and during DS Vi node is discharged to zero. Similarly, Fig.3a show schematic for CT-AND gate and its output is shown in Fig.3b, here output(Vi) reaches high only when both inputs are high, low bumps during 0 1 and 1 0 inputs are assumed to be bellow threshold. Similarly, logic implementation of a non-linear circuit like XOR is shown in the Fig.3. Fig.3a is schematic and Fig.3b is output. In this gate, the output during input 1 1 reaches zero gradually during logic state, however, deterministic nature of our outputs shows potential for further improvement by tuning the capacitances. Fig. 5 show CT implementation of carry logic boolean expression (AC+B(A+C)). As shown in the schematic(Fig. 5a) a third aggressor net would serve as C input. The output of simulation is shown in Fig.5b. Fig 6 shows the stick diagrams of the logic expression in 2D CMOS and CT logic style. It can be observed that CT logic needs 2 transistors while CMOS needs 12 transistors, and CT logic consumes less footprint of .044 μm^2 while CMOS consumes .13 μm^2 foot print. The simple CT and summation bassed implementation of above logic expression shows the potential of CT logic with high fan in logic gates. Table I show transistor count and area comparisons of all logic circuits. Also, emerging 3-D approaches[4] provide additional 3-D architectural benefits to implement CT logic.

References:

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1)

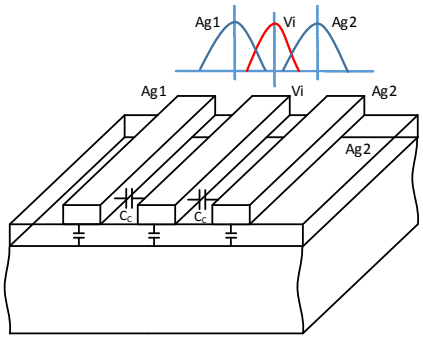

Fig.1.Crosstalk mechanism

2)

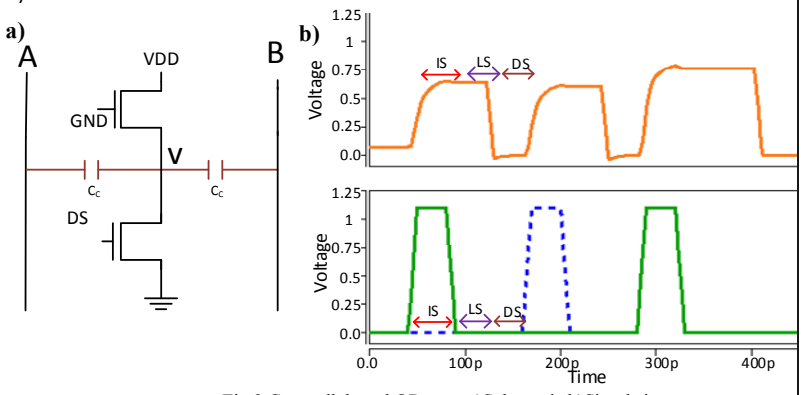

Fig.2.Crosstalk based OR gate, a)Schematic b)Simulation

3)

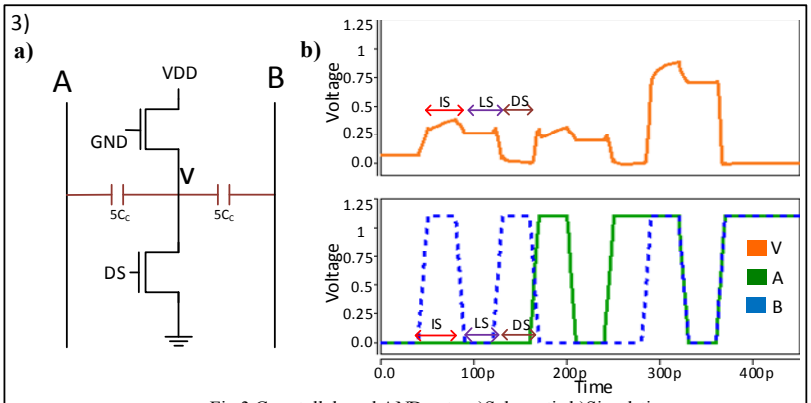

Fig.3.Crosstalk based AND gate, a)Schematic b)Simulation

4)

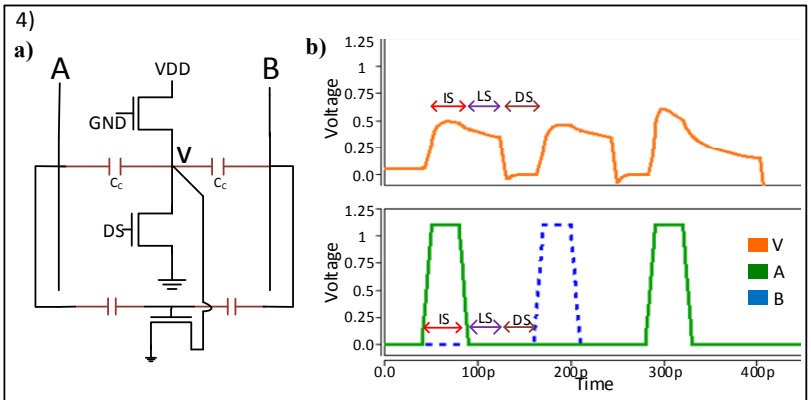

Fig.4.Crosstalk based XOR gate, a)Schematic b)Simulation

5)

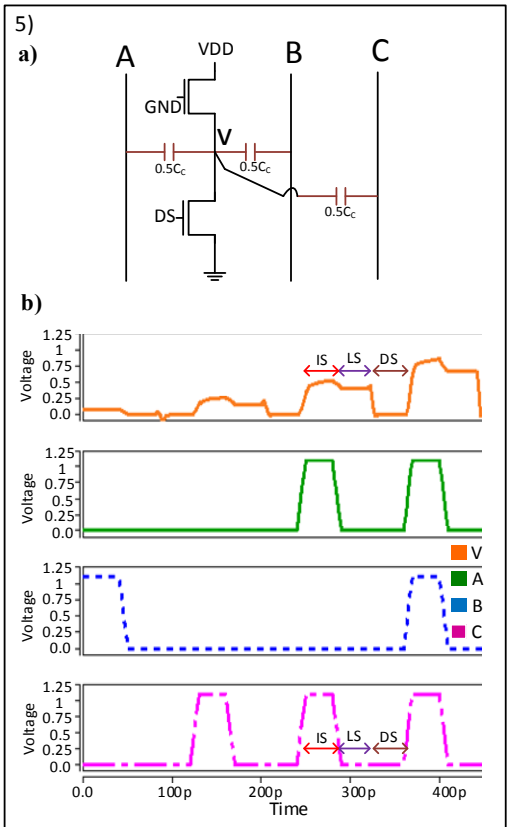

Fig.5.Crosstalk based Carry logic ,a)Schematic b)Simulation

6)

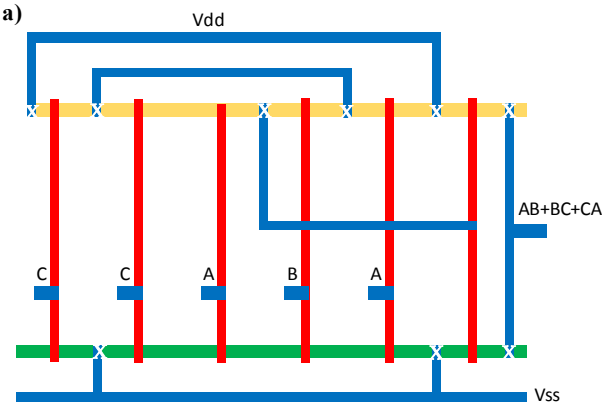

Fig.6.Stick diagrams of logic expression AB+BC+CA, a)2D CMOS style b) Crosstalk logic style

Table I: Transistor count and Area Comparisons

Logic gate	Transistor count	
	CMOS	CT
AND	6	2
OR	6	2
XOR	14	3
Carry	12	2

Logic gate	Area (μm^2)	
	CMOS	CT
AND	.069	.011
OR	.089	.011
XOR	.24	.018
Carry	.13	.015