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Nanosecond Gated CMOS Camera (NSGCC) Interface Control Document (ICD)

LLNL v4 Camera Board

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Rev.	Date	Section Edits	Eng.	Description of Change
2.1.2	4/10/2025	5, 6, 10, 11.1, 12.1, 13, 15, 16, 17, 18,	JMH BTF	nsCamera software release 2.1.2 Updated bit position 16 of STAT_REG to be the HST configuration done status bit for Icarus. Changed bit position 9 to state HST configuration has started. Rename of L/R hemisphere registers, subregisters, and signals to A/B Added SUSPEND_TIME, FPA_INTERFACE_STATE, DELAY_ASSERTION_ROWDCD_EN, HST_EXT_CLK_HALF_PER registers Added Phi Clock registers (HST_PHI_DELAY_DATA, EXT_PHI_CLK_SH0_ON, et al.) Added RSL configuration registers(RSL_CONFIG_DATA_B0, RSL_ZDT_MODE_A_EN, etc.) Added subregisters to HST_PHI_DELAY_DATA, TRIGGER_CTL, CTRL_REG, FPA_OSCILLATOR_SEL_ADDR Moved Radiation-Tolerant Modes Section of 14.9 to new Section 16 Edits for Daedalus implementation, and update to the register map. Added STAT_EDGE_DETECTS register for Daedalus to monitor 5 of the six edge detects. Changed HST_RO_IBIAS/HST_RO_NC_IBIAS from DAC E to state voltage is proportional to the frequency of the respective ring oscillators. Added sentence discussing self-clearing. Made registers that are self-clearing consistent to reader. Added Image Capture Definitions section. Updated Manual Shutter Control sections for Icarus and Daedalus. For Icarus, the hemispheres can be programmed independently. For Daedalus, the hemispheres cannot be programmed independently. Added reference to the jupyter notebook file in the nsCamera software package for how to use manual shutters. Changed hCMOS Project Manager from Jack Dean to Anne Garafalo. Updated Manual shutters description for both Icarus and Daedalus.

				Initialized HST timing modes for A and B hemispheres as unique to understand FPGA upsets. Updated STAT_REG bit positions 3 and 4 for the edge detect monitors between Icarus and Daedalus. Removed dual-edge functionality Updated VAB for Daedalus to be 1.0 V as opposed to 0.5 V (Icarus only). Corrected STAT_REG_SRC STAT_ARM on PDBIAS is ready to be not just Icarus only, but for both Icarus and Daedalus.

Previous change notes may be found in Section 21

Disclaimer

Contents

1 Background

The Ultra-Fast X-ray Imager (UXI) program is an ongoing collaboration between Sandia National Laboratories and Advanced Hybrid CMOS Systems (AHS) to create high speed, multi-frame, time-gated Read Out Integrated Circuits (ROICs), and a corresponding suite of photodetectors to image a wide variety of High Energy Density (HED) physics experiments on both Sandia's Z-Machine and LLNL's National Ignition Facility (NIF).

The Hybrid CMOS (hCMOS) sensors that have been designed by the UXI include the Icarus, which is an improvement on past imagers (Furi and Hippogriff), as well as the more recent Daedalus sensor. The Icarus is a 1024 × 512-pixel array with either 25 µm or 8 µm spatial resolution containing four frames of storage per pixel and has improved timing generation and distribution components while achieved 2 ns time gating. The Daedalus sensor is also a 1024 x 512-pixel array with 25 µm special resolution containing three frames of storage per pixel and has an increased set of features for a wider variety of applications from

interlacing of rows in each frame to configurability of all shutters.[1] See Section 15 for details regarding the Icarus implementation of the firmware and Section 16 for details regarding the Daedalus implementation.

Due to the unique test environments UXI sensors are targeted for, full custom hardware was required to physically mount an Icarus or Daedalus sensor, manage its various functions, and read out pixel data for transfer to a host computer. Beyond experimental functionality, the hardware also needed to accommodate sensor characterization requirements. Lawrence Livermore National Laboratory's 'Version 4.0 Board' was the result of these efforts. It mounts all the components required to fully utilize the Icarus and Daedalus sensors including analog to digital converters to convert pixel data and various system voltages to digital form for readout and analysis, DAC channels for remote configuration of critical bias voltages, static random-access memories to buffer pixel data, RS422 and Gigabit Ethernet communications for remote access, and an FPGA to tie these components together.

This document describes the FPGA electrical interfaces in detail to allow the reader a greater understanding of the device, and to facilitate implementation of custom software to control and manage it.

The Version 4.0 Board is a continuation of the Nano-second Gated CMOS hardware design that retains much of the functionality of the Version 1.0 board while adding features including a DAC instead of digital potentiometers, as well as sensors for pressure and radiation. The Version 4.0 board is intended for applications requiring tight form-factor enclosures. It is composed of two stacking boards; one holds the FPGA and regulators to power the various components of the board while the other contains the mating connector to the sensor, image-readoff ADCs, the DAC, and other components.

2 Design Summary

The Nanosecond Gated CMOS Camera (NSGCC) FPGA is a design targeted for the Microsemi A3PE3000-FG484 device residing on the LLNL Version 4.0 Board. It controls interaction between a host computer and the functions on the board, whose major components include an image sensor mounted on a daughter board, SRAM, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), temperature sensors, and power circuitry.

A summary of the feature set of the FPGA:

- RS422 and Gigabit Ethernet Ports for complete control of FPGA and sensor
- ARM/Disarm function which aggregates critical system status into one status bit
- Controls four NoBL (QDR) 72 Mbits SRAMs and four 8-channel ADCs for digitizing, buffering, and read out of pixel data to a host computer
- Utilizes an 8-channel DAC and two 8-channel ADCs for calibration, monitoring, and tuning of critical bias voltages
- Timer/Counter which increments at 1 second intervals while FPGA is running

[1] This paragraph was sourced from References 2, 4, 5, and 6.

- Temperature sensor to monitor the system temperature
- Radiation-tolerant logic
- Supports the board's sensor voltage protection circuitry and enables image sensor power only when the correct sensor is installed, and the connected power supply provides the proper voltage.
- Power Supply requirement is 7-12 Volts. The maximum current limit is 2.5 A.

A preliminary block diagram of the Version 4.0 Board, including the FPGA, is shown in Figure 1. The image sensor attaches to the Version 4.0 Board via a SamTec SEAF connector.

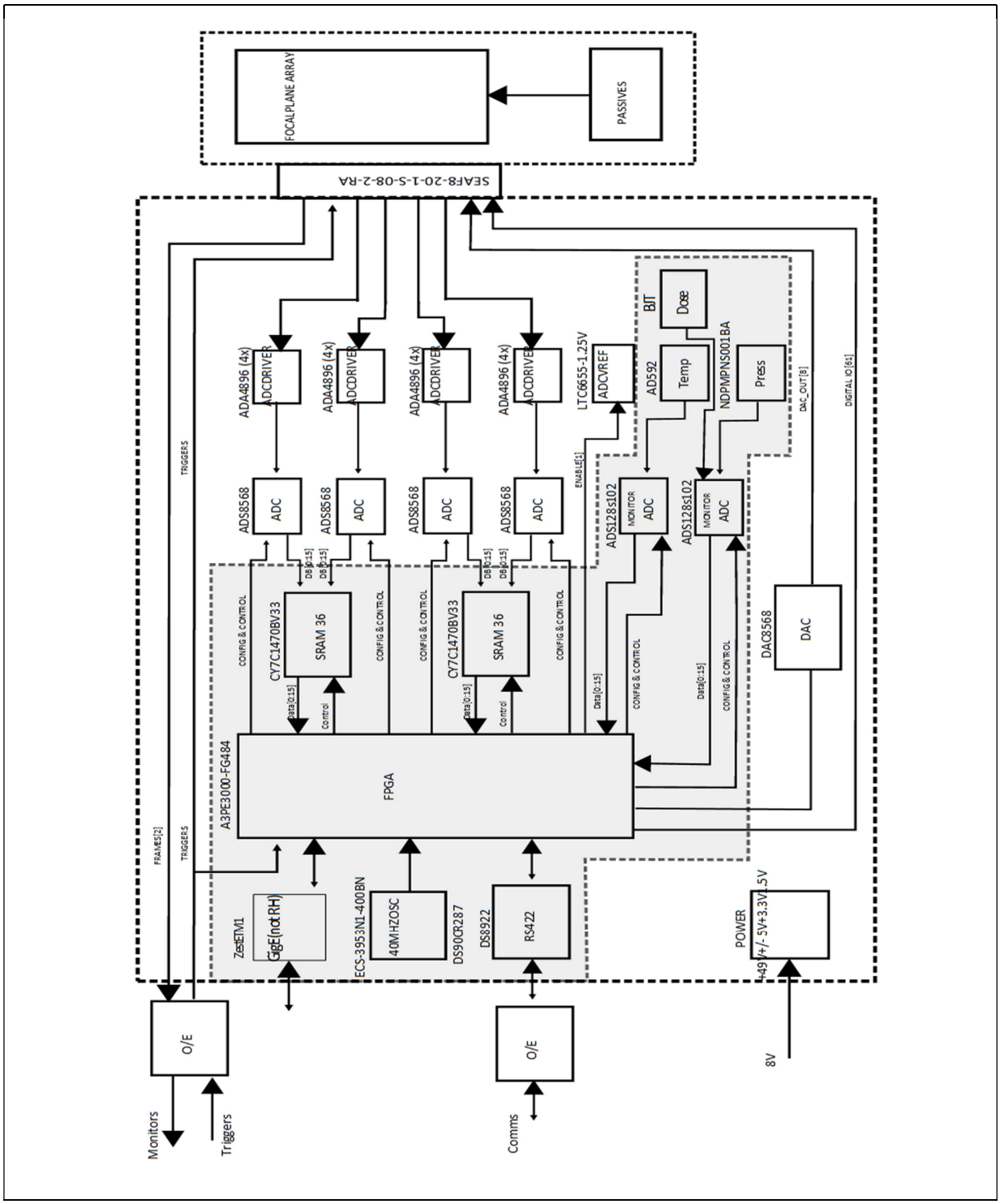

Figure 1: Version 4.0 Board, System Block Diagram

3 Block Diagram

A block diagram of the FPGA internal architecture is shown in Figure 2.

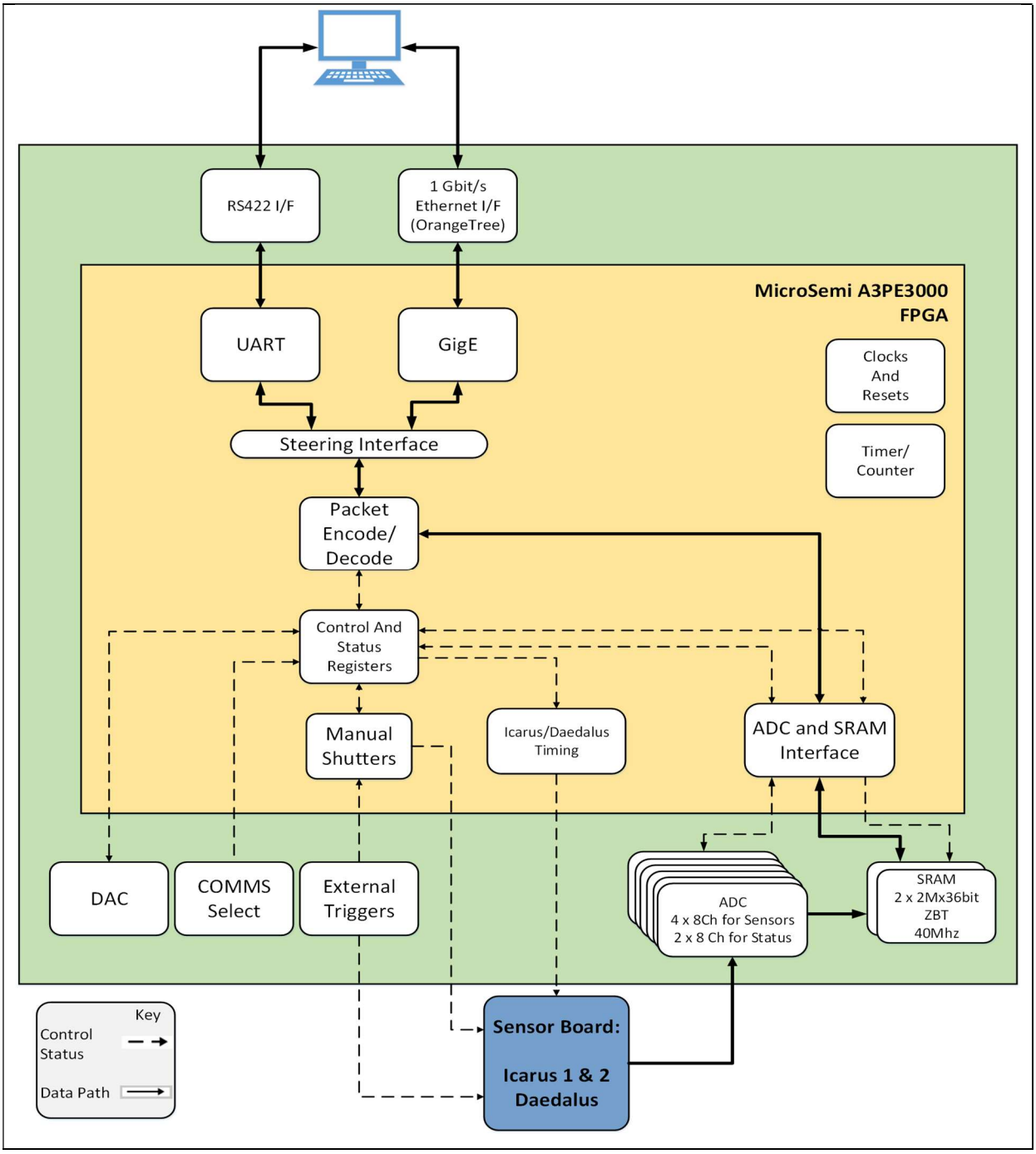

Figure 2: FPGA Block Diagram

4 Host Communications Interfaces

The NSGCC FPGA contains support for two serial interfaces for connectivity to a remote host computer—RS422 via a DB-9 connector, and Gigabit Ethernet via an RJ-45 connector. Only one port can be active at a time. Table **1** shows the typical time required to read data over the available interfaces.

Port	Readoff Time		
	ICARUS 2-Frame Readout	*ICARUS 4-Frame Readout*	*Daedalus 3-Frame Readout*
RS-422	~ 27 s	~ 54 s	~38 s
Gigabit Ethernet	< 1 s	< 1 s	< 1 s

Table 1: Approximate readoff time: Start of sensor readoff to image download by host (does not include software overhead)

The RS422 port has a fixed configuration of 921.6 kbaud, 8 data bits, 0 parity bits, and 1 stop bit; these settings cannot be modified by the user. The Gigabit Ethernet port can be accessed by connecting a standard Gigabit Ethernet adapter via a Cat 5a or better cable.

4.1 Communications Port Selection

Selection of the active communications port is performed through a configuration pin on the FPGA (*comm_port_sel_i*). Table **2** illustrates communications port selection. This table applies to all revisions of the LLNL V4.0 board.

'com_port_sel_i' Jumper State		Port Selected
comm_port_sel_i logic level	*Configuration*	
0	Short JMP1 to GND (Rev AA or AB) or short J5 (Rev AB or later)	RS422
1	Open JMP1 to GND (Rev AA or AB) or open J5 (Rev AB or later)	Gigabit Ethernet

Table 2: Communications Port Selection using FPGA Input Pins

5 Sensor Interface

The NSGCC FPGA controls the configuration and readout of the sensor in timing coordination with ADC conversion and SRAM storage. These functions are implemented with state machines, control logic, and command/status registers that respond to commands received from the host computer. ADC and SRAM functions will be discussed in the following sections: consult the associated sensor-specific ICD for relevant details. The hCMOS sensors, Icarus and Daedalus, consist of two hemispheres that can be independently controlled. The hemispheres are labeled A and B; alternatively, they may be referred to as the left and right hemispheres, respectively. *Warning*: physical 'left' and 'right' will depend upon the deployed orientation of the sensor.

5.1 ADC Interface and Control

The FPGA controls the six analog-to-digital converters (ADCs) on the board. Four of the ADCs are used to convert the image sensor's analog pixel information into 16-bit digital data, while the fifth and sixth are used to monitor DAC channel voltages. The four ADCs used to convert the image sensor's analog pixel information are Texas Instruments ADS8568SPM, which are eight-channel 16-bit devices.

The fifth and sixth ADCs (ADC5 and ADC6) are used to monitor a subset of the board's DAC channels. See Sections 15 and 16 for the mapping of ADC5 inputs for the Icarus and Daedalus sensors, respectively.

The FPGA reads ADC5 and ADC6 periodically and writes the voltage data into the **ADC5_DATA_1** through **ADC5_DATA_4** and **ADC6_DATA_1** through **ADC6_DATA_4** registers; these can be read by the user at any time. The time between updates of these registers is controlled by the **ADC_PPER** register. The associated DAC channels that are monitored are also described in Sections 15.2 and 16.2 for Icarus and Daedalus implementations respectively.

Prior to use, host software must configure the ADCs properly using the **ADC_CTL** and **ADC*X*_CONFIG_DATA** registers (see Section 13.1). First, the appropriate **ADC*X*_CONFIG_DATA** register(s) must be configured (see the ADS8568SPM data sheet for configuration information). Then the **ADC_CTL** register must be written to force the FPGA to write the configuration data to the targeted ADC(s).

5.2 SRAM Interface and Control

Each of the image sensor ADCs presents its output to the SRAM one channel at a time such that 4×16-bits, or 64 bits of data must be buffered simultaneously and continuously until all intended data is read from the sensor and stored in the SRAM. To handle storage of this data, the Version 4.0 Board contains two Cypress CY7C1470BV33-167AXI 2Mbit×36 SRAMs. When all pixel data has been stored, the FPGA asserts a status bit (**STAT_REG_SRC** bit 0, or **SRAM_READY**). Software waits for this bit to go high and commence readout of pixel data from SRAM to the host for storage and processing.

5.3 Automatic Sensor Detection

Currently, the LLNL V4 board is not able to provide automatic sensor detection.

5.4 Image Capture Definitions

The hCMOS sensors uses Metal-Insulator-Metal (MIM) capacitors to store the pixel charge. The number of capacitors is associated with the number of frames: the Icarus' four frames require four MIM capacitors, while the Daedalus' three frames require three capacitors. Relevant descriptive terms are as follows:

Sensor Image Capture: Arm and Trigger event, enables the shutters and stores pixel voltages in the MIM capacitors.

Pixel Readout: The hCMOS sensor's MIM capacitor voltages are converted to digital data which is then stored in the camera's SRAM. This can occur sequentially after image capture by using triggers or using dedicated methods in firmware and software to perform pixel readout even when image capture has not occurred.

SRAM Readout: The digital data stored in the SRAM is transmitted via RS422 or GigE to the host computer. Can be triggered "manually" in software, possibly bypassing Image Capture and Pixel Readout.

6 Trigger Control

Two triggers are required to initiate image capture and retrieve images from the board—a Coarse Trigger, followed by a Fine Trigger. These triggers can be provided to the board through either hardware (external) or software (internal) triggers. Table 3 indicates the relevant subregister settings.

Subregister	Hardware Trigger	Software Trigger
HW_TRIG_EN	1	0
SW_TRIG_EN	0	1

Table 3: Subregister settings for trigger control

6.1 Hardware Triggers

The default trigger mode requires the use of external equipment to provide hardware triggers. The hardware trigger requirements are:

- Hardware triggers are enabled by asserting the **HW_TRIG_EN** subregister while de-asserting **SW_TRIG_EN** (i.e., setting bit 0 of **TRIGGER_CTL** while clearing bit 2.)
- Both triggers must adhere to TTL logic levels as measured on the board
- Both triggers must have a minimum 60 ns pulse width as measured on the board
- For Icarus sensor operation, a minimum of 35 µs is needed between the rising edge of the Coarse Trigger and the rising edge of the Fine Trigger to obtain a successful edge detect (w0_top_a_edge1) assertion after the assertion of the Fine Trigger. Please see the 'UXI_Icarus_FPA' document for more details regarding the edge detect signal from the Icarus sensor.[5]

  For Daedalus sensor operation, the Fine Trigger must be held low at least 35 µs for a successful edge detect (SH2_fall_UR). If the FPGA is set to program the sensor using the RSL Interlacing mode, the Fine Trigger must be held low for 200 µs to obtain a successful edge detect. Please see the 'Daedalus HDD-v2' document for more details regarding the edge detect signal from the Daedalus sensor.[6]
- The signal source must be able to drive a 50 Ω load since both triggers are terminated on the board.

6.2 Software Triggers

The software triggers are generated internally to the FPGA and exceed the requirements for the hardware triggers; the pulse width of both triggers is 10 µs and the rising edges occur 100 µs apart.

The software trigger is enabled by asserting the **SW_TRIG_EN** subregister while de-asserting **HW_TRIG_EN** (clearing bit 0 of **TRIGGER_CTL** while setting bit 2). When subregister **SW_TRIG_START** is asserted, the software control logic will activate and assert first the Coarse Trigger then the Fine Trigger as described in the previous paragraph. **SW_TRIG_START** is self-clearing, so software does not need to clear it to disable this function.

Note that inside the FPGA, the hardware and software triggers are logically ORed together. Therefore, when the Software Trigger function is used, the hardware triggers must not be asserted.

This functionality should not be confused with the direct use of the **SW_COARSE_TRIGGER** subregister, which is used to send only a Coarse Trigger for programming of the sensor.

7 Digital-to-Analog Converter Channels

There are eight DAC channels on the board that are used to bias miscellaneous image sensor functions. The DAC is a TI8568 device; configuration is performed via the DAC data registers (**DAC_REG_A_AND_B**, **DAC_REG_C_AND_D**, **DAC_REG_E_AND_F**, and **DAC_REG_G_AND_H**), and the DAC control register (**DAC_CTL**).

To ensure that the DAC channels are programmed to valid values immediately upon turning on system power, the FPGA will detect the de-assertion of the system reset signal, and after a 1 ms delay will automatically program all DAC channels to the default values contained in their respective DAC data registers. See Sections 15 and for the Icarus and Daedalus DAC assignments, respectively. Specific voltages that the Daedalus sensor should bias are described in Table 14 in Section 16.2 .

When the user writes to the **DAC_CTL** register, a DAC write command is initiated. It takes some time for the command to be generated, serialized, sent to the DAC, and for the DAC interface module to then terminate the process. If a DAC write is initiated while a previous DAC write is still in progress, the second DAC write will neither be executed nor buffered; it will be lost. This is not an issue when using the RS422 interface due to the slow communications rate but is potentially a problem when using the Gigabit Ethernet interface. Interface software must not execute a DAC write command for at least 50 µs following a previous DAC write command when the Gigabit Ethernet interface is used.

8 Temperature Sensor

Two functionally identical temperature transducers in parallel are used to measure the temperature. The temperature transducers (AD592 and ISL71590SEH) differ in their radiation tolerance. Analog voltage measured at the output voltage can be converted to temperature via the conversion, 1 mV = 1 Kelvin since a 1 kΩ pull-down resistor is used. The on-board 12-bit ADC monitor, ADC128S102, converts the analog reading to digital and stores the reading into the appropriate section of a register, e.g., ADC5_DATA2(11:0).

In order to reduce the number of bits needed for storage, the temperature is recorded in Celsius rather than Kelvin, (the lowest temperature is never expected to be less than 0 degrees Celsius). This shifts the digital value stored lower by 339 (equivalent to 273.15 K) using the calculation:

$$Round\left[(273.15\ Kelvin)\left(\frac{2^{12} counts}{3.3\ V}\right)\left(\frac{1\ V}{1000\ mV}\right)\left(\frac{1\ mV}{1\ Kelvin}\right)\right] = 339\ counts$$

For example, assume that a 12-bit digital reading of `0x1C6` is read by the ADC monitor. The decimal conversion of `0x1C6` is 454 counts. We shift this down by subtracting 339 to get 115. This in turn can be converted to a temperature in Celsius:

$$Temp = (measurement - 339\ counts)\left(\frac{3.3\ V}{2^{12}\ counts}\right) = \frac{(454 - 339) * 3.3\ V}{2^{12}}$$
$$= 92.65\ mV \rightarrow\ 92.65\ ^{\circ}C$$

Shifting the temperature range in this manner allows all expected temperature values to be represented in 7 bits, without requiring a change of scale. The resulting value is stored in the **STAT_REG_SRC** status register and is accessible from the **STAT_TEMP** subregister.

After the system is powered on, the FPGA will continually read the temperature transducers at an interval determined by the **ADC_PPER** register.

9 Pressure Sensor

A Honeywell NBPLPNN030PAUNV absolute-type pressure sensor is used to measure the board's environmental pressure. This device exhibits a maximum measurement of 30 PSI. The 12-bit ADC monitor, ADC128S102, polls the monitor of two separate pressure outputs: pressure positive and pressure negative. The polling is performed in the same manner as the temperature sensor. The calculation to convert the monitored readings in mV to PSI using the difference of pressure positive and pressure negative is as follows:

Given a nominal sensitivity of the sensor of $21\frac{mV}{V}$, the dimensional conversion from volts to PSI is

$$21\ \frac{mV}{V/_{span}}\left(\frac{5\ V/_{span}}{30\ PSI}\right) = 3.5\frac{mV}{PSI}$$

The sensitivity of any particular pressure sensor can be anywhere in the range between 15.5 and 26.0 mv/V/span, and there is a potential offset of ±7 mv/V, so accurate pressure readings require sensor calibration.

The maximum pressure reportable by the sensor is 30 PSI, thus the maximum voltage difference is calculated as 140 mV. In hexadecimal this is 0x8C. Since this can be represented in eight bits, we can neglect the higher four bits of the twelve-bit monitor and store the results in eight bits of register space.

10 Miscellaneous Firmware Features

Several FPGA (firmware) features are available on Icarus and Daedalus Interfaces.

10.1 Firmware Startup

When the camera is powered on, the firmware holds itself in reset for 100 ms. Experiments show that the FPGA needs to be held in reset for at least 100 ms for the firmware clock to properly stabilize. A firmware clock buffer intellectual property (IP) core is implemented as opposed to a Phase Lock Loop or Multi-Mode Clock Module, etc. as both experimentation and literature research provide evidence that clock buffers exhibit more radiation tolerance. The clock buffer buffers the 40 MHz crystal oscillator that is instantiated by the FPGA.

The default HST timing modes for both Icarus and Daedalus firmware builds are initialized as follows:

- A hemisphere: 2-3 timing mode (2 ns integration with 3 ns interframe time) with 4 ns delay.
- B hemisphere: 5-3 timing mode (5 ns integration with 3 ns interframe time) with 1 ns delay.

These settings are made on startup to allow for analysis of potential upsets to the firmware. Having unique timing modes for both hemispheres helps to provide an insight into upsets to the FPGA.

10.2 Photodiode Bias Control and Status

The Photodiode Bias (the onboard 49 V switching regulator) can be turned off when using boards with firmware revisions AC and later. The FPGA can shut down the regulator at the respective shutdown pin by setting the **PDBIAS_LOW** subregister to '1'. The feature allows for sensor hot-swapping and for taking data while the photodiode is not biased for comparison.

The status of the photodiode bias can be read from the **PDBIAS_UNREADY** subregister. A '0' value indicates the bias is functional (exceeding 10 V), while a '1' indicates a faulty or non-functional bias below 10 V.

10.3 Delaying Pixel Readoff

The pixel readout from an Icarus sensor can be delayed by the firmware. A counter is implemented in the FPGA before readoff from the sensor is initiated. The delay time is set by the **DELAY_READOFF** register, up to a maximum of 107 seconds.

10.4 Power-On Image Reset Mode

The power-on image reset mode allows the user to extract reasonable images from the SRAMs after power-up or reset. This is a fallback mode for when image-readoff fails due to communication error or FPGA upset. Currently, this feature is available only for the Icarus hCMOS sensor. Power-on image reset mode is the default mode for the standard Icarus firmware. The standard Daedalus firmware does not yet include this mode. Pixel readoff is initiated 175 ms after the FPGA is held in reset.

11 Packet Formats

The NSGCC FPGA supports three packet types: Command, Response, and Burst Response (i.e., pixel) Packets. Their formats and usage are described in this section.

11.1 Command Packet

A Command Packet is sent by the host to the FPGA; it may not be sent by the FPGA. A Command Packet is used to send an instruction to the FPGA for execution. All Command Packets shall have the format shown in Table 4.

16 bits	4 bits	12 bits	32 bits	16 bits
Preamble	Command	Address	Data	CRC16

Table 4: Command Packet Format

Preamble	Bit pattern that precedes actual packet data to assist the receiver in determining the start of the packet. The preamble is fixed to 0xAAAA
Command	0x0: Write Single 0x1: Read Single 0x2: Read Burst (i.e., Read Pixels) All other values not supported
Address	Bit[11:0]: Defines the address of the target register of a Write Single or Read Single command. For a Read Burst command, this field is not used, but is recommended that it be filled with zeros.
Data	Bit[31:0]: Contains write data for a Write Single command. This field is not used for Read Single or Read Burst commands, but it is recommended that it be filled with zeros.
CRC16	Bit[15:0]: CRC-16 field, calculated over the entire packet, excluding the preamble and CRC field itself. The CRC16 field exists for RS422 packets only; for Ethernet packets, the CRC16 field does not exist.

Table 5: Command Packet Fields

11.2 Response Packet

A response packet is sent by the FPGA to the host; it may not be sent by the host. Response Packets are sent either (1) in response to a Write Single packet where the response packets are not disabled, or (2) in response to a Read Single packet.

The Response Packet format is similar to the Command Packet format; this enables host software to easily correlate a Response Packet to the Command Packet that was the cause of its generation. However, there are a couple of minor differences, such as asserting the MSB of the Command field, and the content of the Data field.

16 bits	4 bits	12 bits	32 bits	16 bits
Preamble	Command	Address	Status	CRC16

Table 6: Response Packet Format

Preamble	Bit pattern that precedes actual packet data to assist the receiver in determining the start of the packet. The preamble is fixed to 0xAAAA
Command	Contains the contents of the command field of the corresponding Command Packet, except that the MSB is asserted. 0x8: Write Single 0x9: Read Single 0xA: Read Burst (i.e., Read Pixels)
Address	Same as the source Command Packet
Status	For Read Single Commands: This field contains the data read from the target register. For Write Single Commands: This field contains status information, particularly errors, contained in the transmitted command packet. This status information does NOT refer to the response packet. Bit[0]: CRC error Bit[1]: Invalid Command – command not executed Bit[2]: Invalid Sub-Command – command not executed
CRC16	Bit[15:0]: CRC-16 field, calculated over the entire packet, excluding the preamble and CRC field itself. The CRC16 field exists for RS422 packets only; for Ethernet packets, the CRC16 field does not exist.

Table 7: Response Packet Fields

11.3 Burst Response Packet

Burst Response (or Pixel) Packets are sent in response to a Read Burst (or Read Pixels) command.

16 bits	4 bits	12 bits	32 bits	Variable	16 bits
Preamble	Command	Address	Status	Payload	CRC16

Table 8: Burst Response Packet Format

Preamble	Bit pattern that precedes actual packet data to assist the receiver in determining the start of the packet. The preamble is fixed to 0xAAAA
Command	Contains the Command field of the Command Packet, except that the MSB is asserted. 0xA: Read Burst (i.e. Read Pixels)
Reserved	Field is not used, should be set to 0x000
Payload Length	Length of the Payload field, in bytes. This is the total number of bytes transmitted for a particular SRAM readout.
Payload	Payload. This field contains pixel data. Each pixel occupies 16-bits of payload; if the actual pixel data is less than 16 bits, the pixel data shall be zero-justified
CRC16	CRC-16 field, calculated over the entire packet, excluding the preamble and CRC field itself. The CRC16 field exists for RS422 packets only; for Ethernet packets, the CRC16 field does not exist.

Table 9: Burst Response Fields

12 Instructions

Three instructions are currently supported: Write Single, Read Single, and Read Burst.

The Write Single instruction is used by the host to update and modify the NSGCC FPGA's control registers. By writing to the appropriate control registers in the correct sequence, the host can control all NSGCC FPGA and Version 4.0 Board functions. When the FPGA receives a command packet with a Write Single instruction with response packets enabled, it will return a response packet indicating reception of the packet and whether it was received error-free.

The Read Single instruction is used to read the content of a single NSGCC control or status register. This instruction enables the host to determine the status of all FPGA functions that are supported. When a command packet with a Read Single instruction is received by the FPGA, it *must* return a response packet, which contains the FPGA target register contents. Again, it is up to the host to determine a suitable timeout period while awaiting the response packet and to re-send the packet if required.

The Read Burst instruction is used to read sensor data from the Version 4.0 Board's SRAM; it should be sent by the host only after pixel data is read from the ADC and stored in SRAM. When this instruction is received by the FPGA via a command packet, it will return a single of Burst Response packets with the format described in the previous section.

13 Registers

This section lists all NSGCC FPGA registers accessible by the software. All registers are 32 bits wide, although not all bits are used in every register. Registers or individual bits of registers may be self-clearing; that is, the firmware will ingest any bits set then automatically clear them. The different register types are defined as follows:

- Read Only: Software can read the register but cannot modify its contents. The register's contents are updated/modified only by internal FPGA hardware.
- Read/Write: Software can read or write the register; hardware cannot update/modify the register contents, unless stated.
- Self-Clearing: Software can read the register; the register's contents are cleared (i.e., reset to zeros) when read by software. However, if software has not resolved the underlying cause of asserted status bits, reading this type of register may not result in all zeros being read from it. A typical example is an interrupt register, when the underlying source of the interrupt has not been cleared.

13.1 Register Map

A pale green background indicates an Icarus-specific setting; pale gold indicates a Daedalus-specific setting. Unless 'Icarus2' is specified in an entry, 'Icarus' refers to both Icarus and Icarus2.

Address	*Register Name*		*Board*	*Access*	*Default value*
Register description	*Bit range*	*Details of bit range (may include **SUBREGISTER_NAME**)*			
0x000	**FPGA_NUM**		V1, V4		0x8400_0301
Product Number of the FPGA design Eight-character sequence: 1: Board developer 2: Board revision number 3-5: Unused 6: Communication interfaces 7: Radiation tolerance 8: Sensor build	31	Board developer			
		0	SNL		
		1	LLNL		
	30:28	Unused			
	27:24	Board major revision number			
		0001	LLNLv1		
		0100	LLNLv4		
	23:10	Unused			
	9	'1' indicates Gigabit Ethernet interface implemented			
	8	'1' indicates RS422 interface implemented			
	7:5	Unused			
	4	Radiation tolerance. '1' indicates optimized radiation-tolerant implementation			
	3:0	Sensor implementation			
		0000	Undefined		
		0001	Icarus		
		0010	Daedalus		
		0011	Reserved		
0x001	**FPGA_REV**		V1, V4	Read-only	---
Revision of FPGA design.	7:0	Day of FPGA code release (ex: 0x29 for the 29th day of the month)			
	15:8	Month of FPGA code release (ex: 0x12 for the month of December)			
	23:16	Year of FPGA code release (ex: 0x18 for the year 2018)			
	27:24	Unused			

		31:28	Board version (ex: 0x4 for v4 board)		
0x010	**HS_TIMING_CTL**		V1, V4	Read/Write, self-clearing	0x0000_0000
Control of HS Timing Function		0	**HST_MODE** - Configure timing. This bit is self-clearing. When '1', HST configuration is initiated with respect to the FPA interface.		
0x013	**HS_TIMING_DATA_ALO**		V1, V4	Read/Write	0xC631_8C60
Custom high-speed timing A side, LSBs		31:0	Timing pattern bits [31:0] for A side. Initialized in the firmware along with HST_TIMING_DATA_AHI to 2-3 timing mode with 4 ns delay.		
0x014	**HS_TIMING_DATA_AHI**		V1, V4	Read/Write	0x0000_0018
Custom high-speed timing A side, MSBs		7:0	Timing pattern bits [39:32] for A side. Initialized in the firmware along with HST_TIMING_DATA_ALO to 2-3 timing mode with 4 ns delay.		
0x015	**HS_TIMING_DATA_BLO**		V1, V4	Read/Write	0x7C7C_7C7C
Custom high-speed timing B side, LSBs		31:0	Timing pattern bits [31:0] for B side. Initialized in the firmware along with HST_TIMING_DATA_BHI to 5-3 timing mode with 1 ns delay.		
0x016	**HS_TIMING_DATA_BHI**		V1, V4	Read/Write	0x0000_007C
Custom high-speed timing B side, MSBs		7:0	Timing pattern bits [39:32] for B side. Initialized in the firmware along with HST_TIMING_DATA_BLO to 5-3 timing mode with 1 ns delay.		
0x017	**SW_TRIGGER_CONTROL**		V1, V4	Write-only, self-clearing	---
Initiates generation of internal coarse and fine triggers		0	**SW_TRIG_START** - When written with '1', initiates coarse and fine triggers internal to FPGA. The coarse trigger will be 10 µs long, followed by a delay of 11.5 µs, then followed by a 10 µs fine trigger.		
0x018	**HST_READBACK_A_LO**		V1, V4	Read-only	---
HST configuration readback		31:0	HST configuration readback with respect to RSL state machine (bits [31:0] for A side)		
0x019	**HST_READBACK_A_HI**		V1, V4	Read-only	---
HST configuration readback		7:0	HST configuration readback with respect to RSL state machine (bits [39:32] for A side)		
0x01A	**HST_READBACK_B_LO**		V1, V4	Read-only	---
HST configuration readback		31:0	HST configuration readback with respect to RSL state machine (bits [31:0] for B side)		
0x01B	**HST_READBACK_B_HI**		V1, V4	Read-only	---
HST configuration readback		7:0	HST configuration readback with respect to RSL state machine (bits [39:32] for B side)		
0x01C	**SW_COARSE_CONTROL**		V4	Write-only, self-clearing	---

Software Coarse trigger control		0	**SW_COARSE_TRIGGER** - When written with '1', initiates a software coarse trigger. This trigger is a pulse of one FPGA clock cycle to initiate the coarse trigger functionality of configuring the hCMOS sensor. The firmware will then wait for a fine trigger.		
0x024	**STAT_REG**		V1, V4	Read-only	---
Status Register. (Read-only duplicate of STAT_REG_SRC)		31:0	Read-only shadow bits of **STAT_REG_SRC** (0x02F). Reading this register has no effect on these bit values. To clear the applicable bits, **STAT_REG_ SRC** must be read. See 0x02F for bit assignments		
0x025	**CTRL_REG**		V1, V4	Read/Write	0x0000_0000
Control Register		0-1	Unused		
		2	**COLQUENCHEN** - Column Quench Enable. When '1', enables column quench function		
		3	**POWERSAVE** - Power Save Mode. Controls the assertion of *HST_osc_bias_en* to save power.		
			0	*HST_osc_bias_en* is tied high continuously	
			1	*HST_osc_bias_en* is asserted upon the rising edge of the Coarse Trigger; *HST_osc_bias_en* is de-asserted when sensor readout begins	
		4	**REVREAD** - When '1', reverses the frame readout order		
		4	**SLOWREADOFF_0** – Part of a test register for slowing down image-readoff. Bit 4 is the LSB and Bit 5 is the MSB. If bits 4 and 5 are set as "01", then readoff is slowed by a factor of 2. If bits 4 and 5 are set as "10", then readoff is slowed by a factor of 3.		
		5	**SLOWREADOFF_1** – Part of a test register for slowing down image-readoff. Bit 4 is the LSB and Bit 5 is the MSB. If bits 4 and 5 are set as "01", then readoff is slowed by a factor of 2. If bits 4 and 5 are set as "10", then readoff is slowed by a factor of 3.		
		6	**PDBIAS_LOW** – When '1', the PDBIAS +49 V regulator will be disabled. When '0', the regulator will be enabled.		
		7	**ROWDCD_CTL** – When '1', the *row_dcd-enable* input to the sensor will be asserted indefinitely. When '0', the input to the sensor will be controlled by the FPGA's FPA interface.		
		8	**MANSHUT_MODE** – If '1', enable manual shutters. If '0', use high-speed timing. See 0x050 for Icarus manual shutter control		
		9	**INTERLACING_EN** – Enable interlacing mode		
		10	**IMAGE_DATA_RETRIEVED** – Indicator that the user has retrieved all image data from camera. This is a self-clearing bit.		
0x026	**DAC_CTL**		V4	Read/Write	0x0000_0000

DAC configuration control for specific channels	0	**DAC_CONFIG** - When written with a '1', the DAC selected by DAC_SEL will be configured with the value in its corresponding register. This bit is self-clearing.		
	3:1	**DAC_SEL[2:0]** - Selects the DAC channel to configure. Selection is sequential, i.e., "000" = select DAC A, "001" = select DAC B … "111" = select DAC H		
0x027	**DAC_REG_A_AND_B**		V4	Read/Write	---
DAC A and B configuration data See Section 15.2 and 16.2 for DAC channel description of Icarus and Daedalus implementations respectively.	15:0	**DACB / HST_A_NDELAY** – see register 0x09C. Control voltage to respective sensor pin. It is the A side n transistor delay buffer voltage. Decreasing the voltage increases the delay of the side n transistor.[5]			3.3 V
	31:16	**DACA / HST_A_PDELAY** – see register 0x099. Control voltage to respective sensor pin. It is the A side p transistor delay buffer voltage. Decreasing this voltage increases the delay of side n transistor.[5]			0 V
0x028	**DAC_REG_C_AND_D**		V4	Read/Write	---
DAC C and D configuration data See Section 15.2 and 16.2 for DAC channel description of Icarus and Daedalus implementations respectively.	15:0	**DACD / HST_B_NDELAY** – see register 0x09A. Control voltage to respective sensor pin. It is the B side n transistor delay buffer voltage. Decreasing this voltage increases the delay of the side n transistor.[5]			3.3 V
	31:16	**DACC / HST_B_PDELAY** – see register 0x09B. Control voltage to respective sensor pin. It is the B side p transistor delay buffer voltage. Decreasing this voltage increases the delay of the side n transistor.[5]			0 V
	31:16	**DACC / HST_OSC_VREF_IN** – see register 0x09B. Reference voltage for 500 MHz oscillator.[6]			2.9 V
0x029	**DAC_REG_E_AND_F**		V4	Read/Write	---
DAC E and F configuration data See Section 15.2 and 16.2 for DAC channel description of Icarus and Daedalus implementations respectively.	15:0	**DACF / HST_OSC_CTL** – see register 0x09C. Control voltage to the relaxation oscillator. Decreasing this voltage increases the speed of the oscillator.[5]			1.45
	15:0	**DACF/ COL_TST_IN**– see register 0x09C. Global column current source analog test input pin.[6]			0 V
	31:16	**DACE / HST_RO_IBIAS / HST_RO_NC_IBIAS** – see register 0x098. Control voltage to either the ring with capacitors or without capacitors oscillator determined by register 0x047. Increasing this voltage increases the speed of the oscillator.[5]			2.5 V
	31:16	**DACE / HST_OSC_CTL** – see register 0x098. Control voltage to the 500 MHz oscillator. Decreasing this voltage increases the speed of the oscillator.[6]			1.0 V

0x02A	**DAC_REG_G_AND_H**		V4	Read/Write	---
DAC G and H configuration data See Section 15.2 and 16.2 for DAC channel description of Icarus and Daedalus implementations respectively.	15:0	**DACH / VRST** – see register 0x098. Controls the pixel reset voltage.[5, 6]			.3 V
	31:16	**DACG / VAB –** see register 0x097. Controls the pixel anti-bloom transistor voltage.[5, 6]			.5 V
	31:16	**DACG / VAB –** see register 0x097. Controls the pixel anti-bloom transistor voltage.[5, 6]			1.0 V
0x02D	**SW_RESET**		V1, V4	Write-only, self-clearing	`0x0000_0000`
Software reset	0	**RESET** - *sw_rst.* When asserted, will reset the entire FPGA, including control and status registers. This bit will be automatically cleared after written.			
0x02E	**HST_SETTINGS**		V1, V4	Read-only	---
High Speed timing control	0	**HST_SW_CTL_EN** - When '1', the hstAllWEn pin to the sensor will be directly controlled by the *sw_hst_all_wen* bit. When '0', hstAllWEn will be controlled by FPGA logic.			
	1	**SW_HSTALLWEN** - Will directly drive the hstAllWEn pin to the sensor when *HST_sw_ctl_en* is '1'; e.g., when both HST_SW_CTL_EN and SW_HSTALLWEN are '1', then the hstAllWEn pin to the sensor will be driven to a logical '1' (i.e. high)			
0x02F	**STAT_REG_SRC**		V1, V4	Read-clear	---
Status Register, Source. Contains the source logic for clearable status bits, whereas STAT_REG contains read-only copies. All bits in STAT_REG_SRC register will be cleared when the register is read, except for the Temperature Sensor and the Pressure Sensor bits. Use register `0x02F` to read these bits	0	**SRAM_READY** - sensor readout is complete			
	1	**STAT_COARSE** - Coarse Trigger detected			
	2	**STAT_FINE** - Fine Trigger detected			
	3	**STAT_W3_TOP_A_EDGE1** – Rising edge of fourth frame shutter of top-A hemisphere detected (an edge detect monitor). This is a diagnostic one-shot rising edge of shutter 3 of top of FPA in hemisphere A.			
	3	**STAT_SH0_RISE_B** – Rising edge of first frame shutter of B hemisphere detected (an edge detect monitor). This is a diagnostic one-shot rising edge of shutter 0.			
	4	**STAT_W3_TOP_B_EDGE1** - Rising edge of fourth frame shutter of top-B hemisphere detected (an edge detect monitor. This is a diagnostic one-shot rising edge of shutter 3 of top of FPA in hemisphere B.			
	4	**STAT_SH0_FALL_B** - Falling edge of first frame shutter of B hemisphere detected (an edge detect monitor). This is a diagnostic one-shot falling edge of shutter 0.			
	5	**STAT_SENSREADIP** - Sensor Readout In Progress; Indicates the start of an ADC read cycle in which 32 pixels will be read from the sensor (8 channels x 4 ADCs)			

	6	**STAT_SENSREADDONE** - Sensor Readout Complete – Asserted by ADC control logic; indicates that sensor readout is complete
	7	**STAT_SRAMREADSTART** - SRAM Readout Started - Indicates that SRAM readout has started. This is tied to bit 0 of the SRAM_CTL register, which is controlled by software
	8	**STAT_SRAMREADDONE** - SRAM Readout Complete – Indicates that SRAM readout is complete (all pixels have been read out of SRAM)
	9	**STAT_HSTCONFIGSTART** – HST configuration started
	10	**STAT_ADCSCONFIGURED** - ADC's Configured – Asserted when all five ADCs have been configured
	11	**STAT_DACSCONFIGURED** – all DACs have been configured
	12	**STAT_HST_ALL_W_EN_DETECTED** - *hst_all_w_en* detected
	12	**STAT_RSLNALLWENB -** AllWEn enables all shutter signals to initialize storage caps (side B)
	13	**STAT_TIMERCOUNTERRESET** – indicates that the timer (see 0x03C and 0x03D) has been reset
	14	**STAT_ARMED** - 'ADCs configured' AND 'DACs configured' AND **TRIGGER_CTL**[0] & 'HST_Configured' AND NOT 'coarse trigger detected' AND NOT 'fine trigger detected' AND 'PDBIAS is ready'. Note that all these conditions must be met for ARMED to be asserted.
	15	**STAT_RSLNALLWENA -** AllWEn enables all shutter signals to initialize storage caps (side A)
	16	**STAT_HSTCONFIGDONE**– Indicates that HST (and RSL on Daedalus firmware) is configured.
	23:17	**STAT_TEMP** - Temperature Sensor [6:0] from **ADC5_DATA_2**[11:0] (0x096); see Section 8 .
	31:24	**STAT_PRESS** - Pressure Sensor difference [7:0] from the absolute value difference between MON_PRES_MINUS and MON_PRES_PLUS (see 0x095); see Section 9 .

0x030	**STAT_REG2**	V1, V4	Read-only	---
Status Register 2. (Read-only duplicate of **STAT_REG2_SRC**)	31:0	Read-only shadow bits of **STAT_REG2_SRC**. Reading this register has no effect on these bit values. To clear the applicable bits, **STAT_REG2_ SRC** must be read. See 0x031 for bit assignments		

0x031	**STAT_REG2_SRC**	V1, V4	Read-clear	
Status Register 2, Source. Contains the source logic for clearable status bits, whereas **STAT_REG2** contains	0	**FPA_IF_TO** - When this bit is asserted high, a timeout error has occurred during the sensor-to-SRAM readout process		
	1	**SRAM_RO_TO** - When asserted high, this bit indicates that a timeout has occurred while reading an SRAM row.		

read-only copies. All bits in **STAT_REG2_SRC** register will be cleared when the register is read. See Section 14 for additional details. Use register `0x030` to read these bits	2	**PIXELRD_TOUT_ERR** - When asserted high, this bit indicates that the overall sensor readout process has timed out. It also indicates that the internal transmit data pipeline has reverted from selecting Burst Response (i.e., pixel) data back to Response (i.e., status) data to re-establish communications with the host.
	3	**UART_TX_TO_RST** - When asserted high and the RS422 port is enabled, this bit indicates that a timeout has occurred within the RS422 transmit logic, and the UART TX module has reset itself to recover from the condition.
	4	**UART_RX_TO_RST** - When asserted high and the RS422 port is enabled, this bit indicates that a timeout has occurred within the RS422 receive logic, and the UART RX module has reset itself to recover from the condition.
	5	**PDBIAS_UNREADY** – A '1' indicates that the 49 V regulator is providing less than 10 V and therefore is considered 'unready'. When '0', the 49 V regulator is providing at least 10 V and is therefore considered 'ready'

0x032	**ADC_BYTECOUNTER**	V1, V4	Read-only	---
ADC Byte Counter	25:0	*adc_bytecounter.* This is the byteCounter output of the ADC/SRAM readout module which counts the pixels (in bytes) that have been read from the image sensor and written into the SRAM. If this register is read after a system "hang" has been detected (and prior to a reset), it can indicate if the error occurred during sensor readoff. If it contains a value of zero, then the ADC/SRAM readout module has likely operated normally. If it is a non-zero value, then this may indicate that the error was caused by a failure in the ADC/SRAM module, where the value contained is the pixel/byte number that the image capture hung on. Since this counter is an integral part of the FPGA logic (rather than a test-only feature), it can only be cleared with a system reset.			
0x033	**RBP_PIXEL_CNTR**	V1, V4	Read-only	---
Read Burst Processing Pixel Counter	23:0	This is the *pixel_cntr* output of the steering/read_burst_processing module which counts the pixels (in bytes) that have been read from the transmit FIFO after being read from the SRAM. If this register is read after a system "hang" has been detected (and prior to a reset), it can indicate if the error occurred during SRAM readoff, and if the error occurred at the TX FIFO output in the readout pipeline. If it contains a value of zero, then the ADC/SRAM module has likely operated normally, and the error originated elsewhere. If it is a non-zero value, then this may indicate that the error was caused by a failure in the steering/read_burst_processing module, where the value contained is the pixel/byte number that the image capture hung on. Since this counter is an integral part of the FPGA logic (rather than a test-only feature), it can only be cleared with a system reset.			
0x034	**DIAG_MAX_CNT_0**	V1, V4	Read/Write	---

Diagnostic Max Count Register 0	7:0	**MAXERR_SRT** - Maximum number of errors indicated by *sram_ro_to* (see 0x031) before the counter freezes. Maximum value allowed is 0xFF.
	15:8	Unused
	31:16	**MAXERR_FIT** - Maximum number of errors indicated by *uart_tx_to_rst* (see 0x031) before the counter freezes. Maximum value allowed is 0xFFFF.

0x035	**DIAG_MAX_CNT_1**	V1, V4	Read/Write	---

Diagnostic Max Count Register 1	15:0	**MAXERR_URTR** - Maximum number of errors indicated by *uart_rx_to_rst* (see 0x031) before the counter freezes. Maximum value allowed is 0xFFFF.
	31:16	**MAXERR_UTTR** - Maximum number of errors indicated by *fpa_if_to* (see, 0x031) before the counter freezes. Maximum value allowed is 0xFFFF.

0x036	**DIAG_CNTR_VAL_0**	V1, V4	Read-only	---

Diagnostic Counter Value 0	7:0	**SRT_COUNT** - Current value of *sram_ro_to* counter, which increments when *sram_ro_to* is asserted and is reset only with a system reset. Maximum value is 0xFF; when this value is reached, the counter will freeze until reset.
	15:8	Unused
	31:16	**FIT_COUNT** - Current value of *fpa_if_to* counter, which increments when *fpa_if_to* is asserted and is reset only with a system reset. Maximum value is 0xFFFF; when this value is reached, the counter will freeze until reset.

0x037	**DIAG_CNTR_VAL_1**	V1, V4	Read-only	---

Diagnostic Counter Value 1	15:0	**URTR_COUNT** - Current value of uart_rx_to_rst counter, which increments when *uart_rx_to_rst* is asserted and is reset only with a system reset. Maximum value is 0xFFFF; when this value is reached, the counter will freeze until reset.
	31:16	**UTTR_COUNT** - Current value of uart_tx_to_rst counter, which increments when *uart_tx_to_rst* is asserted and is reset only with a system reset. Maximum value is 0xFFFF; when this value is reached, the counter will freeze until reset.

0x038	**STAT_EDGE_DETECTS**	V4	Read-only	---

Status of thirty-one out of the thirty-two Icarus or five out of the six Daedalus edge detect signals based on the rising edge of the FPGA system clock. Sensor must be	0	W0_TOP_B_EDGE1 - Diagnostic One Shot: Rising edge of w0 shutter into top B side of FPA.
	0	SH0_rise_UR – Diagnostic One Shot: Rising edge of shutter 0 into B side of FPA.
	1	W0_TOP_A_EDGE2 - Diagnostic One Shot: Falling edge of w0 shutter into top A side of FPA.
	1	SH0_fall_UR – Diagnostic One Shot: Falling edge of shutter 0 into B side of FPA.

attached to monitor edge detects. Refer to Icarus HDD document and Daedalus V2 HDD document for reference on edge detect signals.[5, 6]

2	W0_TOP_B_EDGE2 - Diagnostic One Shot: Falling Shot: Falling edge of w0 shutter into top B side of FPA.
2	SH1_rise_UR – Diagnostic One Shot: Rising edge of shutter 1 into B side of FPA.
3	W0_BOT_A_EDGE1 - Diagnostic One Shot: Rising edge of w0 shutter into bottom A side of FPA.
3	SH1_fall_UR – Diagnostic One Shot: Falling edge of shutter 1 into B side of FPA.
4	W0_BOT_B_EDGE1 - Diagnostic One Shot: Rising edge of w0 shutter into bottom B side of FPA.
4	SH2_rise_UR – Diagnostic One Shot: Rising edge of shutter 2 into B side of FPA.
5	W0_BOT_A_EDGE2 - Diagnostic One Shot: Falling edge of w0 shutter into bottom A side of FPA.
6	W0_BOT_B_EDGE2 - Diagnostic One Shot: Falling edge of w0 shutter into bottom B side of FPA.
7	W1_TOP_A_EDGE1 - Diagnostic One Shot: Rising edge of w1 shutter into top A side of FPA.
8	W1_TOP_B_EDGE1 - Diagnostic One Shot: Rising edge of w1 shutter into top B side of FPA.
9	W1_TOP_A_EDGE2 - Diagnostic One Shot: Falling edge of w1 shutter into top A side of FPA.
10	W1_TOP_B_EDGE2 - Diagnostic One Shot: Falling edge of w1 shutter into top B side of FPA.
11	W1_BOT_A_EDGE1 - Diagnostic One Shot: Rising edge of w1 shutter into bottom A side of FPA.
12	W1_BOT_B_EDGE1 - Diagnostic One Shot: Rising edge of w1 shutter into bottom B side of FPA.
13	W1_BOT_A_EDGE2 - Diagnostic One Shot: Falling edge of w1 shutter into bottom A side of FPA.
14	W1_BOT_B_EDGE2 - Diagnostic One Shot: Falling edge of w1 shutter into bottom B side of FPA.
15	W2_TOP_A_EDGE1 - Diagnostic One Shot: Rising edge of w2 shutter into top A side of FPA.
16	W2_TOP_B_EDGE1 - Diagnostic One Shot: Rising edge of w2 shutter into top B side of FPA.
17	W2_TOP_A_EDGE2 - Diagnostic One Shot: Falling edge of w2 shutter into top A side of FPA.
18	W2_TOP_B_EDGE2 - Diagnostic One Shot: Falling edge of w2 shutter into top B side of FPA.
19	W2_BOT_A_EDGE1 - Diagnostic One Shot: Rising edge of w2 shutter into bottom A side of FPA.
20	W2_BOT_B_EDGE1 - Diagnostic One Shot: Rising edge of w2 shutter into bottom B side of FPA.
21	W2_BOT_A_EDGE2 - Diagnostic One Shot: Falling edge of w2 shutter into bottom A side of FPA.
22	W2_BOT_B_EDGE2 - Diagnostic One Shot: Falling edge of w2 shutter into bottom B side of FPA.
23	W3_TOP_A_EDGE1 - Diagnostic One Shot: Rising edge of w3 shutter into top A side of FPA.
24	W3_TOP_B_EDGE1 - Diagnostic One Shot: Rising edge of w3 shutter into top B side of FPA.
25	W3_TOP_A_EDGE2 - Diagnostic One Shot: Falling edge of w3 shutter into top A side of FPA.
26	W3_TOP_B_EDGE2 - Diagnostic One Shot: Falling edge of w3 shutter into top B side of FPA.
27	W3_BOT_A_EDGE1 - Diagnostic One Shot: Rising edge of w3 shutter into bottom A side of FPA.
28	W3_BOT_B_EDGE1 - Diagnostic One Shot: Rising edge of w3 shutter into bottom B side of FPA.
29	W3_BOT_A_EDGE2 - Diagnostic One Shot: Falling edge of w3 shutter into bottom A side of FPA.

	30	W3_BOT_B_EDGE2 - Diagnostic One Shot: Rising edge of w3 shutter into bottom B side of FPA.			
0x03A	**TRIGGER_CTL**		V1, V4	Read/Write	0x0000_0000
Trigger control	0	**HW_TRIG_EN** - When '1' with rest of TRIGGER_CTL bits cleared, coarse and fine triggers are passed to internal logic; when '0', triggers are ignored.			
	1	Unused			
	2	**SW_TRIG_EN** - When '1' with rest of **TRIGGER_CTL** bits cleared, asserting **SW_TRIG_START** will cause the FPGA to generate a coarse and fine trigger.			
0x03B	**SRAM_CTL**		V1, V4	Write; self-clearing	0x0000_0000
Request SRAM Readoff	0	**READ_SRAM** - Request SRAM Data when '1'. This bit is self-clearing. When using RS422, software should send no additional command packets after setting this but until all expected burst response data is received.			
0x03C	**TIMER_CTL**		V1, V4	Write; self-clearing	---
Timer control register	0	**RESET_TIMER** - Resets counter when set to '1'. This bit is self-clearing.			
0x03D	**TIMER_VALUE**		V1, V4	Read-only	---
Current value of timer in FPGA clock cycles	23:0	Current timer counter value in FPGA clock cycles. Increments every second			
0x03E	**VRESET_WAIT_TIME**		V1, V4	Read/Write	0x0000_0000
Time to wait for VRESET to ramp high.	30:0	*Icarus1 only*. Time to wait for VRESET to ramp high, in 25 ns increments. This register is used to recover the image in a 2-frame Icarus			
0x03F	**HSTALLWEN_WAIT_TIME**		V1, V4	Read/Write	0x0000_0190
hstAllWEn active time	30:0	Time for *hstAllWEn* to be active, in 25 ns increments during pixel initialization			
0x041	**ICARUS_VER_SEL**		V1, V4	Read/Write	0x0000_0000
Selects ICARUS type, either 4 or 2 frame version	0	0	4-frame 'Icarus2'		
		1	2-frame 'Icarus'		
0x042	**FPA_ROW_INITIAL**		V1, V4	Read/Write	0x0000_0000
The initial pixel row to read off the SRAM	9:0	Initial row, between 0 and 1023 (0x000 – 0x3FF) for Icarus and Daedalus			
0x043	**FPA_ROW_FINAL**		V1, V4	Read/Write	0x0000_03FF
The final pixel row to read off the SRAM	9:0	Final row, between 0 and 1023 (0x000 – 0x3FF) for Icarus and Daedalus. Must be greater than or equal to **FPA_ROW_INITIAL**			

0x044	FPA_FRAME_INITIAL			V1, V4	Read/Write	0x0000_0000
The initial pixel frame to read off the SRAM	1:0	Initial frame, between 0 and 3 for Icarus2, between 1 and 2 for Icarus, between 0 and 2 for Daedalus				
0x045	**FPA_FRAME_FINAL**			V1, V4	Read/Write	0x0000_0003
The final pixel frame to read off the SRAM	1:0	Final frame, between 0 and 3 for Icarus2, between 1 and 2 for Icarus, between 0 and 2 for Daedalus. Must be greater than or equal to **FPA_FRAME_INITIAL**				
0x046	**FPA_DIVCLK_EN_ADDR**			V1, V4	Read/Write	0x0000_0000
Enable the HST *divClk* output	0	0	Disable HST *divClk*			
		1	Enable HST *divClk*			
0x047	**FPA_OSCILLATOR_SEL_ADDR**			V1, V4	Read/Write	0x0000_0000
Select the oscillator for the ROIC.	1:0	**OSC_SELECT** – Select active oscillator:				
		00	Relaxation/500 MHz oscillator			
		01	Ring/100 MHz oscillator			
		10	Ring oscillator (without caps)			
		11	External clock			
0x04A	**VRESET_HIGH_VALUE**			V1, V4	Read/Write	0x0000_0000
Frame 0 and 3 VRESET value	15:0	**VRESET_HIGH** - *Icarus1, Daedalus only*. Determines programmed VRESET value when Frame 0 and 3 shutters are open during the image recovery period for a 2-frame Icarus. Used in conjunction with **VRESET_WAIT_TIME** and **ICARUS_VER_SEL**. Voltage is scaled to 0xFFFF = 3.3 V. Outside of these two frames, Vreset is set according to the to the value of DACH				
0x04B	**FRAME_ORDER_SEL**			V1, V4	Read/Write	0x0000_0000
Reorders the frame readout	2:0	000	Readout frame order (forwards): [0, 1, 2]			
		001	Readout frame order: [2, 0, 1]			
		010	Readout frame order: [1, 2, 0]			
		011	Readout frame order: [0, 2, 1]			
		100	Readout frame order: [1, 0, 2]			
		101	Readout frame order (reverse): [2, 1, 0]			
0x04C	**MISC_SENSOR_CTL**			V1, V4	Read/Write	0x0000_01BE
Miscellaneous sensor control for Icarus	0	**ACCUMULATION_CTL** – If '1', invoke accumulation mode; relevant sensor pins are controlled by bits 1-4 of this register. If '0', those sensor pins are managed by manual shutter control.[5]				

		Accumulation mode with respect to the Icarus sensor is not possible. Accumulation mode is defined as a programmable mode using manual shutters to accumulate integration for each consecutive frame. Therefore, the first frame would be assigned as still the first frame. The second frame would be defined as the sum of the integration of the first frame and the second frame. The third frame would be defined as the sum of the first three frames. The fourth frame would be defined as the sum of all four frames. **Currently not implemented.** Firmware and software is in-place for eventual deprecation.
	1	**HST_TST_ANRST_EN** – Must have bit 0 enabled of this register. If '1', this asserts the High-Speed Timing manual pixel reset enable pin on the A hemisphere of the sensor. If '0', this disables this pin. [5] This is for Accumulation mode. See bit position 0 description for details. **Currently not implemented.**
	2	**HST_TST_BNRST_EN** – Must have bit 0 enabled of this register. If '1', this asserts the High-Speed Timing manual pixel reset enable pin on the B hemisphere of the sensor. If '0', this disables this pin. [5] This is for Accumulation mode. See bit position 0 description for details. **Currently not implemented.**
	3	**HST_TST_ANRST_IN** – Must have bit 0 enabled of this register. If '1', this asserts the High-Speed Timing manual w1 shutter pin on the A hemisphere of the sensor. If '0', this disables this pin. [5] This is for Accumulation mode. See bit position 0 description for details. **Currently not implemented.**
	4	**HST_TST_BNRST_IN** – Must have bit 0 enabled of this register. If '1', this asserts the High-Speed Timing manual w1 shutter pin on the B hemisphere of the sensor. If '0', this disables this pin. [5] This is for Accumulation mode. See bit position 0 description for details. **Currently not implemented.**
	5	**HST_PXL_RST_EN** – If '1', assert the pixel reset transistor enable pin on the sensor. If '0', this disables this pin. [5]
	6	**HST_CONT_MODE** – If '1', enable continuous mode. Shutter timing generation repeats if the oscillator is enabled.[5]
	7	**COL_DCD_EN** – If '1', enable column decode.[5]
	8	**COL_READOUT_EN** – If '1', enable the pad drivers for the analog image channels.[5]

0x04D	**SUSPEND_TIME**		V4	Read/Write	0x0000_0FA0
Duration of Suspend Mode		31:0	Duration of Suspend Mode in increments of 25 ns (see Section 17.1) Default delay is 100 µs.		
0x04E	**FPA_INTERFACE_STATE**		V4	Read-only	--
Testing diagnostic register		20:0	Diagnostic register for developers (not useful for end users). Indicates the one-hot state of the FPA Interface state machine.		
0x04F	**DELAY_READOFF**		V4	Read/Write	0x0000_0000
Duration of readoff delay		31:0	Duration of delay before assertion of RowDecodeEnable in increments of 25 ns.		
0x050	**MANUAL_SHUTTERS_MODE**		V1, V4	Read/Write	0x0000_0000
Manual Shutters Mode select. When bit 0 is set, the FPGA will generate manual shutters signals for the ROIC when the fine trigger is detected. Otherwise, the on-chip High Speed Timing will be used.		0	**MANSHUT_MODE –** If '1', enable manual shutters. If '0', use high-speed timing. See 0x025 for Daedalus manual shutter control		
0x050	**EXT_PHI_CLK_SH0_ON**		V4	Read/Write	0x0000_0000
Manual Shutters image integration time for frame 0 of Daedalus A and B-sides.		29:0	Amount of integration time in 25 ns steps.		
0x051	**W0_INTEGRATION**		V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time for frame 0 of ICARUS A-side.		29:0	Amount of integration time in 25 ns steps.		
0x051	**EXT_PHI_CLK_SH0_OFF**		V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 0 and 1 of Daedalus A and B-sides.		29:0	Amount of integration time in 25 ns steps.		
0x052	**W0_INTERFRAME**		V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 0 and 1 of ICARUS A-side.		29:0	Amount of interframe time in 25 ns steps.		
0x052	**EXT_PHI_CLK_SH1_ON**		V4	Read/Write	0x0000_0000

Manual Shutters image integration time for frame 1 of Daedalus A and B-sides.	29:0	Amount of integration time in 25 ns steps.		
0x053	**W1_INTEGRATION**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time for frame 1 of ICARUS A-side.	29:0	Amount of interframe time in 25 ns steps.		
0x053	**EXT_PHI_CLK_SH1_OFF**	V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 1 and 2 of Daedalus A and B-sides.	29:0	Amount of integration time in 25 ns steps.		
0x054	**W1_INTERFRAME**	V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 1 and 2 of ICARUS A-side.	29:0	Amount of interframe time in 25 ns steps.		
0x054	**EXT_PHI_CLK_SH2_ON**	V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 2 of Daedalus A and B-sides.	29:0	Amount of integration time in 25 ns steps.		
0x055	**W2_INTEGRATION**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 2 of ICARUS A-side.	29:0	Amount of integration time in 25 ns steps.		
0x056	**W2_INTERFRAME**	V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 2 and 3 of ICARUS A-side.	29:0	Amount of interframe time in 25 ns steps.		
0x057	**W3_INTEGRATION**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 3 of ICARUS A-side.	29:0	Amount of integration time in 25 ns steps.		
0x058	**W0_INTEGRATION_B**	V1, V4	Read/Write	0x0000_0000

Manual Shutters image integration time register for frame 0 of ICARUS B-side.	29:0	Amount of integration time in 25 ns steps.		
0x059	**W0_INTERFRAME_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 0 and 1 of ICARUS B-side.	29:0	Amount of interframe time in 25 ns steps.		
0x05A	**W1_INTEGRATION_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 1 of ICARUS B-side.	29:0	Amount of integration time in 25 ns steps.		
0x05B	**W1_INTERFRAME_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 1 and 2 of ICARUS B-side.	29:0	Amount of interframe time in 25 ns steps.		
0x05C	**W2_INTEGRATION_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 2 of ICARUS B-side.	29:0	Amount of integration time in 25 ns steps.		
0x05D	**W2_INTERFRAME_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters interframe time between acquisitions for frames 2 and 3 of ICARUS B-side.	29:0	Amount of interframe time in 25 ns steps.		
0x05E	**W3_INTEGRATION_B**	V1, V4	Read/Write	0x0000_0000
Manual Shutters image integration time register for frame 3 of ICARUS B-side.	29:0	Amount of integration time in 25 ns steps.		
0x05F	**TIME_ROW_DCD**	V4	Read/Write	0x0002_7100
Row Decode Counter	27:0	Set counter for the assertion of ROW_DCD sensor input in 25 ns steps. Default is 40 ms.		
0x090	**ADC_CTL**	V1, V4	Write; Self-clearing	---
Control of TI8548 (LLNLv1) ADCs	0	Configure ADC 1		
	1	Configure ADC 2		
	2	Configure ADC 3		

		3	Configure ADC 4		
0x091	**ADC1_CONFIG_DATA**		V1, V4	Read/Write	0x83A8_81FF
Configuration data to be manage ADC 1		9:0	Internal reference DAC setting (1 LSB = internal Vref / 1024)		
		13	Internal reference voltage (‘0’ = 2.5 V, ‘1’ = 3 V)		
		15	Internal reference enable		
		24:19	Voltage multiplier controls		
0x092	**ADC2_CONFIG_DATA**		V1, V4	Read/Write	0x83A8_81FF
Configuration data to be manage ADC 2		9:0	Internal reference DAC setting (1 LSB = internal Vref / 102a4)		
		13	Internal reference voltage (‘0’ = 2.5 V, ‘1’ = 3 V)		
		15	Internal reference enable		
		24:19	Voltage multiplier controls		
0x093	**ADC3_CONFIG_DATA**		V1, V4	Read/Write	0x83A8_81FF
Configuration data to be manage ADC 3		9:0	Internal reference DAC setting (1 LSB = internal Vref / 1024)		
		13	Internal reference voltage (‘0’ = 2.5 V, ‘1’ = 3 V)		
		15	Internal reference enable		
		24:19	Voltage multiplier controls		
0x094	**ADC4_CONFIG_DATA**		V1, V4	Read/Write	0x83A8_81FF
Configuration data to be manage ADC 4		9:0	Internal reference DAC setting (1 LSB = internal Vref / 1024)		
		13	Internal reference voltage (‘0’ = 2.5 V, ‘1’ = 3 V)		
		15	Internal reference enable		
		24:19	Voltage multiplier controls		
0x095	**ADC5_DATA_1**		V4	Read-only	---
Monitors 1 and 2 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.		11:0	**MON_CH1 / MON_PRES_MINUS**		
		23:12	**MON_CH2 / MON_PRES_PLUS**		
0x096	**ADC5_DATA_2**		V4	Read-only	---

Monitors 3 and 4 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH3 / MON_TEMP**			
	23:12	**MON_CH4 / MON_COL_TOP_IBIAS_IN**			
0x097	**ADC5_DATA_3**		V4	Read-only	---
Monitors 5 and 6 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH5 / MON_HST_OSC_R_BIAS**			
	23:12	**MON_CH6 / MON_VAB / MON_CHG** (DACG)			
0x098	**ADC5_DATA_4**		V4	Read-only	---
Monitors 7 and 8 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH7 / MON_HST_RO_NC_IBIAS, MON_HST_RO_IBIAS / MON_CHE** (DACE) – see register 0x029			
	11:0	**MON_CH7 / MON_HST_OSC_CTL / MON_CHE** (DACE) – see register 0x029			
	23:12	**MON_CH8 / MON_VRST / MON_CHH** (DACH) – see register 0x02A			
0x099	**ADC6_DATA_1**		V4	Read-only	---
Monitors 9 and 10 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH9 / MON_COL_BOT_IBIAS_IN**			
	23:12	**MON_CH10 / MON_HST_A_PDELAY / MON_CHA** (DACA) – see register 0x027			
	23:12	**MON_CH10 / MON_TSENSE_OUT**			
0x09A	**ADC6_DATA_2**		V4	Read-only	---
Monitors 11 and 12 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH11 / MON_HST_B_NDELAY / MON_CHD** (DACD) – see register 0x028			
	11:0	**MON_CH11 / MON_BGREF**			
	23:12	**MON_CH12** (DOSIMETER)			
0x09B	**ADC6_DATA_3**		V4	Read-only	---
Monitors 13 and 14 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH13 / MON_HST_OSC_VREF_IN**			
	11:0	**MON_CH13 / MON_HST_RO_NC_IBIAS**			
	23:12	**MON_CH14 / MON_HST_B_PDELAY / MON_CHC** (DACC) – see register 0x028			
	23:12	**MON_CH14 / MON_HST_OSC_VREF_IN / MON_CHC** (DACC) – see register 0x028			

0x09C	**ADC6_DATA_4**		V4	Read-only	---
Monitors 15 and 16 data. Full scale is 0-5 V. See Section 5.1 for ADC channel description.	11:0	**MON_CH15 / MON_HST_OSC_CTL / MON_CHF** (DACF) – see register 0x029			
	11:0	**MON_CH15 / MON_COL_TST_IN / MON_CHF** (DACF) – see register 0x029			
	23:12	**MON_CH16 / MON_HST_A_NDELAY / MON_CHB** (DACB) – see register 0x027			
	23:12	**MON_CH16 / MON_HST_OSC_PBIAS_PAD**			
0x09D	**ADC_PPER**		V4	Read/Write	0x000_0064
Polling period for ADC 5 and 6 in milliseconds	27:0	ADC monitor (5 and 6) polling period. Default is 100 ms → 0x64			
0x09E	**ADC_RESET**		V1, V4	Read/Write	0x0000_001F
Controls reset pins to ADC 1 through 4	0	ADC1 standby / reset			
	1	ADC2 standby / reset			
	2	ADC3 standby / reset			
	3	ADC4 standby / reset			
0x120	**HST_TRIGGER_DELAY_DATA_LO**		V1, V4	Read/Write	0x0000_0000
High-speed timing trigger delay, LSBs	31:0	Delay timing pattern [31:0] (each bit represents 150 ps)			
0x121	**HST_TRIGGER_DELAY_DATA_HI**		V1, V4	Read/Write	0x0000_0000
High-speed timing trigger delay, MSBs	7:0	Delay timing pattern [39:32] (each bit represents 150 ps)			
0x122	**HST_PHI_DELAY_DATA**		V1, V4	Read/Write	0x0000_0000
Phi clock delay, LSBs	9:0	**PHI_DELAY_B** - delay timing pattern (each bit represents 150 ps)			
	29:20	**PHI_DELAY_A** - delay timing pattern (each bit represents 150 ps)			
0x129	**HST_EXT_PHI_CLK_HALF_PER**		V4	Read/Write	0x0000_0000
Delay counter for external clock controlled by FPGA.	31:0	Delay count in increments of 50 ns			
0x130	**HST_COUNT_TRIG**		V4	Read/Write	0x0000_0000
Initiate HST generator	0	Initiate HST generator. When asserted, the HST_DIV_CLK is halted[6]			
0x131	**HST_DELAY_EN**		V1, V4	Read/Write	0x0000_0000
Enable trigger delay cell for HST generator	0	Enable trigger delay cell for HST generator[6]			

0x133	**RSL_HFW_MODE_EN**		V1, V4	Read/Write	0x0000_0000
Enable High Full Well mode	0	**HFW** – '1' enables HFW mode			
0x135	**RSL_ZDT_MODE_B_EN**		V1, V4	Read/Write	0x0000_0000
Enable Zero Dead Time mode for B hemisphere	0	**ZDT_B** – '1' enables ZDT mode for B hemisphere			
0x136	**RSL_ZDT_MODE_A_EN**		V1, V4	Read/Write	0x0000_0000
Enable Zero Dead Time mode for A hemisphere	0	**ZDT_A** – '1' enables ZDT mode for A hemisphere			
0x137	**BGTRIMA**		V1, V4	Read/Write	0x0000_0000
Drives the BGTRIMA input pins to the Daedalus sensor	2:0	BGTRIMA (Bandgap digital trim bit A) pins to the sensor			
0x138	**BGTRIMB**		V1, V4	Read/Write	0x0000_0000
Drives the BGTRIMB input pins to the Daedalus sensor	3:0	BGTRIMB (Bandgap digital trim bit B) pins to the sensor			
0x139	**COLUMN_TEST_EN**		V1, V4	Read/Write	0x0000_0000
Column Test Enable bit	0	Drives the ColTstEn pin to the sensor (named col_test_en_o in the FPGA), which controls the global column current source test mode. When '1', the following occurs: 1. The sensor's test source followers are enabled on each column current source. 2. The sensor's RDcdEn pin (named RowDcdEn_o in the FPGA) is driven low by the FPGA to disable it 3. The sensor's nQuenchEn pin (named quench_en_n_o in the FPGA) is driven high by the FPGA to disable it 4. The user can then use VRST to drive an analog voltage to the sensor's ColTstIn pin, since VRST is connected to ColTstIn. When '0', the sensor and FPGA operate in normal mode			
0x140	**RSL_CONFIG_DATA_B0**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[31:0] for the RSL interlacing shift register input (side B) to the sensor			
0x141	**RSL_CONFIG_DATA_B1**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[63:32] for the RSL interlacing shift register input (side B) to the sensor			
0x142	**RSL_CONFIG_DATA_B2**		V1, V4	Read/Write	0x0000_0000

RSLScanInB input to the sensor	31:0	Data[95:64] for the RSL interlacing shift register input (side B) to the sensor			
0x143	**RSL_CONFIG_DATA_B3**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[127:96] for the RSL interlacing shift register input (side B) to the sensor			
0x144	**RSL_CONFIG_DATA_B4**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[159:128] for the RSL interlacing shift register input (side B) to the sensor			
0x145	**RSL_CONFIG_DATA_B5**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[191:160] for the RSL interlacing shift register input (side B) to the sensor			
0x146	**RSL_CONFIG_DATA_B6**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[223:192] for the RSL interlacing shift register input (side B) to the sensor			
0x147	**RSL_CONFIG_DATA_B7**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[255:224] for the RSL interlacing shift register input (side B) to the sensor			
0x148	**RSL_CONFIG_DATA_B8**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[287:256] for the RSL interlacing shift register input (side B) to the sensor			
0x149	**RSL_CONFIG_DATA_B9**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[319:288] for the RSL interlacing shift register input (side B) to the sensor			
0x14A	**RSL_CONFIG_DATA_B10**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[351:320] for the RSL interlacing shift register input (side B) to the sensor			
0x14B	**RSL_CONFIG_DATA_B11**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[383:352] for the RSL interlacing shift register input (side B) to the sensor			
0x14C	**RSL_CONFIG_DATA_B12**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[415:384] for the RSL interlacing shift register input (side B) to the sensor			
0x14D	**RSL_CONFIG_DATA_B13**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[447:416] for the RSL interlacing shift register input (side B) to the sensor			
0x14E	**RSL_CONFIG_DATA_B14**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[479:448] for the RSL interlacing shift register input (side B) to the sensor			
0x14F	**RSL_CONFIG_DATA_B15**		V1, V4	Read/Write	0x0000_0000

RSLScanInB input to the sensor	31:0	Data[511:480] for the RSL interlacing shift register input (side B) to the sensor			
0x150	**RSL_CONFIG_DATA_B16**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[543:512] for the RSL interlacing shift register input (side B) to the sensor			
0x151	**RSL_CONFIG_DATA_B17**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[575:544] for the RSL interlacing shift register input (side B) to the sensor			
0x152	**RSL_CONFIG_DATA_B18**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[607:576] for the RSL interlacing shift register input (side B) to the sensor			
0x153	**RSL_CONFIG_DATA_B19**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[639:608] for the RSL interlacing shift register input (side B) to the sensor			
0x154	**RSL_CONFIG_DATA_B20**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[671:640] for the RSL interlacing shift register input (side B) to the sensor			
0x155	**RSL_CONFIG_DATA_B21**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[703:672] for the RSL interlacing shift register input (side B) to the sensor			
0x156	**RSL_CONFIG_DATA_B22**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[735:704] for the RSL interlacing shift register input (side B) to the sensor			
0x157	**RSL_CONFIG_DATA_B23**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[767:736] for the RSL interlacing shift register input (side B) to the sensor			
0x158	**RSL_CONFIG_DATA_B24**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[799:768] for the RSL interlacing shift register input (side B) to the sensor			
0x159	**RSL_CONFIG_DATA_B25**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[831:800] for the RSL interlacing shift register input (side B) to the sensor			
0x15A	**RSL_CONFIG_DATA_B26**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[863:832] for the RSL interlacing shift register input (side B) to the sensor			
0x15B	**RSL_CONFIG_DATA_B27**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[895:864] for the RSL interlacing shift register input (side B) to the sensor			
0x15C	**RSL_CONFIG_DATA_B28**		V1, V4	Read/Write	0x0000_0000

RSLScanInB input to the sensor	31:0	Data[927:896] for the RSL interlacing shift register input (side B) to the sensor			
0x15D	**RSL_CONFIG_DATA_B29**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[959:928] for the RSL interlacing shift register input (side B) to the sensor			
0x15E	**RSL_CONFIG_DATA_B30**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[991:960] for the RSL interlacing shift register input (side B) to the sensor			
0x15F	**RSL_CONFIG_DATA_B31**		V1, V4	Read/Write	0x0000_0000
RSLScanInB input to the sensor	31:0	Data[1023:992] for the RSL interlacing shift register input (side B) to the sensor			
0x160	**RSL_CONFIG_DATA_A0**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[31:0] for the RSL interlacing shift register input (side A) to the sensor			
0x161	**RSL_CONFIG_DATA_A1**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[63:32] for the RSL interlacing shift register input (side A) to the sensor			
0x162	**RSL_CONFIG_DATA_A2**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[95:64] for the RSL interlacing shift register input (side A) to the sensor			
0x163	**RSL_CONFIG_DATA_A3**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[127:96] for the RSL interlacing shift register input (side A) to the sensor			
0x164	**RSL_CONFIG_DATA_A4**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[159:128] for the RSL interlacing shift register input (side A) to the sensor			
0x165	**RSL_CONFIG_DATA_A5**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[191:160] for the RSL interlacing shift register input (side A) to the sensor			
0x166	**RSL_CONFIG_DATA_A6**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[223:192] for the RSL interlacing shift register input (side A) to the sensor			
0x167	**RSL_CONFIG_DATA_A7**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[255:224] for the RSL interlacing shift register input (side A) to the sensor			
0x168	**RSL_CONFIG_DATA_A8**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[287:256] for the RSL interlacing shift register input (side A) to the sensor			
0x169	**RSL_CONFIG_DATA_A9**		V1, V4	Read/Write	0x0000_0000

RSLScanInA input to the sensor	31:0	Data[319:288] for the RSL interlacing shift register input (side A) to the sensor			
0x16A	**RSL_CONFIG_DATA_A10**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[351:320] for the RSL interlacing shift register input (side A) to the sensor			
0x16B	**RSL_CONFIG_DATA_A11**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[383:352] for the RSL interlacing shift register input (side A) to the sensor			
0x16C	**RSL_CONFIG_DATA_A12**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[415:384] for the RSL interlacing shift register input (side A) to the sensor			
0x16D	**RSL_CONFIG_DATA_A13**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[447:416] for the RSL interlacing shift register input (side A) to the sensor			
0x16E	**RSL_CONFIG_DATA_A14**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[479:448] for the RSL interlacing shift register input (side A) to the sensor			
0x16F	**RSL_CONFIG_DATA_A15**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[511:480] for the RSL interlacing shift register input (side A) to the sensor			
0x170	**RSL_CONFIG_DATA_A16**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[543:512] for the RSL interlacing shift register input (side A) to the sensor			
0x171	**RSL_CONFIG_DATA_A17**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[575:544] for the RSL interlacing shift register input (side A) to the sensor			
0x172	**RSL_CONFIG_DATA_A18**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[607:576] for the RSL interlacing shift register input (side A) to the sensor			
0x173	**RSL_CONFIG_DATA_A19**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[639:608] for the RSL interlacing shift register input (side A) to the sensor			
0x174	**RSL_CONFIG_DATA_A20**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[671:640] for the RSL interlacing shift register input (side A) to the sensor			
0x175	**RSL_CONFIG_DATA_A21**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[703:672] for the RSL interlacing shift register input (side A) to the sensor			
0x176	**RSL_CONFIG_DATA_A22**		V1, V4	Read/Write	0x0000_0000

RSLScanInA input to the sensor	31:0	Data[735:704] for the RSL interlacing shift register input (side A) to the sensor			
0x177	**RSL_CONFIG_DATA_A23**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[767:736] for the RSL interlacing shift register input (side A) to the sensor			
0x178	**RSL_CONFIG_DATA_A24**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[799:768] for the RSL interlacing shift register input (side A) to the sensor			
0x179	**RSL_CONFIG_DATA_A25**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[831:800] for the RSL interlacing shift register input (side A) to the sensor			
0x17A	**RSL_CONFIG_DATA_A26**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[863:832] for the RSL interlacing shift register input (side A) to the sensor			
0x17B	**RSL_CONFIG_DATA_A27**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[895:864] for the RSL interlacing shift register input (side A) to the sensor			
0x17C	**RSL_CONFIG_DATA_A28**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[927:896] for the RSL interlacing shift register input (side A) to the sensor			
0x17D	**RSL_CONFIG_DATA_A29**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[959:928] for the RSL interlacing shift register input (side A) to the sensor			
0x17E	**RSL_CONFIG_DATA_A30**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[991:960] for the RSL interlacing shift register input (side A) to the sensor			
0x17F	**RSL_CONFIG_DATA_A31**		V1, V4	Read/Write	0x0000_0000
RSLScanInA input to the sensor	31:0	Data[1023:992] for the RSL interlacing shift register input (side A) to the sensor			

14 Error Recovery and Diagnostics

Numerous design and development techniques have been utilized in the NSGCC FPGA to ensure that it operates as reliably as possible; however, due to the harsh operational environment that the system is targeted for, logic failures are unavoidable and will occur. In this case, the FPGA's error recovery and diagnostic features become critical, enabling the FPGA to recover from an error and allowing the user to diagnose the root cause so that corrections can be made. These features include

- Status registers, counters, and timers in various parts of the sensor and SRAM readout pipelines to detect when logic modules and state machines have "hung" and to assist in determining the root causes
- Automatic resets in the RS422 logic section, which ensure that communications can be re-established in case of an error in the RS422 modules
- A software reset to enable the user to return the board to its default configuration when desired.

The following sub-sections describe the implemented error recovery and diagnostic features.

14.1 Software Reset

A software reset has been implemented which resets all logic within the FPGA. To activate the software reset, write a '1' to the **RESET** subregister. This bit will self-clear after being written. Note that all internal FPGA logic will be reset to their default values, including the control registers.

14.2 Automatic Resets on RS422 Transmit and Receive

To ensure that serial communications are maintained in the event of Single Event Upsets in the RS422 logic, automatic resets in both the RS422 transmit and receive sections have been implemented. In the event of a detected "hang" in the RS422 logic, all modules related to reception of command packets and transmission of response packets are reset automatically. The modules which are reset are the RS422, Steering, and Packet Encode/Decode modules. Note that a "hang" condition is determined when an operation takes much longer than under normal operation.

The RS422 transmit module (which generates response packets to the host) is determined to be hung when a byte transfer takes 1 ms, which is much longer than is expected under normal conditions. The RS422 receive module (where the FPGA receives a command packet) is determined to be hung when a byte transfer takes longer than 100 ms (to account for host system performance).

When a "hang" in either the transmit or receive RS422 sections is detected, the appropriate bits in the **STAT_REG2_SRC** and **STAT_REG2** registers are asserted.

14.3 ADC to SRAM module Timeout

A counter exists in the ADC to SRAM module which can be useful in determining the root cause of errors which occur during image sensor read off. This will count the number of pixels (in bytes) that have been read out from the sensor and written into the SRAMs. During normal operation, this counter will count to the final pixel/byte and reset itself to zero. In the event of an FPGA hang, the value held by this counter could be helpful in diagnosing a fault. If an error or FPGA hang occurs, and RS422 communications have

been maintained, a non-zero value in this counter indicates that the error occurred during image sensor readout, while the value indicates the last pixel that was read out successfully. If the counter contains a value of zero, then the root cause of the error likely resides elsewhere.

The host can access the read-only status register **ADC_BYTECOUNTER**. Note that this register cannot be cleared by software; to clear the register, the counter itself must be cleared by returning the ADC-to-SRAM module to its default state (which may require resetting the FPGA).

14.4 FPA Interface Module Timeout

Additional indicators of an error occurring during image sensor readoff reside in the FPA Interface Module, which controls image sensor timing during image-readoff.

To control sensor readoff, the FPA Interface module sends control signals to the ADC to SRAM module. Two of the more useful ones for error detection are *adcReadWriteStart* (which initiates an 8-channel ADC read) and *readOffDone* (which indicates that all desired frames/pixels have been read out from the sensor). To determine if the state machine in this module has hung, the time between these signals is monitored. Since the time between *adcReadWriteStart* pulses is normally 2.875 µs, and the time between the last *adcReadWriteStart* pulse and *readOffDone* is 925 ns, a counter has been implemented that will assert an error bit if the time for either of these events exceeds 2 × 2.875 µs, or 5.75 µs. This error bit is called *fpa_if_to*, and it resides in the **STAT_REG2** and **STAT_REG2_SRC** registers.

14.5 SRAM Readoff Module Timeout

To assist in detecting the root cause of errors occurring during SRAM readoff, a diagnostic counter has been implemented to monitor timing in the SRAM Readoff Row module which controls SRAM readoff on a per-row basis.

To determine an error in this module, the signal *dataOutEn_n* is monitored. This signal is low during the time when row data is being read from the SRAM; in between rows, it goes high for a small number of clock cycles. If *dataOutEn_n* has been monitored as low for an abnormally long period of time, an error bit is asserted (this is the *sram_ro_to* bit in the **STAT_REG2** and **STAT_REG2_SRC** registers).

During normal operation, *dataOutEn_n* is low for 12.8 µs; the error bit is not asserted unless the signal has been low for 25.6 µs.

14.6 Read Burst Processing Module Timeouts

A timeout counter has been implemented to determine the overall length of time that it takes for the entire image sensor readoff and SRAM readout processes to occur. If the length of time has been found to be much longer than normal, then the logic decides that an error has occurred, and two operations occur: (1) control of the transmit data pipeline within the FPGA reverts from Burst Response (i.e., pixel) data back to Response (i.e., status) data to re-enable communications with the host, and (2) the *pixelrd_timeout_err* bit in the **STAT_REG2** and **STAT_REG2_SRC** registers is asserted.

14.7 Resets

Due to the complexity of the radiation tolerant version of the FPGA, numerous resets are generated and used for different purposes. Table 10 lists all the resets used within the device, their modules of origin, purpose, and the logic they affect.

Reset signal	Driver (origin) module	Purpose	Connected modules
sys_rst_n_i	N/A - PCB reset	System reset	clocks_and_resets.vhd (used as input to other reset signals, then distributed to appropriate logic)
sw_rst	Ctl_and_status_ regs.vhd	Software-controlled system reset	clocks_and_resets.vhd (used as input to other reset signals, then distributed to appropriate logic)
cns_reg_rst	Clocks_and_ resets	Reset signal dedicated to resetting the control and status module. Is not asserted under any condition except by sys_rst_n_i. Preserves register state in case any other reset occurs.	ctl_and_status_regs.vhd
sys_rst / sysrst	Clocks_and_ resets	Asserted when sys_rst_n_i or sw_rst are asserted	timer_counter.vhd rs422.vhd dummy_adc_rd.vhd
seu_rec_rst	Seu_recovery .vhd	Asserted if fpa interface times out due to SEU occur	Connected to seu_sys_rst_bl, shot_sys_rst, and shot_sys_rst_bl signals
seu_sys_rst_bl	Nsgcc_top.vhd	OR function of *sys_rst* and *seu_rec_rst*. Used specifically to reset logic in fpa_interface.vhd that does NOT need to be held in a particular state during the shot.	fpa_interface.vhd – used to reset all logic (and sub-modules) except for the state machine and related logic.
rt_shot_hold	Clocks_and_ resets.vhd	Hold rad-susceptible logic in reset for 20us following fine trigger	fpa_interface.vhd – holds state machine in WAIT_FOR_FINE_ TRIG state for 20us following fine trigger. If an SEU occurs that corrupts the state machine, it will transition back to WAIT_FOR_FINE_TRIG
shot_sys_rst	Nsgcc_top.vhd	OR function of sys_rst, rt_shot_hold, and seu_rec_rst	sw_trigger_ctl.vhd
shot_sys_rst_bl	Nsgcc_top.vhd	Boolean version of shot_sys_rst	sram_readoff_top.vhd adc_to_sram_read_control
timeout_rec_rst	Rs422_top.vhd	Asserted when timeouts occur during an rs422 RX or TX transaction.	Connected to *shot_comms_rst* signal
shot_comms_rst	Nsgcc_top.vhd	OR function of *timeout_rec_rst* and *shot_sys_rst*. Resets affected modules if an rs422 timeout occurs	steering.vhd packet_enc_dec.vhd

Table 10: Device Resets

15 Icarus implementation

Information regarding the Icarus sensor interface can be found in the UXI ICARUS – Focal Plane Array Interface Document.

15.1 ADC Interface and Control

The FPGA controls the six analog-to-digital converters (ADCs) on the board. Four of the ADCs are used to convert the image sensor's analog pixel information into 16-bit digital data, while the fifth and sixth are used to monitor DAC channel voltages and specific sensor pin voltages. The four ADCs used to convert the image sensor's analog pixel information to digital data are Texas Instruments 'ADS8568SPM's, which are eight-channel 16-bit devices. Since the Icarus sensor is a 32-channel device, four of these 8-channel devices (numbered ADC1 through ADC4) are required to read out all sensor channels simultaneously. The sensor quadrant and column number connectivity to ADC device number/channel number is shown in Table 11. The two ADCs used for ADC monitoring are Texas Instruments 'ADC128S102's, which are eight-channel 12-bit devices.

Sensor Quadrant	Sensor Column	ADC Device	ADC Channel
Top Left (A)	0-31	4	2
Top Left (A)	32-63	4	3
Top Left (A)	64-95	3	6
Top Left (A)	96-127	3	5
Top Left (A)	128-159	4	0
Top Left (A)	160-191	4	1
Top Left (A)	192-223	4	5
Top Left (A)	224-255	3	1
Top Right (B)	256-287	3	4
Top Right (B)	288-319	3	7
Top Right (B)	320-351	4	4
Top Right (B)	352-383	4	6
Top Right (B)	384-415	4	7
Top Right (B)	416-447	3	0
Top Right (B)	448-479	3	2
Top Right (B)	480-511	3	3
Bottom Left (A)	0-31	2	6
Bottom Left (A)	32-63	2	0
Bottom Left (A)	64-95	2	2
Bottom Left (A)	96-127	2	1
Bottom Left (A)	128-159	2	3
Bottom Left (A)	160-191	2	7
Bottom Left (A)	192-223	2	4
Bottom Left (A)	224-255	1	4
Bottom Right (B)	256-287	1	6
Bottom Right (B)	288-319	1	5
Bottom Right (B)	320-351	1	7
Bottom Right (B)	352-383	1	3
Bottom Right (B)	384-415	1	2
Bottom Right (B)	416-447	1	1
Bottom Right (B)	448-479	1	0
Bottom Right (B)	480-511	2	5

Table 11: Icarus Sensor Channel to ADC Device/Channel Connectivity

15.2 ADC and monitor assignments

The Icarus-configured board ADC, DAC, and monitor assignments are shown in Table **12**.

DAC	Monitor Channel	ADC: Pin	Function	Description	Sens. Pin	Nominal Voltage (V)
A	**MON_HST_A_ PDELAY**	6:5	*HST_A_PDELAY*	Delay voltage for A side pixel array. Increase to add delay.	78	0
B	**MON_HST_A_NDELAY**	6:11	*HST_A_NDELAY*	Delay voltage for A side pixel array. Decrease to add delay.	70	3.3
C	**MON_HST_B_PDELAY**	6:9	*HST_B_PDELAY*	Delay voltage for B side pixel array. Increase to add delay.	94	0
D	**MON_HST_B_NDELAY**	6:6	*HST_B_NDELAY*	Delay voltage for B side pixel array. Decrease to add delay.	86	3.3
E	**MON_HST_RO_IBIAS / MON_HST_RO_NC_ IBIAS**	5:10	*HST_RO_IBIAS/ HST_RO_NC_ IBIAS*	Ring oscillator with capacitors bias control voltage.	46	2.5
F	**MON_HST_OSC_CTL**	6:10	*HST_OSC_CTL*	Relaxation oscillator bias control voltage.	48	1.45
G	**MON_VAB**	5:9	*VAB*	Gate voltage of all anti-bloom transistors in the ICARUS pixel array.	28	0.5
H	**MON_VRST**	5:11	*VRST*	Resets the voltage for all pixels.	61, 69, 77	0.3
---	**MON_PRES_MINUS**	5:4	---	Mems pressure sensor, negative output pin (see Section 9)	---	---
---	**MON_PRES_PLUS**	5:5	---	Mems pressure sensor, positive output pin (see Section 9)	---	
---	**MON_TEMP**	5:6	---	Temperature transducer voltage (see Section 8)	---	---
---	**MON_COL_TOP_ IBIAS_IN**	5:7	---	Column bias for top hemisphere of ICARUS sensor.	8	High Z
---	**MON_HST_OSC_ R_BIAS**	5:8	---	Current sink set for ring oscillator with capacitors.	16	High Z
---	**MON_COL_BOT_ IBIAS_IN**	6:4	---	Column bias for bottom hemisphere of ICARUS sensor.	153	High Z
---	**DOSIMETER**	6:7	---	Voltage of dosimeter	---	---
---	**MON_HST_OSC_ VREF_IN**	6:8	---	Oscillator voltage reference, biased by a voltage divider to a specific voltage of 2.9 V.	87	2.9

Table 12. ICARUS DAC and Monitor Assignments
(see the 'UXI_Icarus_FPA' document for more details[5])

15.3 Anti-Bloom Circuit Control

Each Icarus pixel contains an anti-bloom transistor that is designed to shunt photocurrents greater than full-well, which protects the pixel circuitry from large photo diode signal fluctuations. The gate voltage of the transistor controls the V_{DS} at which the transistor starts conducting current; the VAB pin on the ICARUS sensor is connected to the gate of the anti-bloom transistors and enables the user to apply a voltage to it. On the Version 4.0 Board, VAB is controlled by the **VAB** subregister (set using **DACG**).[5]

15.4 High-Speed Timing (HST) Control

The High-Speed Timing Control function is discussed in detail in the *UXI ICARUS – Focal Plane Array Interface Document,* so this document will not repeat the information contained in that interface document.[5] However, some important things to note regarding this FPGA's implementation of the HST programming sequences are:

1. High Speed Timing must be configured prior to initiating the programming sequence using the **HS_TIMING_DATA_ALO**, **HS_TIMING_DATA_AHI**, **HS_TIMING_DATA_BLO**, and **HS_TIMING_DATA_BHI** registers. These four registers define the 80 bits of A and B side timing described in Figure 6 through 12 of the *UXI ICARUS – Focal Plane Array Interface Document.*
2. The HST programming sequence is initiated when the FPGA detects the rising edge of the Coarse Trigger. The programming sequence is also initiated when the Power-On Image Reset Mode is implemented (Section 10.4).

15.5 Manual Shutter Control

The user can override the HST function of the Icarus sensor and utilize a Manual Shutter Control function instead. Although the timing granularity is coarse compared with the HST mechanism (25 ns vs 1 ns), the user can set integration for each of the frames and/or interframe times between 25 ns and 26.8 seconds, shown in Figure 3. Since the FPGA exhibits instability in a programmed integration and interframe time close to 25 ns, the Nyquist rate becomes an issue; thus, the software limits the user from inputting integration times shorter than 75 ns. This ensures stable programmed integration and/or interframe time. Manual Shutter Control is discussed in detail in the *UXI ICARUS – Focal Plane Array Interface Document,* so this document will not repeat the information contained there. Note: the use of the HST_DIV_CLK monitor is not needed here as the FPGA controls the timing of each integration and interframe time. Manual timing can be set independently for the two hemispheres. Refer to the Jupyter notebook *nsCameraTutorial.ipynb* located in the nsCamera software package docs directory for a demonstration of the use of manual shutters.

Some things to note when using the Manual Shutter Control function of the Icarus sensor:

1. To configure the FPGA and sensor for Manual Shutter control, write a '1' to the **MANSHUT_MODE** subregister.
2. The **W*X*_INTEGRATION** and **W*Y*_INTERFRAME** (X ∈ {0,1,2,3}, Y ∈ {0,1,2}) registers must be programmed to define the timing in 25 ns steps.

3. After the registers are set up properly, the timing sequence in Figure 3 is initiated when the FPGA detects the rising edge of the Fine Trigger.

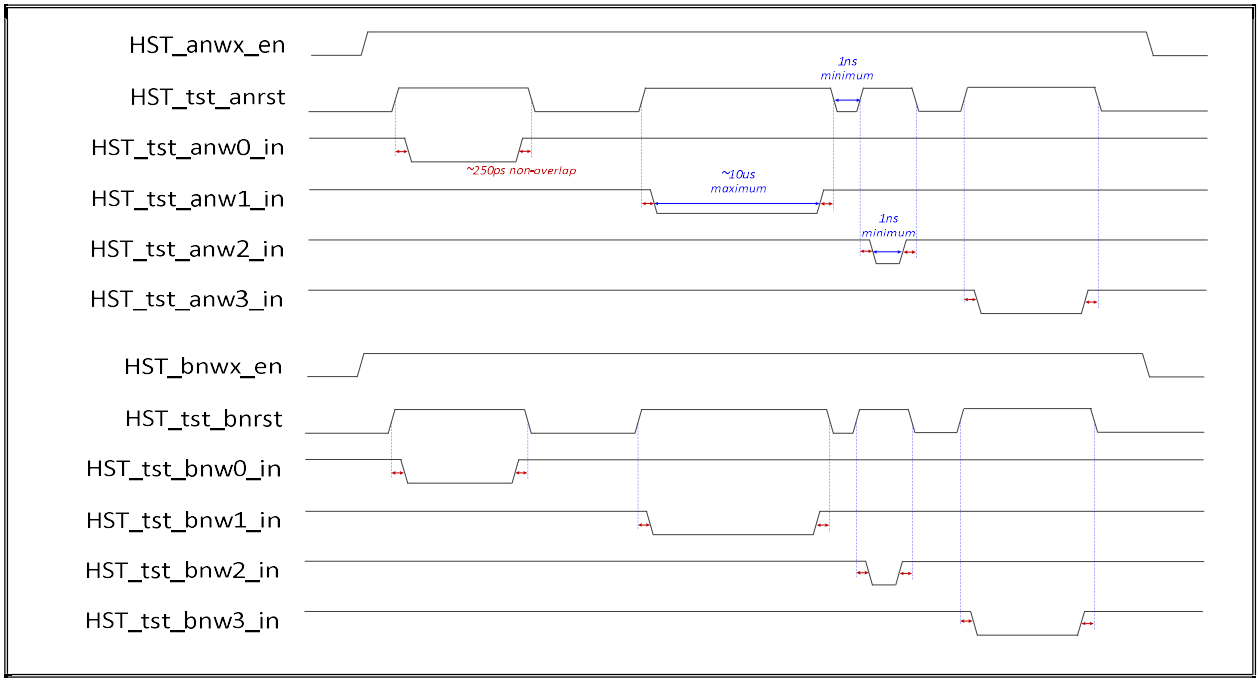

Figure 3. Manual Shutter Timing, Icarus Sensor (A and B sides are here set to the same timing)

15.6 Power Save Mode

Power Save Mode is enabled by asserting bit 3 of the **CTRL_REG** register. When asserted, sensor power saving is achieved by controlling the Icarus sensor's *hst_osc_bias_en* signal. During power save mode, *hst_osc_bias_en* is asserted when the coarse trigger is detected; it is de-asserted once the sensor readout is complete. The effects of the power save mode on LLNL V4 board operation has not been measured.

In addition, internally to the FPGA, power is saved by asserting *hst_data_nRst* for one clock cycle after readoff of image data from FPA to SRAM is complete. This resets the sensor, reducing the current sourced to the board.

16 Daedalus Implementation

Information regarding the Daedalus sensor interface can be found in the *Daedalus HDD-v2.docx*. The current sensor version is version 2 (DV2). The two features that are not implemented in this software 2.1.2 release are the internal temperature sensor (TsenseOut) and the use of the corner diode. The internal temperature sensor requires a transfer function to convert the voltage to temperature units. The 'corner diode' is a standalone component located on the hCMOS sensor composed of a 10x10 array of the same type of diodes used in the pixel array. The purpose of the corner diode is to generate a direct current response to absorbed radiation to provide a time history of the radiation flux seen by the main pixel array to help with troubleshooting, timing, and alignment.[6]

16.1 ADC Interface and Control

The reader should look to Section 15.1 for details of the image-readoff ADC. Table 13 shows the Daedalus sensor channel to ADC connectivity. Note, two out of the four image-readoff ADCs used for the Icarus sensor are also used for the Daedalus sensor, specifically ADCs 3 and 4.

Sensor Hemisphere	Sensor Column	ADC Device	ADC Channel
Left (A)	0-31	4	2
Left (A)	32-63	4	3
Left (A)	64-95	3	6
Left (A)	96-127	3	5
Left (A)	128-159	4	0
Left (A)	160-191	4	1
Left (A)	192-223	4	5
Left (A)	224-255	3	1
Right (B)	256-287	3	4
Right (B)	288-319	3	7
Right (B)	320-351	4	4
Right (B)	352-383	4	6
Right (B)	384-415	4	7
Right (B)	416-447	3	0
Right (B)	448-479	3	2
Right (B)	480-511	3	3

Table 13: Daedalus Sensor Channel to ADC Device/Channel Connectivity

16.2 DAC and monitor assignments

The Daedalus-configured board DAC, and monitor assignments are shown in Table **14**.

DAC	Monitor Channel	ADC: Pin	Function	Description	Sensor Pin	Nominal Voltage (V)
C	**MON_HST_OSC_ VREF_IN**	ADC6: 9	*HST_OSC_ VREF_IN*	Oscillator voltage reference.	94	1.0
E	**MON_HST_ OSC_CTL**	ADC5: 10	*HST_OSC_CTL*	Relaxation oscillator bias control voltage.	46	1.0
F	**MON_COL_ TST_IN**	ADC6: 10	*colTstIn*	Global column current source test pin.	48	0
G	**MON_VAB**	ADC5: 9	*VAB*	Gate voltage of all anti-bloom transistors in the pixel array.	28	1.0
H	**MON_VRST**	ADC5: 11	*VRST*	Resets the voltage for all pixels.	29, 45, 61, 69, 77	0.3
---	**MON_PRES_ MINUS**	ADC5: 4	---	Mems pressure sensor, negative output pin (see Section 9)	---	---
---	**MON_PRES_ PLUS**	ADC5: 5	---	Mems pressure sensor, positive output pin (see Section 9)	---	---
---	**MON_TEMP**	ADC5: 6	---	Temperature transducer voltage (see Section 8)	---	---
---	**MON_TSENSE_ OUT**	ADC6: 5	*TSenseOut*	Monitor the temperature of the Daedalus sensor.	78	---
---	**MON_BGREF**	ADC6: 6	---	Bandgap voltage reference.	86	1.0
---	**DOSIMETER**	ADC6: 7	---	Voltage of dosimeter	---	---
---	**MON_HST_RO_ NC_IBIAS**	ADC6: 8	HST_RO_NC_ IBIAS	Ring oscillator biased by a voltage divider to a specific voltage of ~1.0 V	87	1.0
---	**MON_HST_OSC_ PBIAS_PAD**	ADC6: 11	HST_OSC_ PBIAS_PAD	Current mirror node for oscillator bias	70	2.0

Table 14: Daedalus DAC and Monitor Assignments; see the 'Daedalus HDD-v2" document for more details[7]

16.3 Anti-Bloom Circuit Control

See Section 15.3 (Daedalus and Icarus behaviors are identical).

16.4 High-Speed Timing (HST) Control

See Section 15.4 (Daedalus and Icarus behaviors are identical). Daedalus HST control is also referred to as HST Phi Clock Programming.

16.5 Trigger Delay

Trigger Delay is implemented as described in the *Daedalus HDD-v2.docx* document. It is a user-defined delay between the Fine Trigger and the start time of the selected oscillator; in effect, it is a delay between the Fine Trigger and the opening of Frame 0. The registers **HST_TRIGGER_DELAY_DATA_LO** and **HST_**

TRIGGER_DELAY_DATA_HI are used to program a 40-bit shift register representing a delay of around 150 ps for each bit, up to a maximum delay of about 6 ns. (Experimentally, the maximum trigger delay is 5.7 ns.) Trigger delay is enabled by writing a '1' to the **HST_DEL_EN** subregister.

16.6 HST Phi Clock Delay Programming

The phi clock signals generated in the High-Speed Timing generation logic can be delayed independently by programming a register (Phi Clock Delay) that controls the enable of digital delay elements in the propagation path of the A and B side phi clocks. [6] This delay can be measured between the rising edge of the HST_DIV_CLK and the SH0_UR_RISING edge detect monitor. Subregisters **PHI_DELAY_A** and **PHI_DELAY_B** are used to program the hemisphere-specific timing sequences. Each delay block has a fixed delay of around 150 ps for each bit. 10 bits or delay blocks are available for each hemisphere for a maximum delay of 1.5 ns. See the reference paper, "Characterization suite of a 1 ns, multi-frame hybridized CMOS imager for the ultra-fast X-ray imager program", for detailed measurements on the actual Daedalus A and B hemisphere delay measurements.[7]

16.7 Manual Shutter Control

Manual shutter control on Daedalus is performed by bypassing the Phi clock and allowing the FPGA to directly control shutter timing. Manual shutter mode can be activated by setting the **MANSHUT_MODE** subregister to '1'. This asserts the sensor pin HST_TEST_PHI_EN which shifts sensor control timing to an FPGA Phi clock. The five integration and interframe times are programmed using register addresses 0x50 through 0x54. Note: the use of the HST_DIV_CLK monitor is not needed here as the FPGA controls the timing of each integration and interframe time. Maximum timing uncertainty for first invoking integration or interframe time is equal to the FPGA's system clock period of 25 ns. The user can set each integration and interframe time to any multiple of 25 ns up to a maximum of 26.8 seconds. The minimum integration setting for manual shutters is two clock cycles of the 25 ns clock period. To prevent metastability in registering manual shutters, the software limits the user to a minimum of 75 ns integration. Manual timing cannot be set independently for the two hemispheres. Refer to the Jupyter notebook *nsCameraTutorial.ipynb* located in the nsCamera software package docs directory for a demonstration of the use of manual shutters.

16.8 High Full-Well (HFW) Programming

This feature allows a single frame to be captured that exhibits a full-well capacity three times that of a normal readout. This mode is relevant to experiments with massive fluences or for detection of high energy X-rays and is more fully described in the *Daedalus HDD-v2.docx* document. Setting the subregister **HFW** to '1' asserts both sensor pins, RSLHFWModeA and RSLHFWModeB, in addition to HSTSingleShotMode.[6] Figure 4 shows the gate profile of a 2 ns integration, 2 ns interframe time HFW gate profile.

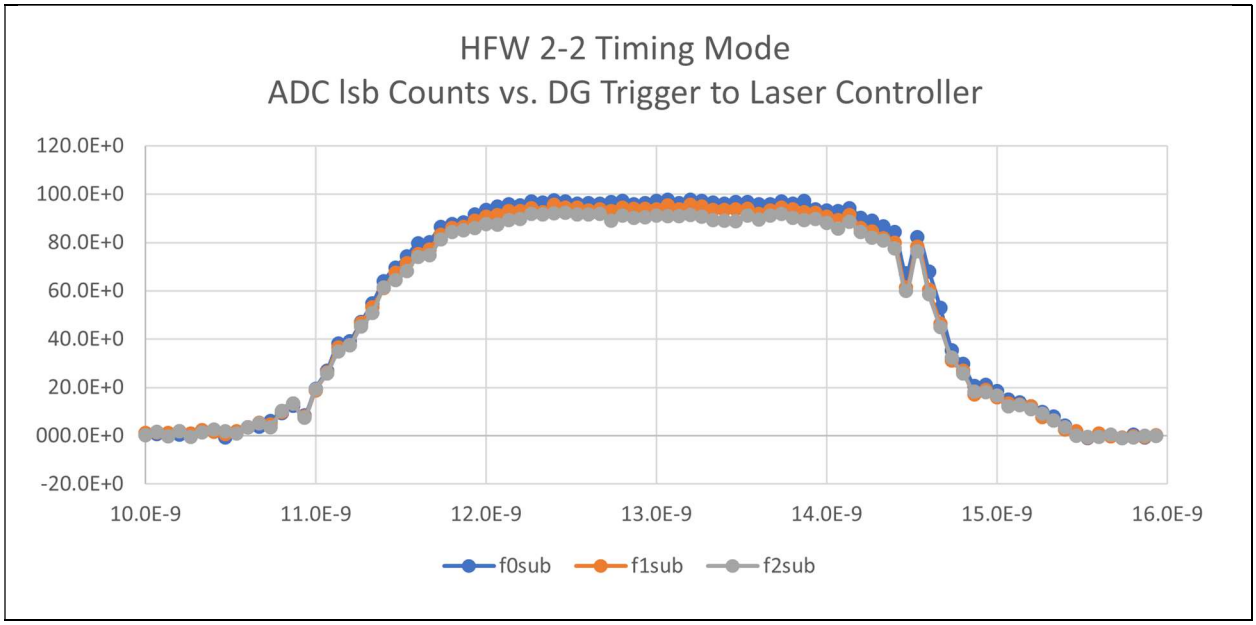

Figure 4: High Full Well Gate Profile

16.9 Zero Dead Timing (ZDT) Programming

This feature interlaces pixel rows both spatially and temporally permitting continuous data collection. This mode is described in the *Daedalus HDD-v2.docx* document. The mode can be set for each hemisphere independently through subregisters **ZDT_A** and **ZDT_B**. Six 512×512-pixel frames are generated if ZDT is implemented.

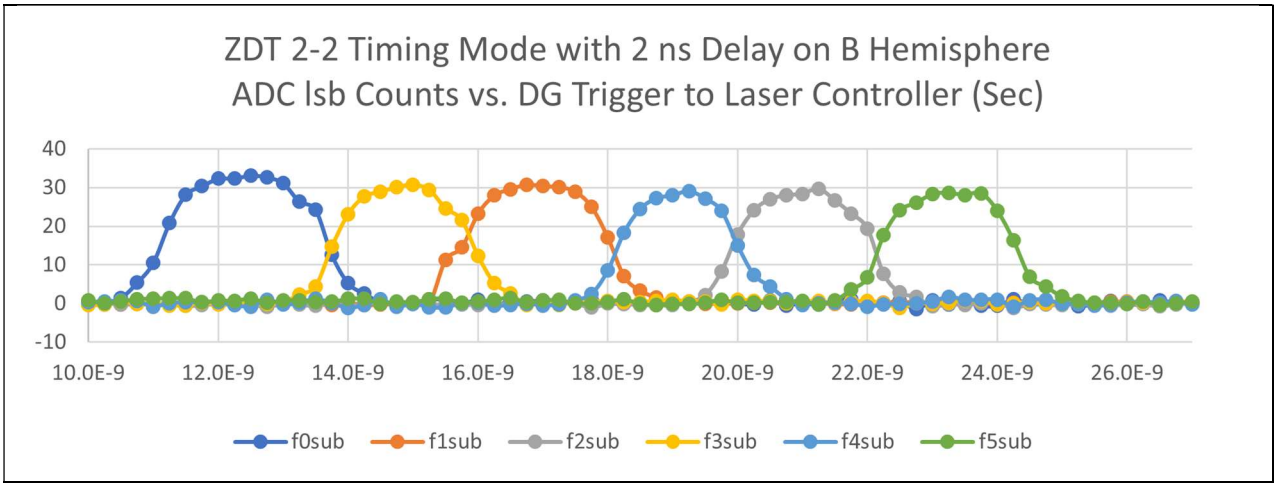

Figure 5: Zero Dead Timing Gate Profile

The drawback of ZDT is a reduction of the vertical resolution to half of its physical value. Even row shutters are 'open' according to the conventional HST scheme. Odd rows have inverted timing ('open' while the even rows are 'closed' and vice-versa).[6] Figure 5 shows the gate profile of a 2 ns integration, 2 ns interframe time ZDT gate profile.

16.10 Row Shutter Logic (RSL) Interlacing Programming

Interlacing allows for increased timing coverage; additional image frames can be acquired, but at the expense of vertical resolution. For example, twice the frames of data can be captured at half the vertical resolution (i.e., six 512×512-pixel frames rather than the original three 1024×512-pixel frames).[6] As with ZDT, the drawback to this mode is a reduction in vertical resolution by a factor of $i + 1$, where i is the interlacing factor (the number of added interlaced rows). For example, an interlacing factor $i = 3$ generates twelve frames of 256×512 resolution instead of three at 1024×512.

RSL is programmed using 1024 bits for each hemisphere. These bits are used to deserialize the shutter and inter-frame timing information from the phi clock signal. The extraction of each frame's shutter timing and inter-frame time can be set to apply simultaneously for all rows of the pixel array (the default state) or to apply sequentially for interlaced subsets of rows (e.g., even rows first, then odd rows).

Set the **INTERLACING_EN** subregister to '1' to enable RSL Interlacing. This will direct the FPGA to configure all 1024 rows restricting the minimum timing between rising edge of the Coarse Trigger and the rising

edge of the Fine Trigger to 200 µs. The user can define the interlacing factor up to 1023, allowing for a maximum of 3 x 1024 = 3,072 frames generated. Figure 6 shows the gate profile of a 2 ns integration, 2 ns interframe time with four rows interlaced gate profile showing 4 rows x 3 shutters = 12 frames. The programming of Row Shutter Logic (RSL) is described in more depth in the *Daedalus HDD-v2.docx* document.

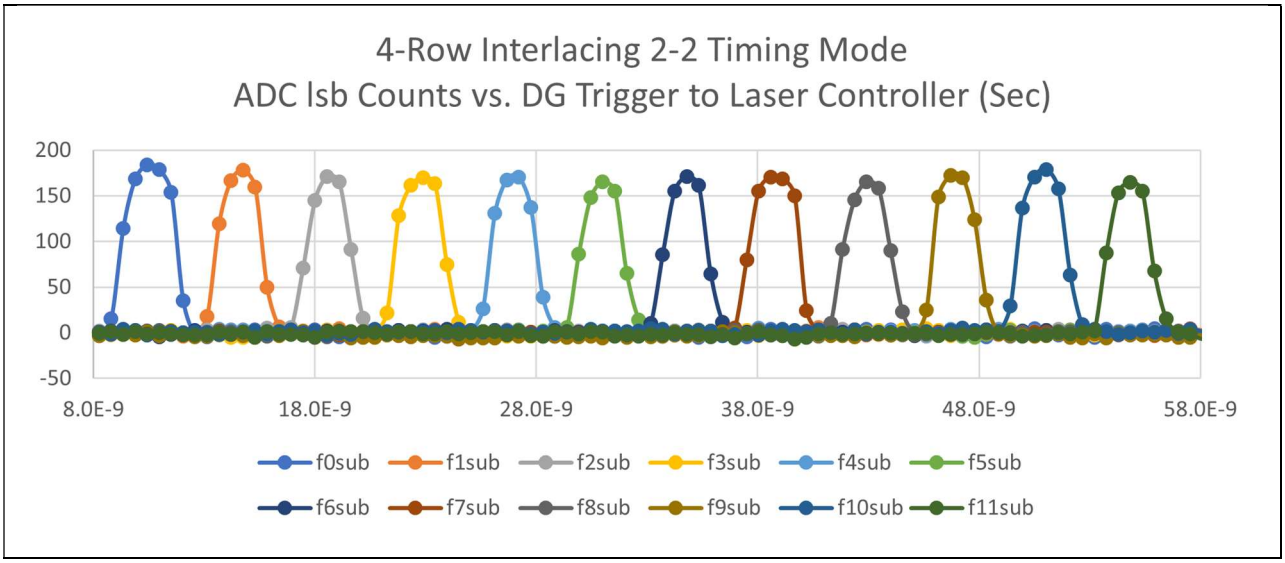

Figure 6: 4-Row RSL Interlacing Gate Profile

17 Radiation-Tolerant Modes

The radiation-tolerant features are currently Icarus-specific in terms of the firmware. They attempt to provide protection from Single-Event Upsets (SEUs) that might strike sensitive nodes on the circuitry or upset the firmware in certain areas. Current Icarus-specific firmware uses both Triple Modular Redundancy (TMR) and Hamming Encoding in crucial areas of the FPGA to provide extra protection. Radiation-protection features are intended for use with the RS422 communication protocol.

17.1 Suspend Mode

This mode holds various modules in reset for a default 100 µs upon every rising edge of the fine trigger, delaying the use of potentially sensitive FPGA modules until the passing of the radiation event. RS422 communication, for example, is held in reset until the suspend mode duration has elapsed. The default duration can be overwritten with the SUSPEND_TIME register.

17.2 Blink Mode

This mode has only been utilized with Icarus firmware and is not yet ready for general use. It is available for limited offline testing due to the FPGA power down causing the CMOS image capture process to fail (losing images). If intense radiation exposure is expected, critical radiation-susceptible hardware can be

turned off by putting the device into blink mode to prevent hardware upset. The external AUX input can be used to put the board into blink mode. The mode will initiate a power-down of the following hardware components on the camera board without turning off power to the sensor:

- Image-readoff ADCs
- DAC
- External reference for image-readoff ADCs
- FPGA
- Crystal oscillator for FPGA
- SRAMs
- Pressure sensor
- Temperature sensor
- Push-button reset
- GigE
- RS422
- ADC monitors

Figure 7 shows the recommended timing of blink mode, which should only be used with hardware triggers.

1. The external Coarse Trigger must be asserted for at least 60 ns to allow the FPGA to detect the trigger.
2. The external AUX Trigger should be asserted no sooner than 11.5 µs after the rising edge of the Coarse Trigger to allow time for the FPGA to program the high-speed timing of the sensor.

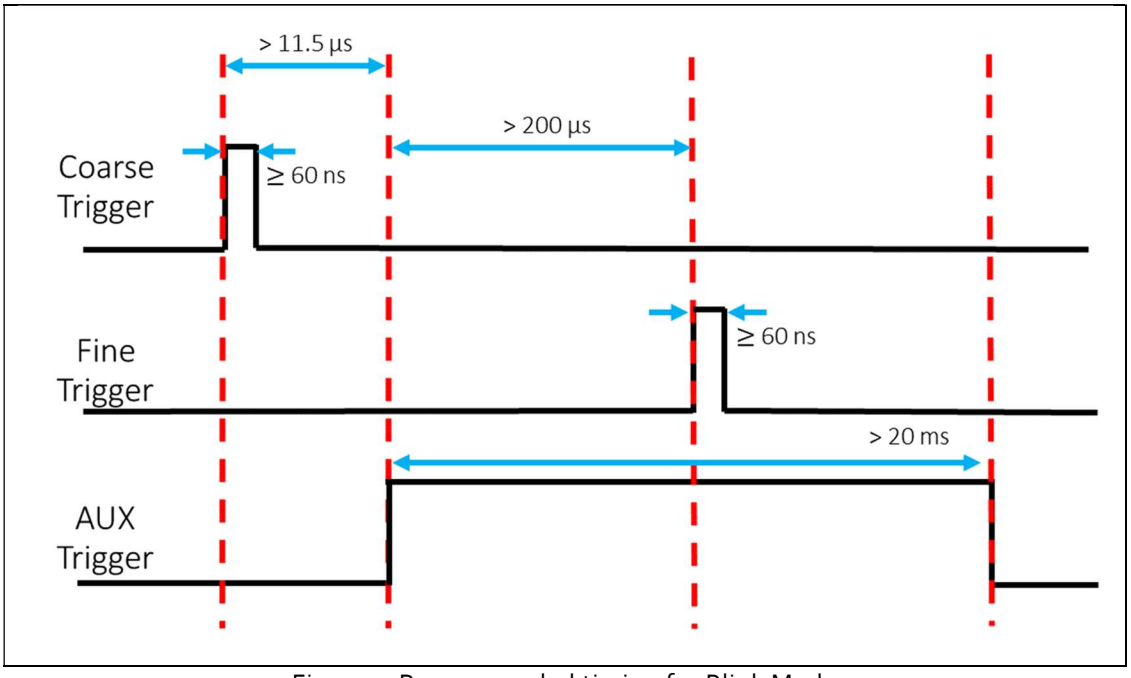

Figure 7. Recommended timing for Blink Mode

3. The AUX must be asserted for at least 200 µs before the Fine Trigger is issued in order to fully power down the FPGA.
4. When the AUX input is de-asserted, the hardware components are turned back on and various system parameters are reset.
5. The FPGA waits 40 ms after powerup before automatically initiating pixel readoff from the sensor to the SRAM as a precaution against artifacts or noise caused using by the AUX trigger. This delay is configurable using the **TIME_ROW_DCD** register.
6. Sensor readoff to SRAM takes about 178.59 ms for a 4-frame capture and 89.29 ms for a 2-frame capture.
7. Once readoff is complete, the FPGA sets the **SRAM_READY** bit of the **STAT_REG** register to "1".
8. The software monitors this **SRAM_READY** bit to know when to download image data from SRAM to the host.

18 RS422 USB Cable

The RS422 USB cable that has been tested for the camera board is the ACCESS I/O Products, Inc. USB-422-IND cable. The datasheet and drivers for this product can be accessed at https://accesio.com/?p=/usb/usb-232-422485-IND.html .

19 Software Support

The 'nsCamera' python package provides a software driver and user interface for operating the NSGC camera. The software runs on Windows, MacOS and Linux. Python 3 is recommended; Python 2 is supported but deprecated.

The software is distributed as a compressed archive or is available as part of a complete pre-packaged python environment. Instructions for installation and use are given in the project's README.md file. The software is also available as a MicroManager plugin for use in imageJ.

A Jupyter notebook tutorial *nsCameraTutorial.ipynb* that introduces the software and demonstrates many of the board's features can be found in the *nsCamera/docs* directory. This directory also contains detailed code documentation and the test script *testSuite.py*, which performs an extensive sequence of tests to verify the proper operation of the hardware and software.

20 ELM-U References

LLNL's Enterprise Lifecycle Management – Unclassified (ELM-U) stores various references for the LLNL V4.0 board. Specifically, the revisions of the board are documented and divided into two boards: FPGA and ADC board. The references include schematics, Gerber files, CAD drawings, etc. The ELM numbers (assembly numbers) for the green FPGA and ADC boards are **1002464594** and **1002550381** respectively and for the red FPGA and ADC boards are **1007765984** and **1007766734** respectively.

21 Change note history

See the first page of this document for more recent changes.

Rev.	Date	Section Edits	Eng.	Description of Change
1.0	10/19/17	N/A	CCM	Initial Release
1.01	12/27/17	13	CCM	Fix dual_edge_Trig_en description – s.b. in trigger_ctl register
1.02	1/22/18	13	CCM	Fix typos in register table entries for register 0x99 ADC5_DATA_4.
1.03	2/8/18	14.7	CCM	Add table listing all FPGA resets for rad hard version.
1.04	3/7/18	11-14, 16	JMH	Divergence of Icarus & Daedalus ICD versions Change to 12-bit register addresses Removed specifications for Sandia Rev C board
1.05	3/20/18	13	JMH	Removed obsolete registers
1.06	4/10/18	-	JMH	Divergence of LLNLv1 and LLNLv4 versions Expanded FPGA_NUM definitions
1.07	6/26/18	-	JMH	Spinoff of sensor-specific implementation into separate document. Added subregister names to register list
		1.1-12	BTF	Revised ADC monitor registers, removed temperature sensor data and pper registers, revised DAC registers, replaced POT with DAC channel, revised POT11 to DAC Channel G, ADC_CTL register and ADC_RESET register now controls only 4 of the 16-bit ADCs (ADS8568)
1.08	7/31/18	All	JMH	Register and subregister definitions added Reintegration of sensor-specific details
1.09	9/26/18	1.1-12	JMH BTF	Revised ADC monitor registers, removed temperature sensor data and pper registers, revised DAC registers, replaced POT with DAC channel, revised POT11 to DAC Channel G, ADC_CTL register and ADC_RESET register now controls only 4 of the 16-bit ADCs (ADS8568)
1.10	12/5/18		JMH	Updated default DAC values, VRESET_HIGH is 16 bits
1.11	6/4/19	13	JMH	Added SW_TRIG_EN, Daedalus mode details
1.12	6/24/19	All	BTF	Edited the description of each pot for an ICARUS configured board. Pointed the register map descriptions to the appropriate section to describe the pot/dac channel. Removed sensor power control section 6.4. Edited automatic sensor detection is unavailable currently. Minor edits throughout the sections. Synced to nsCamera 2.0.8
1.13	9/30/19	5, 7, 13.1	BTF	More detailed information on the Daedalus-configured board for pot values. Added TRIGGER_CTL register info for previous firmware version vs. after of 9/19.
1.14	11/8/19	3	BTF JMH	Updated block diagram to include BJT dosimeter. Updated ADC_PPER description, trigger operations

1.15	11/13/19	2, 6, 7, 11.1, 13, 16	BTF	Removed italicization and modified ADC monitor table for Daedalus to be 1.0 and 2.0 instead of 1 and 2 V. Resolved comments made by Jeremy. Updated default DAC channel voltages in Register Map section. Need input on if we want to describe pot voltage values in the register map as it is redundant from Section 6 and 7. Need update on CTL_REG in Section 13 for reverse readoff and slow readoff.
1.16	1/5/20	9, 11	BTF	Reworded Temperature Sensor section for the scale from 12-bits to 7-bits. Revised register definitions to match LLNL_v4.py board file script with respect to monitor ADC names.
1.17	2/14/20	11	BTF	Removed SENSOR_VOLT_STAT and SENSOR_VOLT_CTL registers. Removed September 2019 TRIGGER_CTL setting for the trigger modes.
1.18	2/29/20	5.1 6, 12.1	BTF	Described in more detail on Daedalus sensor pins that are disconnected by DAC channels, yet able to be monitored by ADC monitors. Moved tables 3 and 4 in order (MS Word issue possibly). Edited dual edge trigger section. Synced to nsCamera 2.0.9
1.19	5/4/20	3, 6, 11, 14.1, 15	BTF	Attempted to resolve comments: resolved figure with Daedalus timing block, explained more details on dual edge trigger, described details for Daedalus registers, and added what features work for Daedalus and what features do not. Edited section 14.1 to accommodate v4 ADC context.
1.20	5/24/20	5,7,11 13,14	JMH	Sensor-specific details moved to sensor sections and restructured. Removed unused quad_enable registers. Updated Daedalus DAC & monitor assignments
1.21	8/13/20	12, 14, 15	BTF	Added V4 specific register and sub registers to accommodate PDBIAS status, control of PDBIAS, and control of ROW_DCD_ENABLE. Edited Section 14.2 and 15.1 tables.
1.22	9/22/2020	2, 7, 13.1, 16	BTF	Added the sensor readoff time for Daedalus. Added new section on Radiation-Tolerant Modes. Fixed up register map with respect to Daedalus implementation. Updated Daedalus Implementation section.
2.0	10/16/2020	6.3, 12.1, 14, 15, 16, 18	BTF	Added Section 18 mentioning the RS422 USB driver location that is used and primarily tested with the hardware. Added Section 20 to discuss ELM-U references to the board. Rewrote Daedalus sections for bypass Phi Clock and RSL programming in Section 16 . Updated temperature data in STAT_REG as 12-bits instead of 11 bits and confirmed Daedalus RSL left and right signals as always '0' in Section 13.1 . Updated Dual Edge Trigger. Also updated the title of the ICD as LLNL v4 Camera Board instead of " " " FPGA Board. Moved Power Save Mode Section to Icarus Implementation Section 15 since the mode applies only to Icarus. POWERSAVE subregister was also changed to Icarus only. LED_EN subregister was removed since there are no controllable LEDs on the Ver 4.0 board. Synchronized to nsCamera 2.1
2.0.1	11/3/2020	12.1	BTF	Added MISC_SENSOR_CTL register to control miscellaneous Icarus sensor pins.
2.0.2	1/8/2021	12.1	BTF	Added five more bits to MISC_SENSOR_CTL register for accumulation mode control and reordered the register.
2.0.3	2/1/2021	12.1	JMH	Rename of STAT_POTSCONFIGURED to STAT_DACSCONFIGURED
2.0.4	6/28/2021	12.1	JMH	Added SW_COARSE_CONTROL register
2.1	7/6/2021	-	JMH	nsCamera software release 2.1.1

22 References

1) Sandia National Laboratories, et al. “UXI ICARUS – Focal Plane Array Interface Document.” Revision 6, 8/23/16
2) Claus, L., et al. “An overview of the Ultra-Fast X-ray Imager (UXI) program at Sandia Labs.” Proceedings Volume 9591, *Target Diagnostics Physics and Engineering for Inertial Confinement Fusion IV*; 95910P (2015); doi: 10.1117/12.2188336
3) Claus, Liam D., et al. “The Ultrafast X-ray Imager (UXI) Program.” No. SAND2016-7045PE. Sandia National Laboratories (SNL-NM), Albuquerque, NM (United States), 2016.
4) Claus, L., et al. "Design and characterization of an improved 2 ns multi-frame imager for the ultra-fast x-ray imager (UXI) program at Sandia National Laboratories." Proc. SPIE 10390, *Target Diagnostics Physics and Engineering for Inertial Confinement Fusion VI*, 103900A (24 August 2017); doi: 10.1117/12.2275293
5) Sanchez, Marcos. “Icarus HDD V2.” Version 8. Advanced Hybrid CMOS Systems (AHS), Albuquerque, NM (United States), February 22, 2024.
6) Sanchez, Marcos. “Daedalus HDD-v2.” Revision 15. Advanced HCMOS Systems (AHS), Albuquerque, NM (United States), October 7, 2022.
7) Garafalo et al. (2023, October 3). “Characterization suite of a 1ns, multi-frame hybridized CMOS imager for the ultra-fast x-ray imager program.” Livermore, CA, United States of America.