AEG | MIS

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Description of interface:

Direct driven LCDs with Drivers of MIS-Series 6000

445 922.BG

„ Only for Information “
„ Will not be exchanged by matter of revision “

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1. Technology

The driver ICs (s. fig. 1) are CMOS devices for static driven LCDs. They are mounted in TAB-technology (Tape Automated Bonding) onto the rim of the displays glass. They belong to the class of electro-statically endangered devices which have to be treated according to the valid ESD guide lines.The interface between the display and the external drive electronics consist of 8 or 9 lines :

1. DI data input
2. V_{CC} supply voltage for the logic part of the IC
3. V_{DD} supply voltage for the segment outputs of the IC
4. V_{SS} ground
5. R reset
6. FL switching frequency of the segment outputs
7. LD strobe (LOAD)
8. CL clock frequency (CLOCK)
9. DO data output (optional)

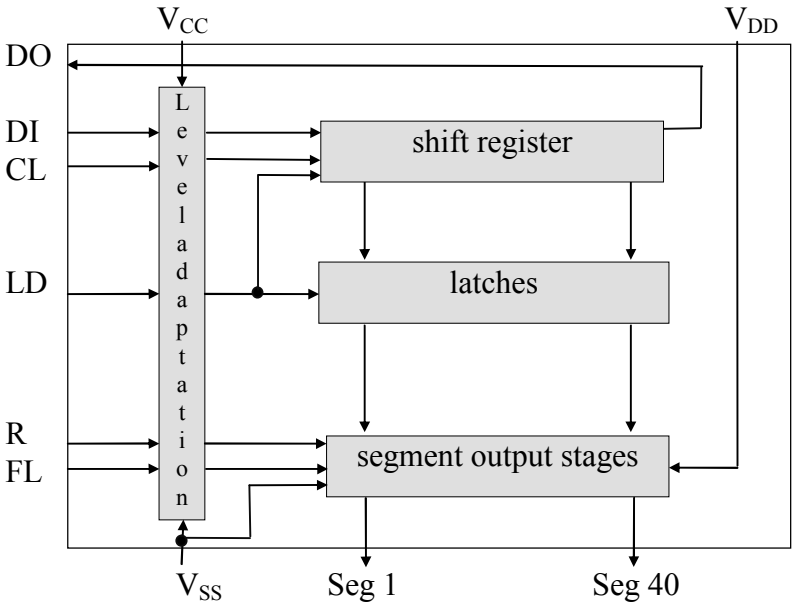


Diagram 1 : Block diagram of the driver function

2. Supply voltages V_{CC} and V_{DD}

During operation it must be ensured that V_{DD} is always greater than V_{CC}. In case of $V_{DD} < V_{CC}$ the damping diodes in the driver will feed from V_{CC} to V_{DD}. Consequently the current in V_{CC} will increase and cause a malfunction of the device and in extreme cases this leads to the destruction of the IC.

If the FL-signal is missing V_{CC} and V_{DD} have to be set to V_{SS} -potential.
By switching off the electronics (the interface signals are undefined) V_{CC} and V_{DD} have to be switched off at the same time.

3. Control lines

The control lines CL, LD, R and FL are operated in a parallel mode. Together with the DI-line they are converted internally via level converter to the supply voltage level V_{CC}. The segment output stages are supplied with the higher supply voltage V_{DD}. The DO-signal is always at the V_{CC} or V_{SS}-level.

3.1 Data input DI / data output DO

The data input of the LCD is connected to the data input of the first IC of the LCD. If there are several drivers on the display in each case the data output of the preceding component is linked to the data input of the following driver. Additionally the DO signal can be used to check the proper function of the LCD.

All supply and control lines are fed in general to a 8-pin or 9-pin input plug. In case of cascadable LCDs the DO-line of the last driver is fed to the 8^{th} pin of an output plug or to the 9^{th} pin of the input plug.

By using the DI-line the data are read into the internal shift register by allocating every bit to a defined segment of the display. The exact allocation segment ↔ bit is described in the individual bit map (Funktionsplan) of the LCD.

If the backplane (BP) of the display is also operated by the driver every segment to be activated has to have the inverse logical information as the backplane e.g. if for the backplane a logic ´0´ (´1´) is used, a logic ´1´ (´0´) will activate the segment.

In case of displaying the same information for a longer time, the corresponding data word has to be read into the display in regular time intervals (e.g. 1 sec.) in order to avoid a damage of the drivers or the whole LCD. This may happen if the data word is changed by disturbing signals.

3.2 Clock signal CL

The clock signal CL is the clock frequency for the internal shift register of the drivers. The data at DI is transfered into the shift register with the falling edge of CL (see 5. Operating conditions). The setup time between DI and CL has to be ≥ 250 ns.

3.3 Strobe signal LD

The control line LD is used to connect and separate the outputs of the shift registers to the latches of the driver. The triggering is done by level and not by the edge of the LD-signal. If the LD-signal is ´high´ the data are transfered from the shift registers to the latches. The LD-pulse itself has to be triggered always to the same edge of the FL-signal.
Thus the feeding of the data into the shift register is separated from the status of the display and the data can be shifted through the shift registers until they have reached the correct position without changing the segment outputs.

3.4 Switching frequency FL

The FL-frequency allows the invertion of all segment outputs at the same time thus producing the AC voltage for driving the LCD. This AC voltage has to be free from DC components : $V_{DC} \leq 50$ mV . In order to reach this, the duty factor of the FL-signal has to be 1 : 1.

The FL frequency should be around 64Hz and in the range between 30 and 70 Hz. The range of 50 Hz should be avoided because of possible interferences with the ambient light.

3.5 Reset signal R

With the reset signal R all segment outputs can be set simultanously to zero. As long as the reset signal R is ´high´ all segment outputs are ´0´. The information in the shift register and in the latches are not affected.
The reset signal is used to avoid undefined states and short circuits between parallel operating segments (e.g. backplanes) during the switching on and switching off periods.
After switching on the external driving electronic the reset line R has to be held on ´high´ as long as the correct information is being shifted into all drivers. Thereafter R can be set to ´low´ or ´V_{SS}´.
If the reset line R is not used it has to be tied to V_{SS}.

4. Cascading of LCDs

As mentioned in 3.1 LCDs with static drivers of the MIS sequence 6000 can be cascaded. When cascading LCDs a so called “module driver“ containing a signal driver and capacitors has to be used between each 2 LCDs which guarantees the required form of the signals. An operation without errrors and particulary a correct data flow can not be guaranteed if no such module driver is used.

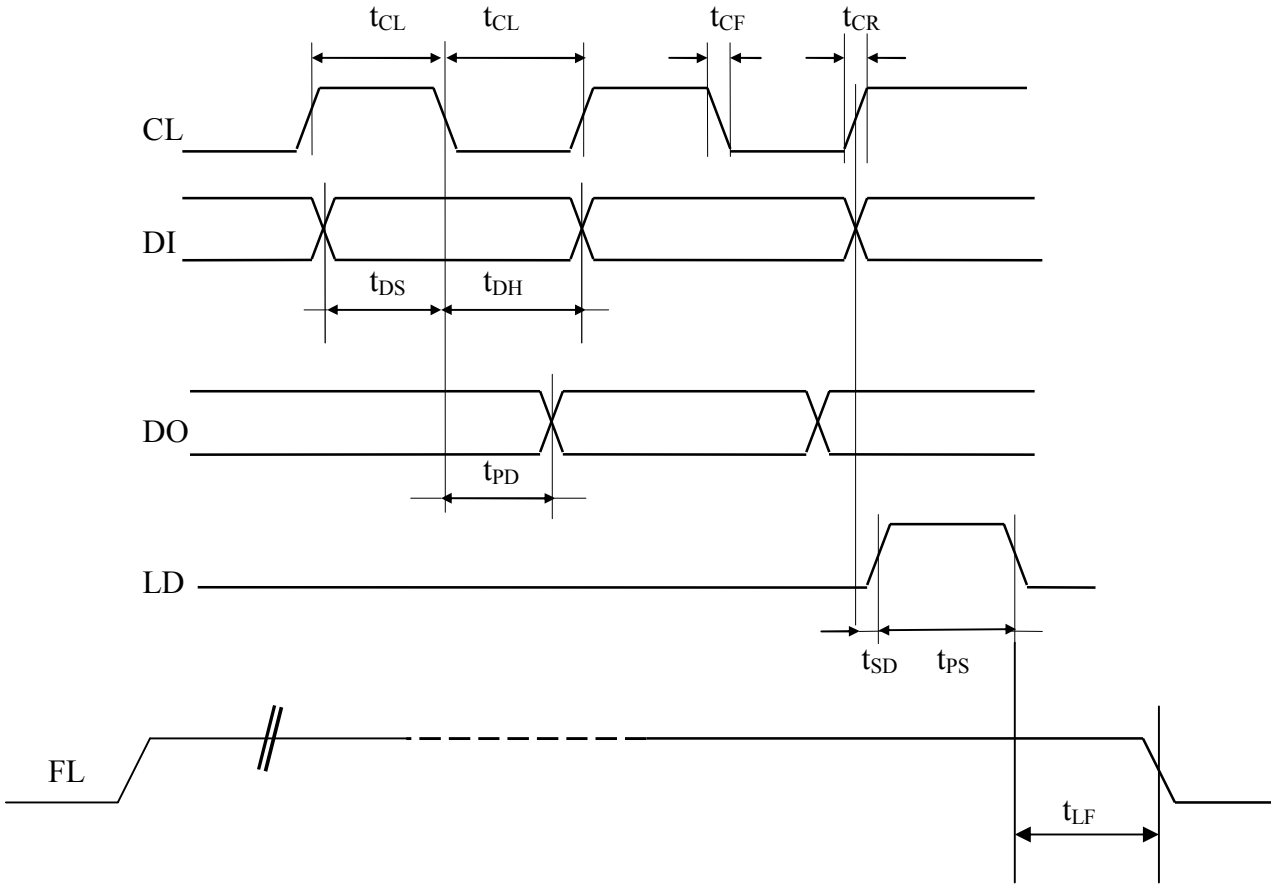
5. Operating conditions:

The specific operating values for the LCDs have to be taken from the specific data sheet „Typblatt“ of the LCD.
The values in the following table are for individual drivers. If not otherwise indicated : T = 25°C.

Parameter	condition	symbol	min.	typ.	max.	unit
supply voltages						
LCD supply voltage		V_{DD}	5,0	8	12,0	V
logic supply voltage		V_{CC}	4,75	5	5,25	V
static current in V_{DD}		I_{DD}			10	µA
static current in V_{CC}		I_{CC}			5	µA
data output DO						
H - output voltage		V_{DOH}	4,5			V
L - output voltage		V_{DOL}			0,5	V
control lines						
H - input voltage	V_{CC} = 5 V		3,6			V
L - input voltage	V_{CC} = 5 V				0,8	V
input current	V_{CC} = 5 V			5		µA
input capacity	pro IC	C_I			5	pF
CL frequency		CL		100	300	kHz
FL frequency		FL	30	64	128	Hz
rise time for DI, CL, LD, FL, R		t_R			0,5	µs
CL-pulse width High	V_{DD} = 5 V	t_{CL}	1,5			µs
CL-pulse width Low	V_{DD} = 5 V	t_{CL}	1,5			µs
CL rise time	V_{DD} = 5 V	t_{CR}			0,5	µs
CL fall time	V_{DD} = 5 V	t_{CF}			0,5	µs
DI-setup-time	V_{DD} = 5 V	t_{DS}	0,25			µs
DI-hold-time	V_{DD} = 5 V	t_{DH}	0			µs
DO-propagation	V_{DD} = 5 V	t_{PD}	0,02	0,6	0,8	µs
LD- pulse width	V_{DD} = 5 V	t_{PS}	3		$2t_{CL}$-t_{DS}*	µs
LD-pulse delay	V_{DD} = 5 V	t_{SD}	0		$2t_{CL}$-t_{DS}*	µs
LD synchronisation to FL		T_{LF}		5		µs
power dissipation	P			100		mW

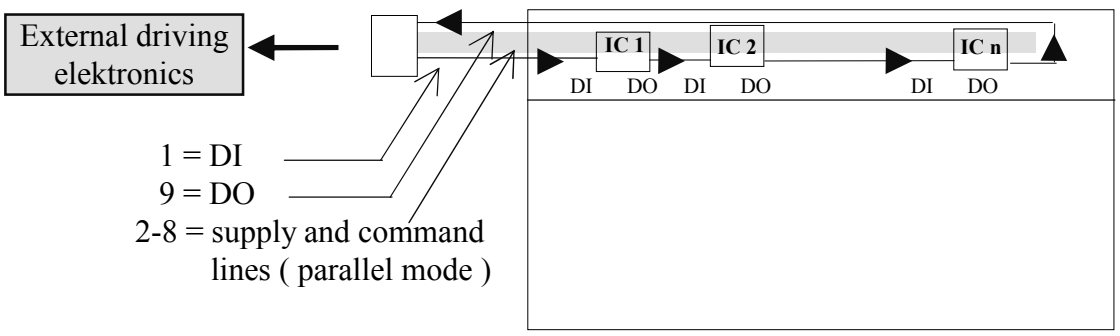
* : only limited when IC´s are cascaded.

Timing waveforms :

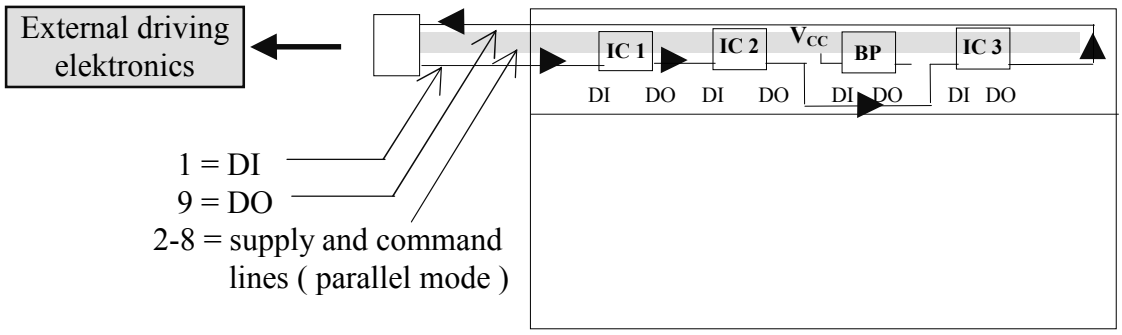


6. Applications

6.1.1. one LCD with one IC - rim (several ICs)

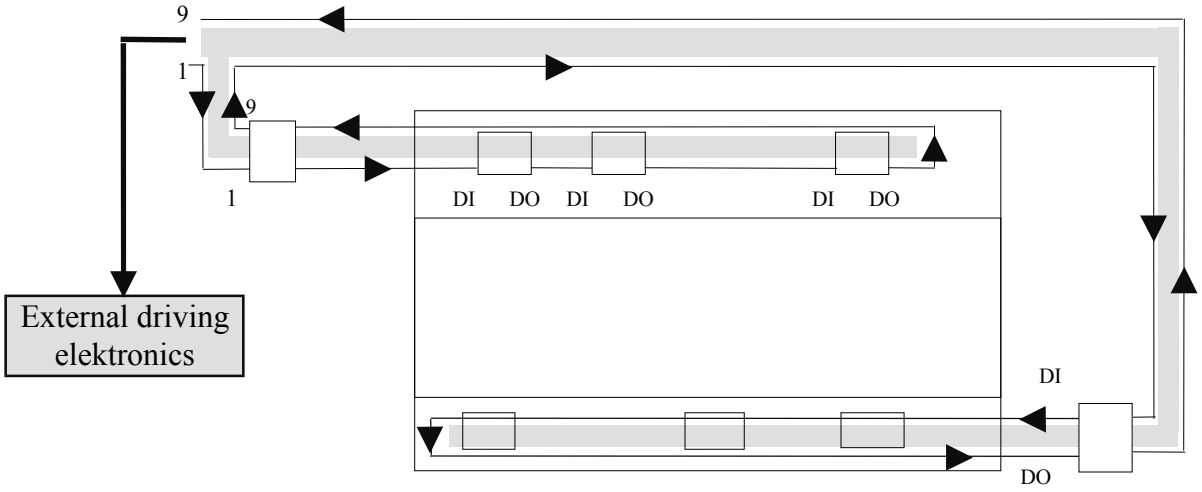


6.1.2. one LCD with several ICs and one ore several backplane-ICs (BP)

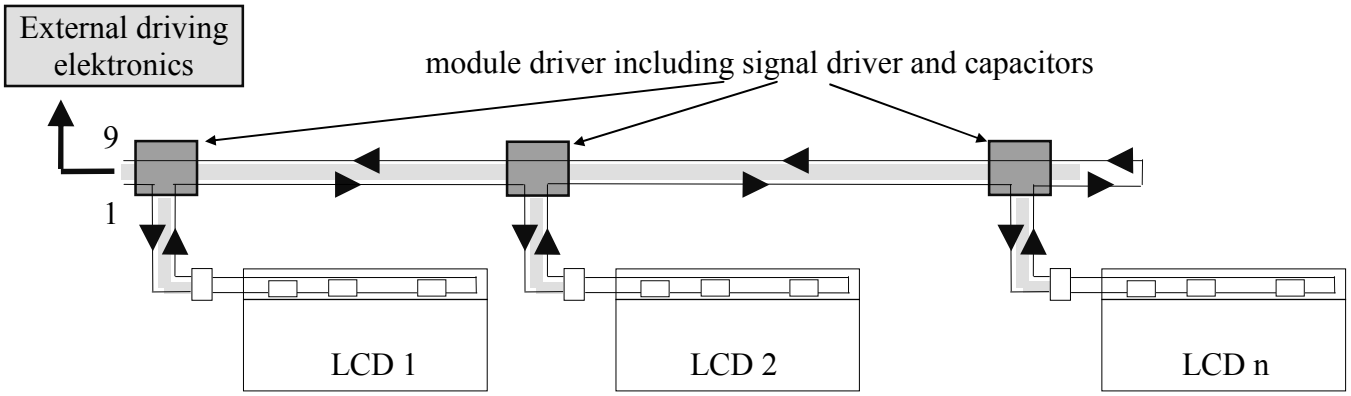


Remark : The DI of the BP-ICs are on V_{CC}-potential, therefore the BP-potential is logical „High“. The DO of the BP-ICs are open. The DO of the proceeding IC is connected with the DI of the succeding IC.

6.2 one LCD with two IC - rims



6.3 Cascade of several LCDs with one IC rim



6.4 Cascade of several LCDs with two IC rims