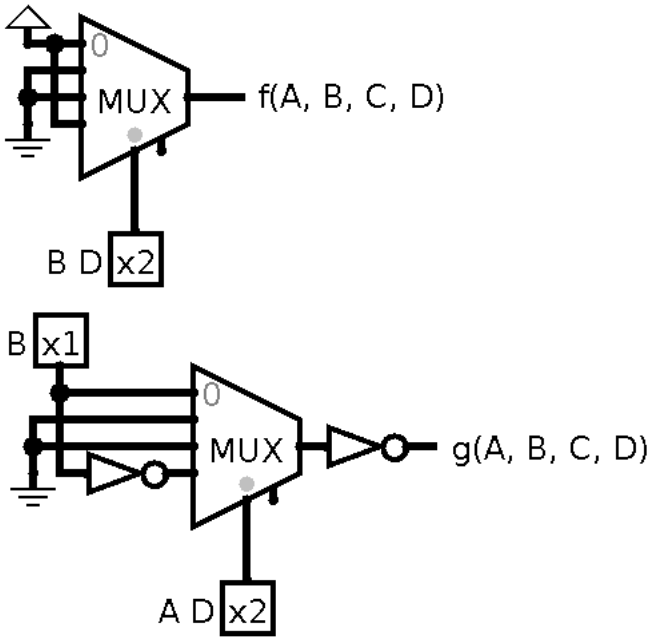
Homework 4

Mitchel Fields

March 3, 2016

Problem 1



Problem 2

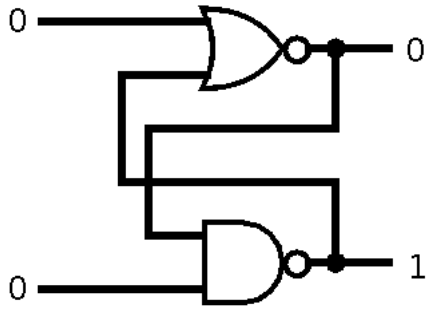
```
# Mitchel Fields
# Mux simulator for f(A,B,C,D) and g(A,B,C,D)

def NOT(a):
        return 1 - a

def mux(I0, I1, I2, I3, C1, C0):
        if (C1 & C0) == 1:
                return I0
        elif (NOT(C1) & C0) == 1:
```

```
            return l1
        elif (C1 & NOT(C0)) == 1:
            return l2
        else:
            return l3

def main():

    print( "  A  B  C  D  |  f  g  " )
    print( "--------------+--------" )

    for A in [0,1]:
        for B in [0,1]:
            for C in [0,1]:
                for D in [0,1]:
                    f = mux(1,0,0,1,B,D)
                    g = NOT(mux(B,0,0,NOT(B),A,D))

                    print("%3d%3d%3d%3d  |%3d%3d" %
                          (A, B, C, D, f, g))

main()
```

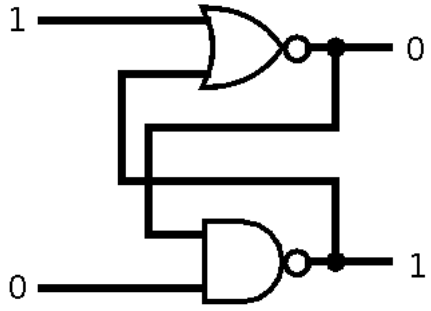
A	B	C	D	f	g
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0

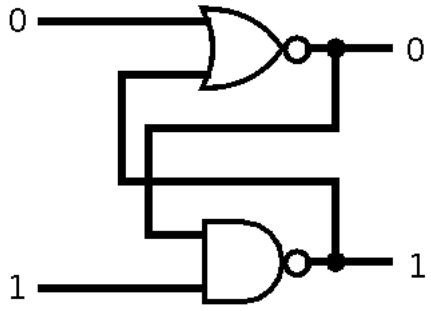
Problem 3

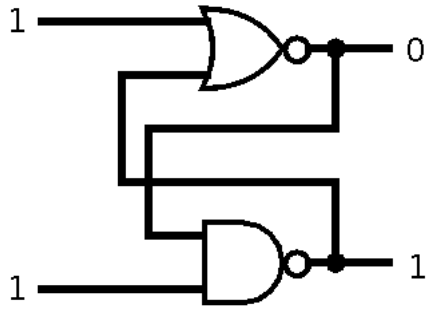
The circuit is not a latch. When initialized, the ciruit will default to the following state:



And cannot be changed:

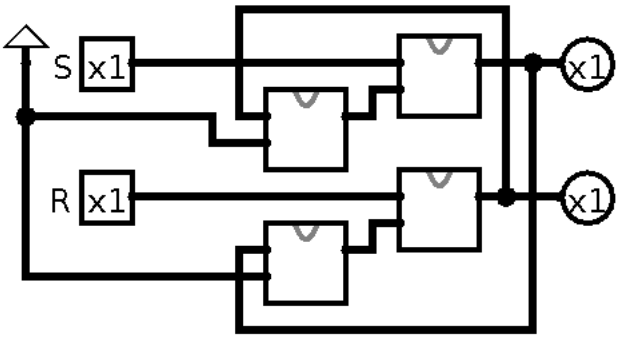






Problem 4

A latch can be created with the first gate the following way (the square gates represent the AND with an inverted input):



The XOR with an inverted input cannot be made into a latch. It can only implement an inverter and, through that, an XOR and XNOR. These gates cannot be arranged to be equivalent to a NOR or a NAND gate. They cannot be made to pass in 3 states and block in 1 and, thus, cannot form a latch.