MIPS_ONEMORE

author: Maksim Shaklunov

email: mshaklunov@gmail.com

2015

1 Pins

Name	Dir	Description
System		
sys_clk	input	Clock
sys_rst	input	0: Idle. 1: Synchronous reset.
sys_int[5:0]	input	Six hardware maskable interrupts with active high level.
Program memory interface (Wishbone pipelined mode)		
pmem_stall_i	input	Wishbone STALL_I signal.
pmem_ack_i	input	Wishbone ACK_I signal.
pmem_dat_i[31:0]	input	Wishbone DAT_I signal.
pmem_adr_o[31:2]	output	Wishbone ADR_O[31:2] signal. ADR_O[1:0] must be tied to low level.
pmem_cyc_o	output	Wishbone CYC_O signal.
pmem_stb_o	output	Wishbone STB_O signal.
Data memory interface (Wishbone pipelined mode)		
dmem_stall_i	input	Wishbone STALL_I signal.
dmem_ack_i	input	Wishbone ACK_I signal.
dmem_dat_i[31:0]	input	Wishbone DAT_I signal.
dmem_adr_o[31:2]	output	Wishbone ADR_O[31:2] signal. ADR_O[1:0] must be tied to low level.
dmem_dat_o[31:0]	output	Wishbone DAT_O signal.
dmem_cyc_o	input	Wishbone CYC_O signal.
dmem_stb_o	output	Wishbone STB_O signal.
dmem_we_o	output	Wishbone WE_O signal.
dmem_sel_o[3:0]	output	Wishbone SEL_O signal.

2 Implemented instructions

	Branch	40	SLLV
1	BEQ	41	SRLV
2	BNE	42	SRAV
3	BLEZ	43	SLT
4	BLTZ	44	SLTU
5	BGTZ	45	SLTI
6	BGEZ	46	SLTIU
7	J	47	SUB
8	JR	48	SUBU
9	JAL	49	XOR
10	JALR	50	XORI
	Memory		**CP0**
11	LB	51	ERET
12	LH	52	MTC0
13	LW	53	MFC0
14	LBU		
15	LHU		
16	SB		
17	SH		
18	SW		
	ALU integer		
19	ADD		
20	ADDU		
21	ADDI		
22	ADDIU		
23	AND		
24	ANDI		
25	DIV		
26	DIVU		
27	LUI		
28	MULT		
29	MULTU		
30	MFHI		
31	MTHI		
32	MFLO		
33	MTLO		
34	NOR		
35	OR		
36	ORI		
37	SLL		
38	SRL		
39	SRA		

3 CP0

MIPS_ONEMORE has the system control coprocessor (CP0) which provides exception handling. When reset condition is becoming then program counter is loaded by 0xBFC0_0000, all other exceptions load program counter by 0x8000_0000. Five registers is implemented in CP0.

CP0 registers

Number	Name	Description
0-7	-	Reserved in the MIPS_ONEMORE.
8	BadVAddr	Reports the address for the most recent address-related exception.
9-12	-	Reserved in the MIPS_ONEMORE.
12	Status	Processor status and control.
13	Cause	Cause of last exception.
14	EPC	Program counter at last exception.
15-31	-	Reserved in the MIPS_ONEMORE.

BadVAddr

Number	Access	Reset	Name	Description
31:0	R	0	BadVAddr	Bad memory address at which address error exception occured.

Status

Number	Access	Reset	Name	Description
31:16	R	0	-	Reserved.
15:10	R/W	0	IM7-IM2	Interrupt Mask. Controls the enabling of each of the hardware interrupts. An interrupt is taken if interrupts are enabled and the corresponding bits are set in both the Interrupt Mask field of the Status register (IM7-IM2) and the Interrupt Pending field of the Cause register (IP7-IP2) and the IE bit is set in the Status register.
9:2	R	0	-	Reserved.
1	R/W	1	EXL	Exception Level. Set by the processor when any exception is taken. When EXL is set: • Interrupts are disabled. • EPC, Cause will not be updated if another exception is taken.
0	R/W	0	IE	0: Interrupts are disabled. 1: Interrupts are enabled.

Cause

Number	Access	Reset	Name	Description
31	R	0	BD	Indicates whether the last exception taken occurred in a branch delay slot: 0: Not in delay slot. 1: In delay slot.
30:16	R	0	-	Reserved.
15:10	R	0	IP7-IP2	Hardware interrupt signals, sampling value of sys_int bus.
9:2	R	0	-	Reserved.
6:2	R	1	ExcCode	Exception code. 0: Interrupt. 4: Address error exception (load). 5: Address error exception (store). 10: Reserved instruction exception. 12: Arithmetic overflow exception.
1:0	R	0	-	Reserved

EPC

Number	Access	Reset	Name	Description
31:0	R/W	0	EPC	Contains program counter value at which processing resumes after an exception has been serviced.

.