

**USB\_DEVTRSAC**

**Verification table**

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No	Testcase description	Testcase in testbench
1	POWERED state. All EPs is not active at any USB transactions. Transaction interface has no any activity.	tcase_powered
2	DEFAULT state. - Detecting USB reset. - EP0 is available through Control transfers. - EP15-1 is not active at any USB transactions.	tcase_default
3	ADDRESSED state. - Processing SetAddress() request. Applying new address. - EP0 is available through Control transfers. - EP15-1 is not active at any USB transactions. - EP15-0 is not respond at transaction with previous address. - Transition to DEFAULT state with SetAddress(0). - Transition to DEFAULT state with USB reset.	tcase_addressed
4	CONFIGURED state. - Processing SetConfiguration() request. - All EP15-0 is available through transactions. - Transition to ADDRESSED state with SetConfiguration(0). - Transition to DEFAULT state with USB reset.	tcase_configured
5	SUSPENDED state. - POWERED to SUSPENDED and back. Wakeup signaling is not available in POWERED state. - DEFAULT to SUSPENDED and back. Wakeup signaling is not available in DEFAULT state. - ADDRESSED to SUSPENDED and back. Wakeup signaling is not available in ADDRESSED state. - CONFIGURED to SUSPENDED and back. Wakeup signaling is not available in CONFIGURED state. - Remote wakeup signaling.	tcase_suspended
6	Bulk/Interrupt transfers. - BulkIn with various packet size. - BulkIn with NAK. - BulkIn with STALL. - BulkIn host don't reply by handshake. - BulkOut with various packet size. - BulkOut with NAK. - BulkOut with STALL. - BulkOut host send data with previous DATA PID. - InterruptIn with don't care about ACK (always toggle bit). - Resetting toggle bits with SetConfiguration().	tcase_bulkint

No	Testcase description	Testcase in testbench
	<ul style="list-style-type: none"> <li>- Not resetting toggle bits with failed SetConfiguration().</li> <li>- Resetting toggle bits with ClearFeature(EP_HALT).</li> <li>- Not resetting toggle bits with failed SetConfiguration(EP_HALT).</li> <li>- Resetting toggle bits with ep_enable inputs.</li> </ul>	
7	<p>Isochronous transfers.</p> <ul style="list-style-type: none"> <li>- IsochronousIn with various packet size.</li> <li>- IsochronousOut with various packet size.</li> <li>- SOF receiving</li> </ul>	tcase_trfer_isoch
8	<p>Control transfers.</p> <ul style="list-style-type: none"> <li>- ControlIn interleaved BulkIn.</li> <li>- ControlIn interleaved BulkOut.</li> <li>- ControlIn interrupted by ControlIn.</li> <li>- ControlIn with multiple Status stage.</li> <li>- ControlOut interleaved BulkIn.</li> <li>- ControlOut interleaved BulkOut.</li> <li>- ControlIn interrupted by ControlOut.</li> <li>- ControlOut with multiple Status stage.</li> </ul>	tcase_trfer_control
9	<p>Bit stream receiving.</p> <ul style="list-style-type: none"> <li>- Consecutive jitter equal +20ns for full-speed and +141ns for low-speed. DUT must receive packet with no error.</li> <li>- Consecutive jitter equal -20ns for full-speed and -141ns for low-speed. DUT must receive packet with no error.</li> <li>- Invalid value of two first SYNC bits. DUT must receive packet with no error.</li> <li>- Invalid duration (up 90% shrinking) of two first SYNC bits. DUT must receive packet with no error.</li> <li>- Error PID. DUT must ignore packet.</li> <li>- Error CRC5, CRC16. DUT must ignore packet.</li> <li>- Packet with stuffed last bit. DUT must receive/send packet with no error.</li> <li>- Packet with lengthened last bit by as much as 75ns for full-speed and 260ns for low-speed. DUT must receive packet with no error.</li> </ul>	tcase_bitstream
10	<p>Reply delay.</p> <p>Checking that is no error when DUT receive reply with 35 cycles delay on transaction interface.</p>	tcase_reply_delay