Core1262-868M

From Waveshare Wiki
Jump to: navigation, search

Overview

CoreSX1262-xF

(https://www.waveshare.com/core1262-868m.htm)

RPI, SPI, UART, I2C

Introduction

Core1262-868M is a LoRa core module that incorporates a new-generation SX1262 chip. It is mini and features long-range transmission and high anti-interference capability. The module uses the Sub-GHz band, and combined with the LoRa gateway, it can be connected to servers like the TTN server to build the LoRa network.

More (https://www.waveshare.com/core1262-868m.htm)

Note:

1. The product's original name is Core1262-868M, later renamed as Core1262-HF, suitable for 850~930MHz frequency band.
2. Add Core1262-LF, suitable for 410~490MHz frequency band.

Features

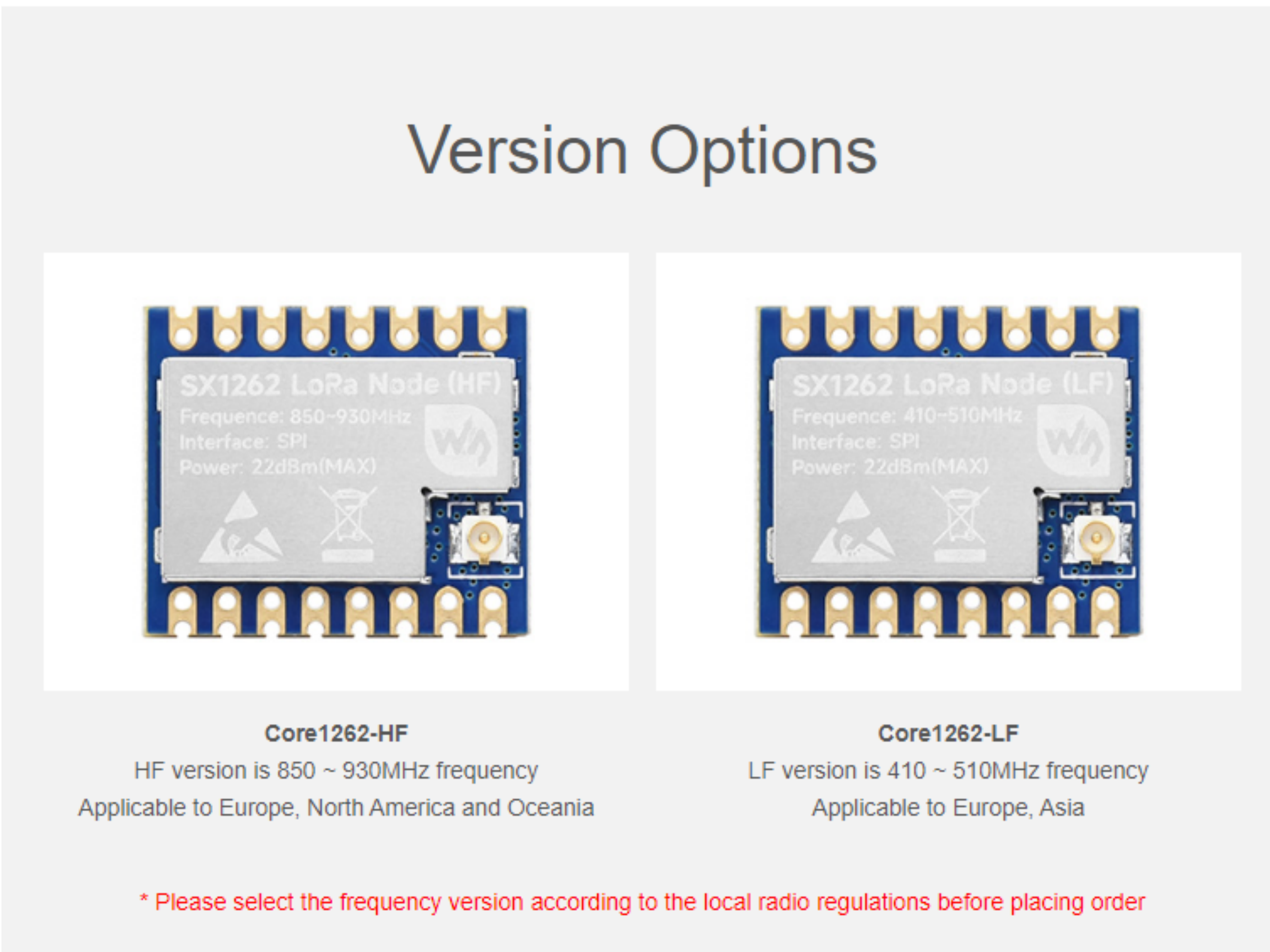
- The new generation SX1262 has higher power efficiency and longer transmission distance than the SX1278.
- Suitable for Sub-GHz band, combined with the gateway, quick connect to cloud servers to build LoRa/LoRaWAN network.
- Suitable for the application scenarios such as industry, smart home, and data acquisition.
- Adopts high-quality components such as TCXO for working stably under harsh conditions.
- Comes with online development resources and manual (examples for Raspberry Pi Pico/STM32).

Parameter

Electric	Parameter
RF Chip	SX1262

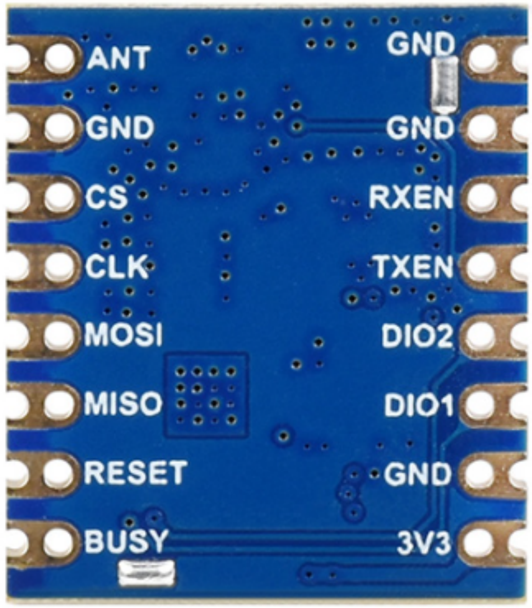
Operating Frequency	Sub-GHz: Core1262-LF: 410~490MHz Core1262-HF:850~930MHz
Modulation	LoRa/(G)FSK
Emit Power	22dBm@3.3V
Operating Voltage	3.3V
Module Current	Emitting current: 45mA@14dBm Receiving current: 5.3mA@125KHz
Communication Bus	SPI
Operating Temperature	-40 ~ 85℃
Dimensions	19.00 × 22.00mm

Version Selection



(/wiki/File:Core1262-868MF.png)

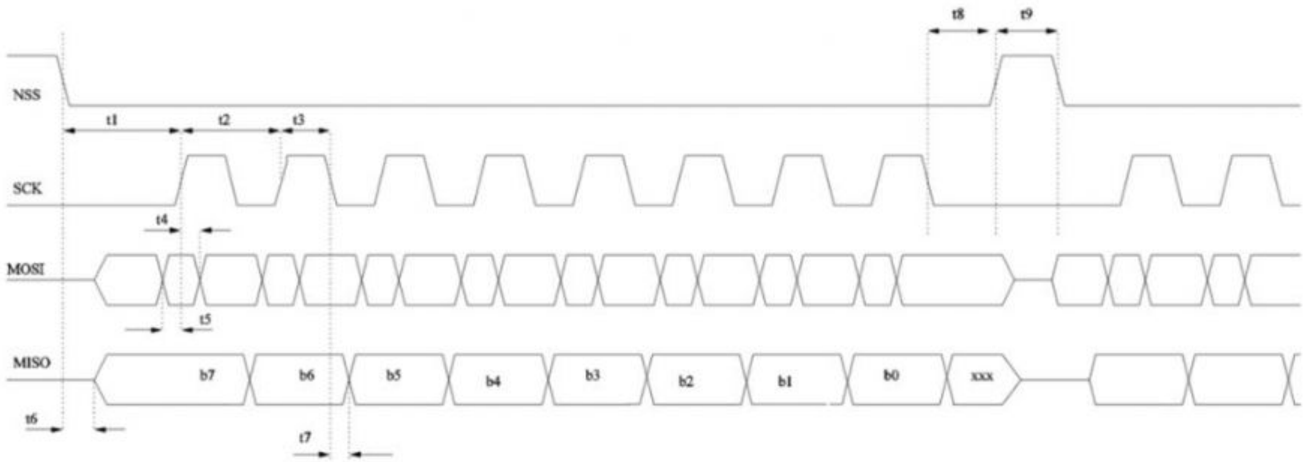
Pinout Definition



ANT	antenna	GND	ground
GND	ground	GND	ground
CS	SX1262 CS pin	RXEN	RF RX enable
CLK	SX1262 CLK pin	TXEN	RF TX enable
MOSI	SX1262 MOSI pin	DIO2	SX1262 DIO2 pin
MISO	SX1262 MISO pin	DIO1	SX1262 DIO1 pin
RESET	RESET pin	GND	ground
BUSY	SX1262 BUSY pin	3V3	power supply positive

(/wiki/File:Pinout-core.png)

- The ANT pin is an antenna pin, which can be connected to an antenna stand such as SMA when mounting the bottom board.
- CS MOSI MISO CLK is the SPI interface of SX1262, and BUSY is the status pin of SX1262.
  - Use MCU's SPI bus to communicate with Core1262-xF. When MCU reads and writes SX1262 registers, it needs to read and write parameters in the order of Opcode + Address + Data. For more information, please refer to chapters 8, 10, 11, and 12 of the datasheet (https://files.waveshare.com/upload/e/e1/DS_SX1261-2_V1.2.pdf). The maximum SPI speed is 18MHz. The communication is shown in the figure below.
-
  - When the MCU reads and writes the SX1262 register, it needs to detect the BUSY pin first. The low level indicates that it is idle and can be read and written normally, and the high level indicates that it is busy and cannot read and write the register, as shown in the figure below.



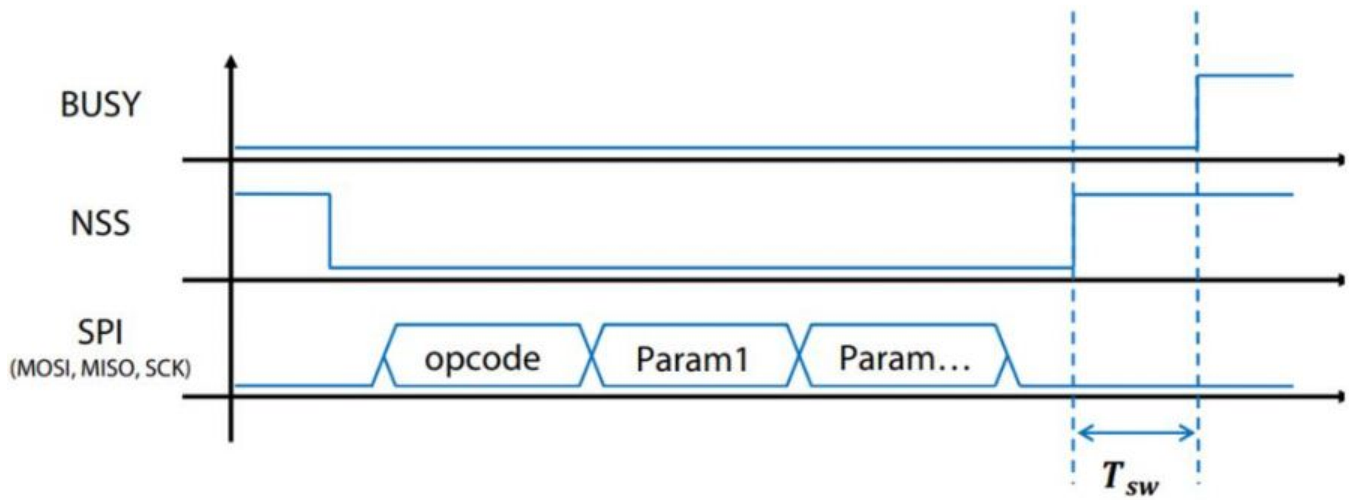


Figure 8-3: Switching Time Definition

Table 11-2: Commands to Access the Radio Registers and FIFO Buffer

Command	Opcode	Parameters	Description
WriteRegister	0x0D	address[15:0], data[0:n]	Write into one or several registers
ReadRegister	0x1D	address[15:0]	Read one or several registers
WriteBuffer	0x0E	offset, data[0:n]	Write data into the FIFO
ReadBuffer	0x1E	offset	Read data from the FIFO

(/wiki/File:Core1262-868M_pin1.jpg)

- RESET is the factory reset pin of SX1262, pull it low for 100us to restore the default parameters of the register, and keep a high level when working.
- RXEN, TXEN are RF single-pole switch (SPDT (https://files.waveshare.com/upload/c/c6/Datasheet-RTC6603SP-RichWave.pdf)) pins, RXEN low level, TXE high level, SX1262 is in receiving mode, RXEN high level, TXEN low level, SX1262 is in transmitting mode.
- DIO1, DIO2, and DIO3 are SX1262 functional GPIO pins, which can be set as input and

output to indicate various states of SX1262 (8.5 IRQ Handling in the figure below), usually, DIO1 is set as an interrupt output in the state shown in the figure below, and DIO2 is connected to RXEN Set as the control pin of the RF single-pole switch, DIO3 is set to supply power to the TCXO, for details, please refer to Datasheet (https://files.waveshare.com/upload/c/cb/DS_SX1261-2_V1.2_%281%29.pdf) 8.3.2, 8.5 summary.

8.3.2 Digital Input/Output

Any of the 3 DIOs can be selected as an output interrupt source for the application. When the application receives ar interrupt, it can determine the source by using the command *GetIrqStatus(...)*. The interrupt can then be cleared using the *ClearIrqStatus(...)* command. The Pin Description is as follows:

DIO1 is the generic IRQ line, any interrupt can be mapped to DIO1. The complete list of available IRQ can be found ir Section 8.4 "Digital Interface Status versus Chip modes" on page 54.

DIO2 has a double functionality. As DIO1, DIO2 can be used as a generic IRQ line and any IRQ can be routed through thi: pin. Also, DIO2 can be configured to drive an RF switch through the use of the command *SetDio2AsRfSwitchCtrl(...)*. In thi: mode, DIO2 will be at a logical 1 during Tx and at a logical 0 in any other mode.

DIO3 also has a double functionality and as DIO1 or DIO2, it can be used as a generic IRQ line. Also, DIO3 can be used tc automatically control a TCXO through the command *SetDio3AsTCXOCtrl(...)*. In this case, the device will automatically powe cycle the TCXO when needed.

8.5 IRQ Handling

In total there are 10 possible interrupt sources depending on the selected frame and chip mode. Each one can be enabled or masked. In addition, each one can be mapped to DIO1, DIO2 or DIO3.

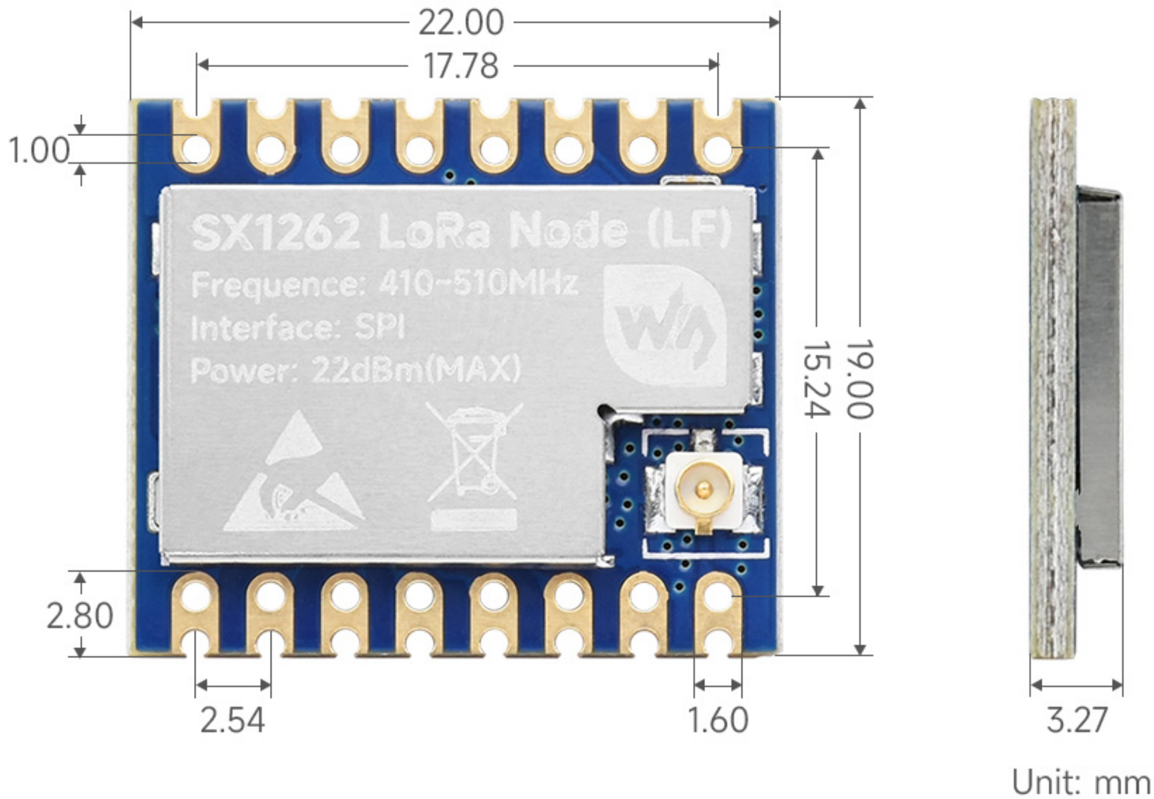
Table 8-4: IRQ Status Registers

Bit	IRQ	Description	Modulation
0	TxDone	Packet transmission completed	All
1	RxDone	Packet received	All
2	PreambleDetected	Preamble detected	All
3	SyncWordValid	Valid Sync Word detected	FSK
4	HeaderValid	Valid LoRa® Header received	LoRa®
5	HeaderErr	LoRa® Header CRC error	LoRa®
6	CrcErr	Wrong CRC received	All
7	CadDone	Channel activity detection finished	LoRa®
8	CadDetected	Channel activity detected	LoRa®
9	Timeout	Rx or Tx Timeout	All

For more information on how to setup IRQ and DIOs, refer to the function *SetDioIrqParams()* in Section 13.3.1 "SetDioIrqParams" on page 79

(/wiki/File:Core1262-868M_pin2.jpg)

Dimensions



(/wiki/File:Dimensions2.jpg)

LoRa & LoRaWAN

What is LoRa ?

Semtech (https://www.semtech.com/)'s LoRa is a long-distance, low-power wireless platform for the Internet of Things (IoT), which generally refers to radio frequency chips using LoRa technology. The main features are as follows:

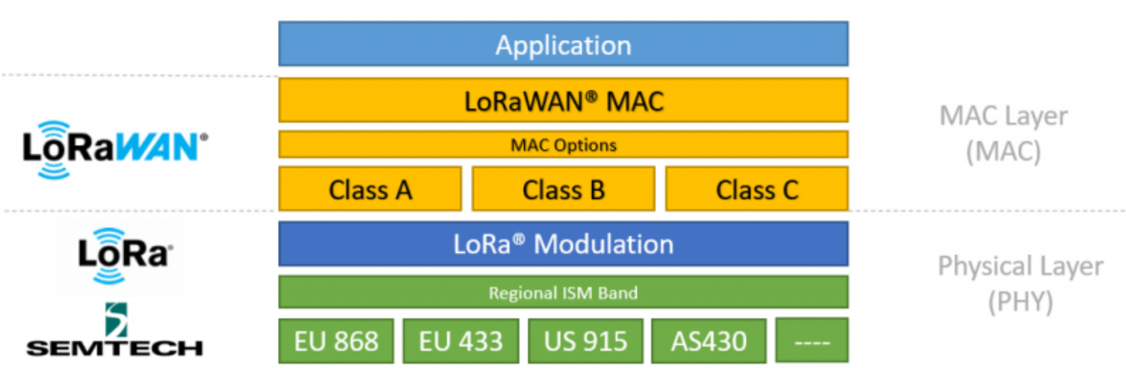
- The spread spectrum modulation technology adopted by LoRa (abbreviation of long range) is derived from Chirp Spread Spectrum (CSS) technology, which is one of the long-distance wireless transmission technology and LPWAN communication technology. Spread spectrum technology uses bandwidth for sensitivity technology, Wi-Fi, ZigBee, etc. all use spread spectrum technology, but the characteristic of LoRa modulation is that it is close to the limit of Shannon's theorem, and the sensitivity can be improved with maximum efficiency. Compared with traditional FSK technology, at the same communication rate, LoRa is more sensitive than FSK by 8 ~12dBm. At present, LoRa mainly operates in the ISM frequency band of Sub-GHz.
- LoRa technology integrates technologies such as digital spread spectrum, digital signal processing, and forward error correction coding, which greatly improves the performance of long-distance communication. LoRa's link budget is better than any other standardized

communication technology. The main factors that determine the distance in a given environment.

- LoRa RF chips mainly include SX127X series, SX126X series, SX130X series, of which SX127X, SX126X series are used for LoRa nodes, and SX130X is used for LoRa gateways. For details, please refer to Semtech (https://www.semtech.com/)'s product list.

What is LoRaWAN ?

- LoRaWAN (https://lora-alliance.org/about-lorawan/) is an open protocol for low-power wide-area networks built on LoRa radio modulation technology. Designed to wirelessly connect battery-powered "things" to the Internet in regional, national, or global networks, and target critical Internet of Things (IoT) requirements such as two-way directional communication, end-to-end security, mobility, and localized services. The node wirelessly connects to the Internet with network access authentication, which is equivalent to establishing an encrypted communication channel between the node and the server. The LoRaWAN protocol level is shown in the figure below.
  - The Class A/B/C node devices in the MAC layer basically cover all the application scenarios of the Internet of Things. The difference among them is that the time slots for nodes to send and receive are different.
  - EU868 and AS430 in the Modulation layer show that frequency band parameters are different in different countries. Please click the reference link (https://lora-alliance.org/wp-content/uploads/2019/11/rp_2-1.0.0_final_release.pdf) for regional parameters.



(/wiki/

File:SX1262-LoRa-HAT-0201.png)

- To achieve LoRaWAN network coverage in cities or other areas, it needs to be composed of four parts: node (LoRa node radio frequency chip), gateway (or base station, LoRa gateway radio frequency chip), server, and cloud, as shown in the following figure.
  - The DEVICE (node device) needs to initiate a network access request packet to the GATEWAY (gateway) and then to the server. After the authentication is passed, it can send and receive application data with the server normally.
  - GATEWAY (gateway) can communicate with the server through a wired network, 3/4/5G wireless network
  - The main operators on the server side are TTN (https://eu1.cloud.thethings.network/console/), etc. For building cloud services by yourself, please refer to lorawan-stack (http