EE6312 Advanced Analog ICs - Final Project: System Level Design

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1 Design Specifications

We are designing a system for $10bit$ resolution and $5Ksamples/s$.

2 Voltage Choices

2.1 Full-Scale and Least Significant Bit Voltages

To calculate the V_{FS}, we made the assumption that we will need at the most two overdrive voltages of headroom and two overdrive voltages to the floor. We made this assumption because we are not yet sure of our OTA topology and we did not want to limit ourselves to single stack output biasing circuitry.

To calculate V_{LSB}, we simply found the total number of quantization levels (2^{10}) and found the difference between each level based on the V_{FS} at the output.

2.2 Common-Mode Voltage

We chose our V_{CM} to be half the supply voltage of $1.8V$.

3 Switched-Capacitor Input Stage

3.1 Capacitor Sizing

We used the below expressions to calculate our C_{min} value. Since there are four capacitors in parallel, when doing noise analysis we can consider them as 1 capacitor of value $4C_{samp}$. This limit is based on the noise specification of the system. Based on our value for C_{min}, we chose a reasonable value for C_{hold} and C_{sample}.

$$C_{min} = kT/\overline{V_{RMS}^2} \tag{1}$$

where $\overline{V_{RMS}^2} = \frac{kT}{C} = \frac{V_{LSB}^2}{24}$.

3.2 Transfer Function

At the beginning of the sample phase, the charge at the summing node is given by the below expression.

$$Q_{samp+} = 4C\left(V_{in+} - V_{CM}\right) \tag{2}$$

$$Q_{samp-} = 4C\left(V_{in-} - V_{CM}\right) \tag{3}$$

Then, during the hold phase, all of the charge will go onto the hold capacitor because the OTA forces the summing node to V_{CM} while the other other sides of the caps are brought to V_{CM} as well by the ideal source and closed hold switches.

$$Q_{hold+} = C\left(V_{out+} - V_{CM}\right) \tag{4}$$

$$Q_{hold-} = C\left(V_{out-} - V_{CM}\right) \tag{5}$$

Using the law of charge conservation, we can equate the hold and sample phase capacitor charges.

$$Q_{hold+} = Q_{samp+} \tag{6}$$

$$\left(V_{out+} - V_{CM}\right) = 4\left(V_{in+} - V_{CM}\right) \tag{7}$$

$$Q_{hold-} = Q_{samp-} \tag{8}$$

$$\left(V_{out-} - V_{CM}\right) = 4\left(V_{in-} - V_{CM}\right) \tag{9}$$

Subtracting the two expressions, we get a transfer function of the differential input and output voltages.

$$\left(V_{out+} - V_{out-}\right) = 4\left(V_{in+} - V_{in-}\right) \tag{10}$$

3.3 Maximum Resistance

To find the maximum resistance we could tolerate, we first found the minimum frequency of the non-dominant pole (caused by RC feedback network). To do this, we first estimated the unity gain frequency of our system using $f_{unity} = \frac{g_m}{2\pi C_{hold}}$. Using this value, we estimated the non-dominant pole location by scaling f_{unity} up by a factor of 1.7 to achieve the phase margin we chose (see Table 1). Using the below expression we then found the maximum value of resistance.

$$R_{max} = \frac{1}{2\pi f_{p2} C} \tag{11}$$

3.4 MOSFET Sizing

We decided to use complimentary pass transistor switches and to size the pMOS and nMOS the same. The reason for this is that the charge injection is cancelled between the devices and we can recover the delay cause by the PMOS by increasing the pMOS and nMOS widths together. Note that we used minimum length devices because this has a positive effect on both speed and accuracy. With our R_{max} value, we were able to calculate the necessary $\frac{W}{L}$ ratios using the below expression derived from the parallel combination of R_{on-p} and R_{on-n}.

$$R_{max} = \frac{1}{(\mu_n + \mu_p) C_{ox} \frac{W}{L} (V_{CM} - V_{in} - V_T)} \tag{12}$$

4 OTA Parameters

4.1 DC-Gain

Using the settling constraint and the below expression, we determined a necessary value of the OTA's open-loop gain.

$$\frac{V_{error}}{V_{in}} = \frac{1}{A_{DC}\beta} \tag{13}$$

4.2 Bandwidth

Using the above gain and the unity gain frequency, we were able to calculate a value for our open loop f_{3dB}.

4.3 Phase Margin

We chose a minimum phase margin of 60^o.

4.4 Slewing

We found the slew rate by taking the maximum slope of a sine wave at f_{3dB}. From this value, we were able to use the below expression to calculate the minimum value of I_{slew}.

$$SlewRate = \frac{I_{slew}}{C_{hold}} \tag{14}$$

5 Figures & Tables

Parameter	**Required Value**
Sample Rate	$5Ksamples/s$
Resolution	$10bit$
V_{FS}	$1.0V$ at the output, $0.25V$ at the input
V_{LSB}	$977\mu V$
V_{DD}	$1.8V$
V_{CM}	$0.9V$
C_{min}	$104fF$
C_{hold} & C_{sample}	$110fF$
Phase Margin	60^o
f_{unity}	$1.44GHz$
R_{max}	588Ω
$\frac{W}{L}_n$ & $\frac{W}{L}_p$	10.34
A_{DC}	$84.29dB$
f_{3dB}	$1.44GHz$

Table 1: Specifications for the System Level Components and OTA

6 MATLAB Code

Most of the calculations were performed using the following MATLAB Code.

```
%%% This document is for the EE6312 Propject. It calculates the capacitor
%%% sizes for the hold and sample capacitors.

%%
clear all
close all

N = 10; % Numbers of bits we are using;
V_DD = 1.8;%V
V_ov = .2; %V Basic asumption

V_cm = V_DD/2;

V_FS = (V_DD -(2*V_ov) - (2*V_ov)); % Take off 2 V_ov for
    % output swing at both the top and bottom. Divide by ideal gain for
    % input V_FS.
%V_FS = 1;

V_LSB = V_FS/(2^N);

V_N_RMS_squared_max = V_LSB^2/24;

k = 1.3806488e-23;
T = 300;%K

C_min = k*T/V_N_RMS_squared_max;

 % Settling Constraints
settle_voltage_error = V_LSB/4;
percent_error = 1-(4*V_FS - settle_voltage_error)/(4*V_FS);
t_over_tau = -log(percent_error);
f_s = 5e3;
T_s = 1/f_s;
tau = (T_s/2)/t_over_tau;

f_3db = 1/(2*pi*tau);

 % From calculate C_min
 C = 110e-15;
 R_max = tau/C;

 % Info on transistors
 beta_p = 2*35.5e-6;%A/V^2
 beta_n = 2*170.1e-6;%A/V^2
 t_ox = 4.1e-9;
 epsilon_ox = 3.9*8.854e-12;%F/m
 C_ox = epsilon_ox/t_ox;

 rel_sizing = beta_n/beta_p;
 W_over_L = 1.5; %Minimum for Minimum L
```

```
r_o = 1/(beta_n/2*(W_over_L)*V_ov);
L = 180e-9;%m
W_n = W_over_L*L;
W_p = W_n*rel_sizing;

% Charge Injection
V_Tn = 0.5;%V
V_Tp = 0.5;%V
V_ov_n = V_DD - V_Tn - V_cm;
V_ov_p = -V_Tp + V_cm;

Q_channel_n = -C_ox*W_n*L*V_ov_n;
Q_channel_p = C_ox*W_p*L*V_ov_p;

delta_Q = Q_channel_p + Q_channel_n;

% At the end of the phi_S phase
%delta_Q_switch_side =

% Bandwidth Calculations from Settling Requirements
A_f = (4*V_FS - settle_voltage_error)/V_FS;
%A_f = (4*V_FS - V_LSB)/V_FS;
beta_f = 1/4;
DC_gain = A_f/(1-A_f*beta_f);
DC_gain_dB = 20*log10(DC_gain);

DC_gain_miles = (V_FS*4/settle_voltage_error);
DC_gain_miles_dB = 20*log10(DC_gain_miles);

g_m = 1e-3;
w_unity = g_m/C;
f_unity = w_unity/(2*pi);
f_p2 = 1.7*f_unity;
w_p2 = 2*pi*f_p2;
f_3dB_pole = f_unity/(DC_gain_miles);
w_3dB_pole = 2*pi*f_3dB_pole;

slew_rate = 4*V_FS*w_3dB_pole;
I_slew = slew_rate*C;

%Redo Switch Sizing
R_max2 = 1/(w_p2*C);

W_over_L_min = 1/(R_max2*(beta_n+beta_p)*V_ov_n);
```