A Switched-Capacitor Amplifier for Use in a 2.5bit/stage Pipelined Analog-to-Digital Converter

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***Abstract*—A switched-capacitor amplifier with a nominal gain of 4 was designed for use in a 2.5 bit/stage pipelined analog-to-digital converter (ADC). The total resolution of the ADC was 10 bits. The sample rate of the ADC was $5kS/s$. The amplifier consisted of 4 sample capacitors and 1 hold capacitor in feedback around an operational transconductance amplifier (OTA). The OTA consisted of a pMOS-input folded cascode stage followed by an nMOS common source stage. The open loop DC gain of the OTA was $110.9dB$. The unity gain bandwidth of the OTA was $87.1kHz$. The circuit consumed MAKE THIS MORE ACCURATE $725nW$ of DC power. SOMETHING ABOUT EFFECTIVE NUMBER OF BITS. SOMETHING ABOUT FIGURE OF MERIT.**

***Index Terms*—switched-capacitor amplifier, pipelined analog-to-digital converter**

I. Introduction

PIPELINED 2.5 bit/stage ADCs require accurate

II. System Level Design

A. Top Level Schematic

B. Sample and Hold Capacitors

C. Switches

III. Transistor Level OTA Design

A. Gain Stage

B. Biasing

C. Component Values

IV. Open Loop OTA Results

Upon completion of our OTA design, we performed various open-loop simulations to verify that we had met our required specifications.

A. Open Loop Differential Frequency Response

Keeping the entire switch capacitor system in perspective, the most important specs for us to hit were those for differential gain for total accuracy and unity-gain bandwidth (UGB) for total speed. Therefore, we measured those performance values for our OTA first. As can be seen in our differential gain plot (Figure 1), we successfully hit our specs for gain and UGB across all three PVT corners (see Table III). The plot also shows that we were able to use compensation capacitance to push our dominant pole to a very low frequency ($\approx 0.1Hz$).

We also plotted the phase response of our open loop OTA (see Figure 2). From this plot, the low frequency pole seen in the gain response is confirmed. In addition, it can clearly be seen that the additional poles and the zero created by the compensation capacitor has been pushed out beyond our unity-gain bandwidth. Our phase margin measurements are shown to be very consistent across PVT corners and all above our spec (see Figure III).

B. Open Loop Common Frequency Mode Response

In order for our OTA to be robust against common-mode noise, it is important for the common mode gain to remain very low across all frequencies. As can be seen in our plots for common mode gain (Figure 3) and common mode phase (Figure 4), common mode changes on the input have a very limited effect on the output.

C. Common Mode Feedback Frequency Response

Our goal in developing a common mode feedback (CMFB) network was to provide circuitry to hold our output node at V_{CM}. To ensure that our circuit was functioning as we intended, we broke our feedback loop at the input of the CMFB network and stimulated the circuit with a small signal source. We then measured the output of the CMFB circuit at the node that feeds back to our cascade branch. Our results can be seen in figures 5 and 6.

V. Closed Loop Amplifier Results

After we verified that we had met our open loop OTA specifications, we replaced the ideal OTA in our system level design with our own OTA design to verify that we still met the system level specifications.

A. Nyquist Rate Sinusoidal Transient Response

The first test we ran on our system was a sine wave input at our full-scale amplitude and the Nyquist frequency. As can be seen in our plot (Figure 7), our system samples the input at the end of the sample phase to be $0.35V$ (V_{FS}). Over the course of the hold phase, the output slews and then settles linearly to a value of $1.402V$. This is within our maximum error value (shown below) and shows that our circuit successfully handles a sine wave input. The maximum input referred error we can tolerate is

$$4 * \frac{V_{LSB}}{2} = 5.4mV \tag{1}$$

B. Small Step Transient Response

The second test we performed on our closed loop system was a small step input. As can be seen in figure 8, our output shows a fast settling with little to no slewing. We provided an input step of $2mV$ and observed the output to settle to $8.012mV$ at the end of the hold phase. This is well within our spec for error so this test was successful.

C. Full Scale Step Transient Response

The third test we performed on our closed loop system was a step input at the full-scale voltage. The results of this test closely resembled those of the sine wave input. The reason for this is that the input is again sampled at the full-scale voltage and the output settles accordingly. This test was successful.

D. Sawtooth Transient Response

The fourth and final test we performed on our closed loop system was a sawtooth input at $f_s/20$. As can be seen from our plot in figure 10, our system has no problem settling to the correct output for small changes in the input (along the ramp of the sawtooth). In addition, our output settles to the correct output in time after the edge of the sawtooth when the input drops from the full-scale voltage to the negative full-scale voltage.

E. Effective Number of Bits

F. Figure of Merit

We calculated our figure of merit based on both the DC power consumption of our system as well as the average overall power of our system. Both values of power are shown in table III and the FOM values are shown below.

$$FOM_{DC-POWER} = \frac{Power_{dc}}{2^{ENOB} f_s} = 150.3fJ \quad (2)$$

$$FOM_{TOTAL-POWER} = \frac{Power_{total}}{2^{ENOB} f_s} = 441.4fJ \quad (3)$$

G. Area

With the functionality of our system verified and its performance measured, we made an estimation of the area of our design. To measure the area of the transistors in the design, we used the below formula where $L_{diff} = 0.48\mu m$ and $\alpha = 1.3$.

$$Area_{transistors} = W * (L + L_{diff}) * \alpha = 55.50pm^2 \quad (4)$$

To calculate the area of the capacitors in our circuit, we used the below formula across all of our capacitors where $C_{unit-area} = 1fF/\mu m^2$.

$$Area_{capacitors} = \sum C/C_{unit-area} = 3.00nm^2 \quad (5)$$

Finally, to calculate the area of the resistors in our circuit, we used the below formula across all of the resistors in our design where $R_s = 10\Omega/\mu m^2$.

$$Area_{resistors} = \sum R/R_s = 8.00\mu m^2 \quad (6)$$

Adding the above results for area, we came to a total area estimation as shown below.

$$Area_{total} = 8.0036\mu m^2 \quad (7)$$

VI. Summary of Results

As can be gathered from our numerical results, we successfully reached the goal we set out to accomplish. We designed a $10bit$, $5ksample/s$ amplifier for use in a $2.5bit/stage$ pipelined analog-to-digital converter which settles to an input referred error value less than $\frac{V_{LSB}}{2}$. In the process of designing this amplifier, we were able to maintain a very low value of total power consumption and as a result, a very respectable figure of merit. Thanks to a well thought out design process, we built and amplifier that not only meets its specs, but also maintains those specs over all PVT corners. If this design was put onto silicon and distributed to customers, we believe that it would prove to be robust enough to handle constant unpredictable use.

VII. Possible Improvements

While most of the specifications of our finished amplifier are impressive, one that needs optimization is the total area. Because we originally set out to meet a more stringent specification for gain, we were forced to utilize two 40Ω resistors in the CMFB circuit. These two resistors account for the vast majority of the design's area. Because we ultimately were able to attain a gain far greater than the requirement, in future optimizations of the design we would focus on bringing the value (and hence size) of these resistors down to a more reasonable value. In addition, we believe that with redesign of the OTA, we can achieve a much lower power consumption and utilize much smaller compensation capacitors.

VIII. Conclusion

Through the design of this amplifier, we were able to attain a good deal of knowledge on new circuit techniques as well as design process. Unlike some of our previous designs, we spent a very long time developing our ideas on paper until we were satisfied that they would give us the results we were looking for. Thanks to this patience, once we put our theories into simulation, we were very pleased with the results. We were able to hit our spec after the first iteration of design and we spent most of the remaining design time optimizing for power and accuracy. This project is quite appropriate for the class because it allows a broad range of students with different backgrounds to show interest. Because the design requires some knowledge of digital theory in addition to the heavy analog theory, a strong need for collaboration was instilled and led to a much more organic learning environment.

IX. Seminar Responses: Miles Sherman

A. Simone Gambini: More Than Moore Systems

Dr. Gambini gave an informative and interesting perspective on his work and the industry as a whole. While I was previously aware of a good amount of "More Than Moore" work being done, getting a feel for some specific projects was helpful for my understanding. The one aspect of this seminar that stuck with me was the fact that the noise associated with actually stimulating brain activity is actually larger than the brain's signal poses an interesting problem and a demand for a solution. There is definitely a lot of room for major development in this field.

B. Adad Abidi: Armstrong's Circuits & The Worldwide Spread of Radio

Of the three seminars I attended this semester, I would say this one was the most interesting for me. Dr. Abidi presented the work of Edwin Armstrong in a very specific way so as to motivate a connection between the work of the 1920's and the analog design of today. Armstrong's circuits played a major role in influencing the way we communicate today and it is clear when his fundamental designs are found in the large systems of analog communication chips in modern day devices. Armstrong's main focus in his work seems to be resourcefulness since vacuum tubes were so expensive. Modern day engineers can learn a lot from his work. Even though transistors are a commodity now, there is always optimization to be done.

C. Shanthi Pavan: Continuous-Time Delta Sigma Data Converters

This was the final lecture I attended and I probably had the most trouble following this one due to its more in depth technical discussion of a new topic for me. Dr. Pavan discussed new techniques for the elimination of clock-jitter and non-linearities in delta sigma converters. While I could not follow his exact method of innovation, I was certainly able to learn a good amount about the operation of delta sigma converters. These systems operate by oversampling the input at sampling rates much higher than those at the final output of the system. By doing this, the system can then modulate the noise and push it to higher frequencies than those of interest. The signal is then re-sampled and outputted.

TABLE I
PASSIVE COMPONENT VALUES

Component	Value
Resistors	Ω
Capacitors	F

TABLE II
TRANSISTOR SIZINGS

Transistor	Width (m)	Length (m)	Aspect Ratio

TABLE III
SUMMARY OF SPECIFICATIONS AND RESULTS

Specification	Specification Value	FF Result	TT Result	SS Result
Open Loop OTA DC Gain	$72.20dB$	$102.38dB$	$110.86dB$	$112.57dB$
Open Loop OTA Phase Margin	60^o	75.4^o	75.2^o	74.3^o
Open Loop OTA Unity Gain Bandwidth	$44.10kHz$	$96.93kHz$	$87.34kHz$	$68.83kHz$
DC Power Consumption	–	$747.90nW$	$769.50nW$	$803.16nW$
Overall Power Consumption	–	–	$2.26\mu W$	–
DC Figure of Merit	–	–	$150.3fJ$	–
Overall Figure of Merit	–	–	$441.4fJ$	–
Overall Area	–	–	$8.0036\mu m^2$	–

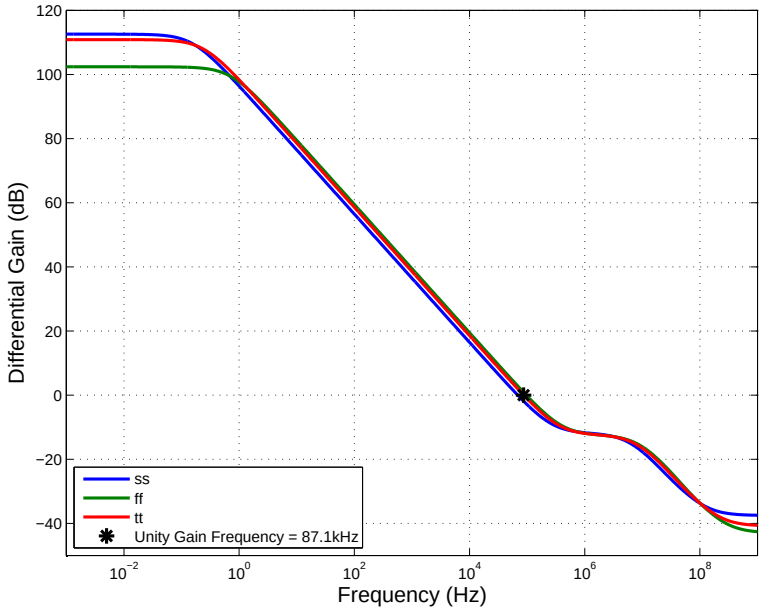

Fig. 1. The open loop differential gain magnitude response of the OTA.

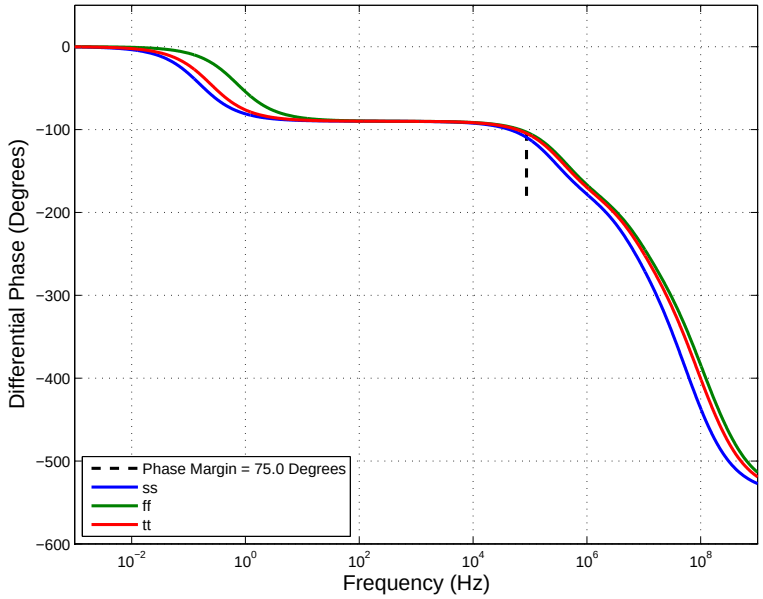

Fig. 2. The open loop differential gain phase response of the OTA.

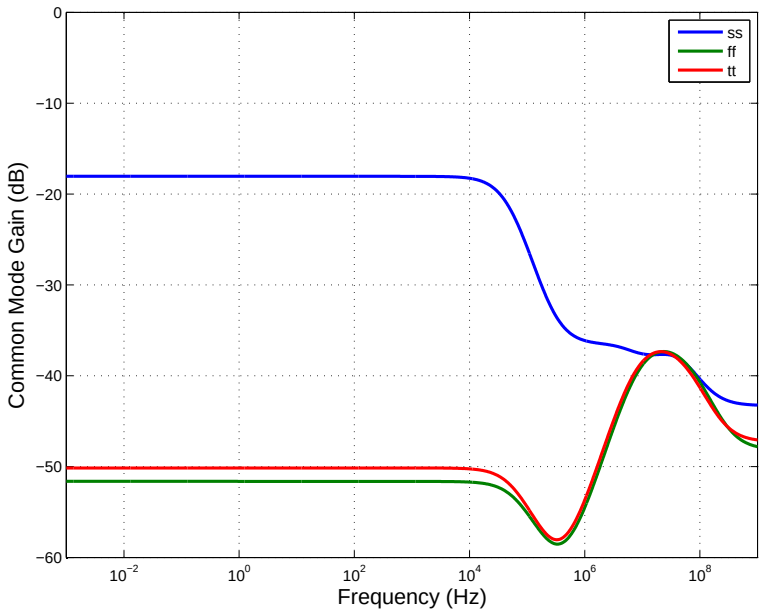

Fig. 3. The open loop common mode gain magnitude response of the OTA.

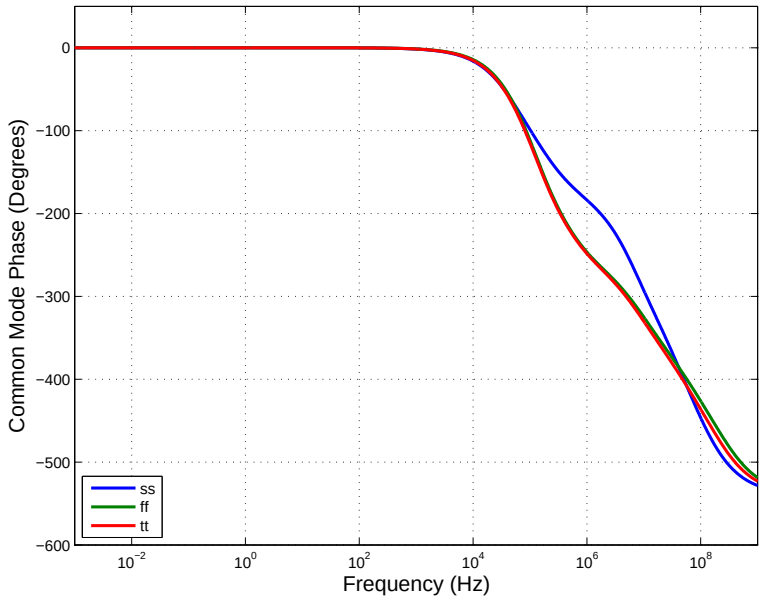

Fig. 4. The open loop common mode gain phase response of the OTA.

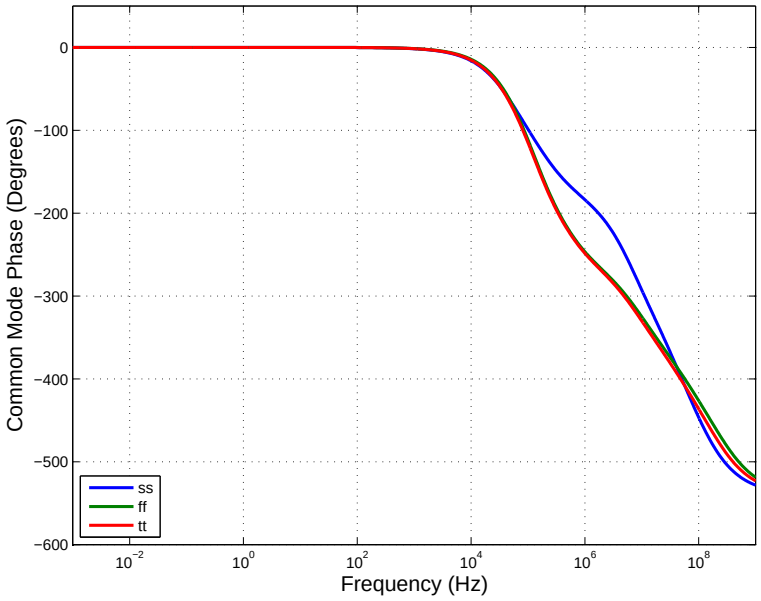

Fig. 5. The common mode feedback network gain phase response.

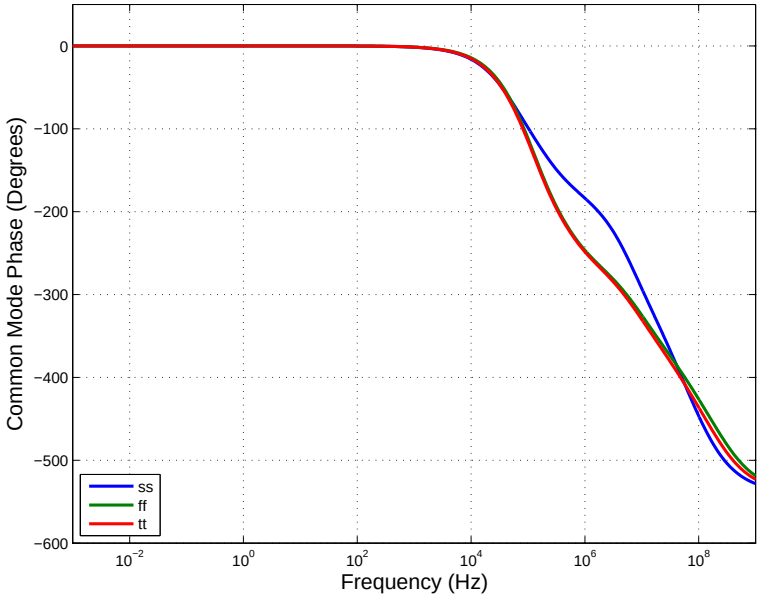

Fig. 6. The common mode feedback network gain magnitude response.

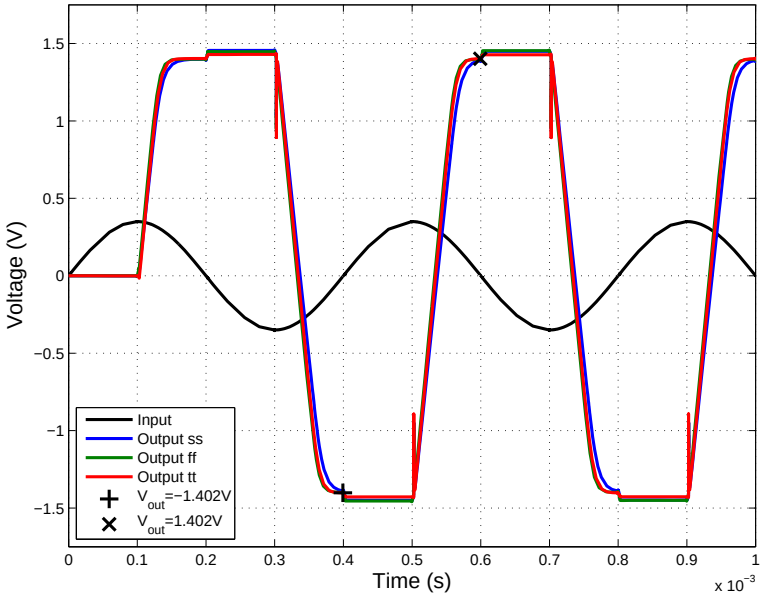

Fig. 7. The closed loop transient response to a full-scale amplitude sinusoid at the Nyquist frequency.

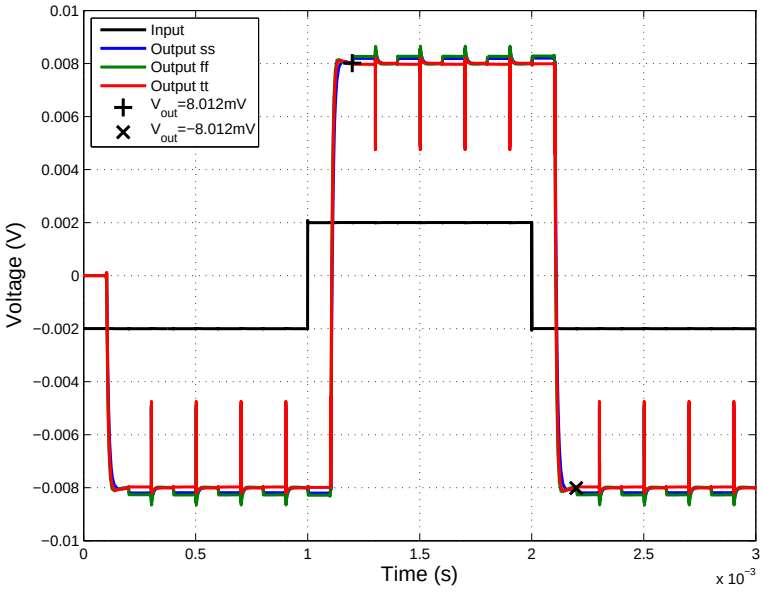

Fig. 8. The closed loop transient response to a small amplitude step input.

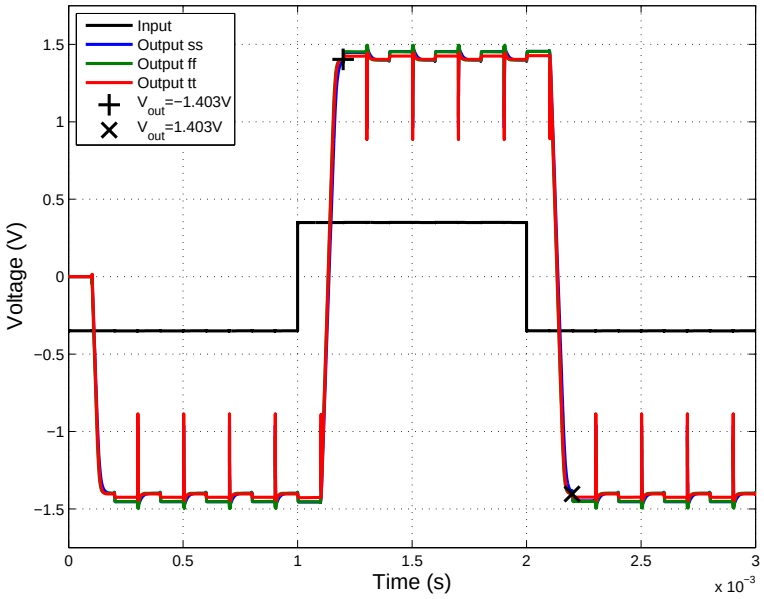

Fig. 9. The closed loop transient response to a full-scale amplitude step input.

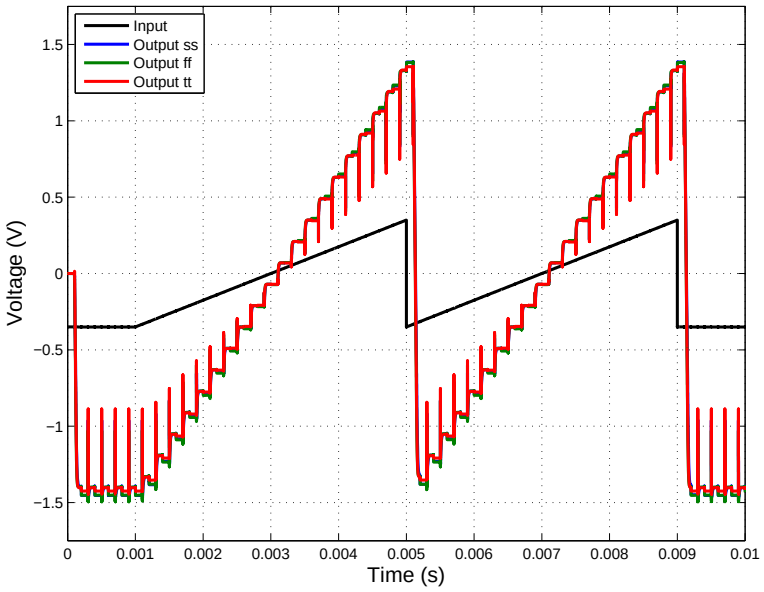

Fig. 10. The closed loop transient response to a full-scale amplitude sawtooth with a frequency of $\frac{f_s}{20}$.