EE6312 Design Project

Spring 2013

The goal of this project is to design a fully differential switched capacitor amplifier including the OTA, MOS switches and capacitors.

Background

The project assignment is inspired by the design of amplifiers for pipelined analog-to-digital converters. It is not strictly necessary to understand the background material in detail, but a brief description is provided here to put the project in a broader context.

Each stage in the pipeline does a coarse A/D conversion to determine the partial digital output X and computes the residue voltage, v_{out}, to be processed by later stages. A basic block diagram of a stage in a 2.5bit/stage pipelined A/D converter is shown in Fig. 1(a). The residue v_{out} is computed as $4 \cdot v_{in} - X \cdot V_{REF}$ in the analog domain, where $X = \{\pm 3, \pm 2, \pm 1, 0\}$.

In modern implementations, the entire circuit (and hence the OTA) is fully differential. There are many different implementations of the dashed area - each having its own advantages w.r.t. sampling, charge injection, parasitics, offset etc.

For your own understanding, you might consider first analyzing the block diagram (Fig. 1(a)) and see for yourself how a pipelined A/D works. Due to the amplification in each stage, the accuracy of the complete A/D converter is strongly dependent on the accuracy of the first and second stage, in particular on the accuracy of the dashed area of the first stage of the pipelined converter.

References

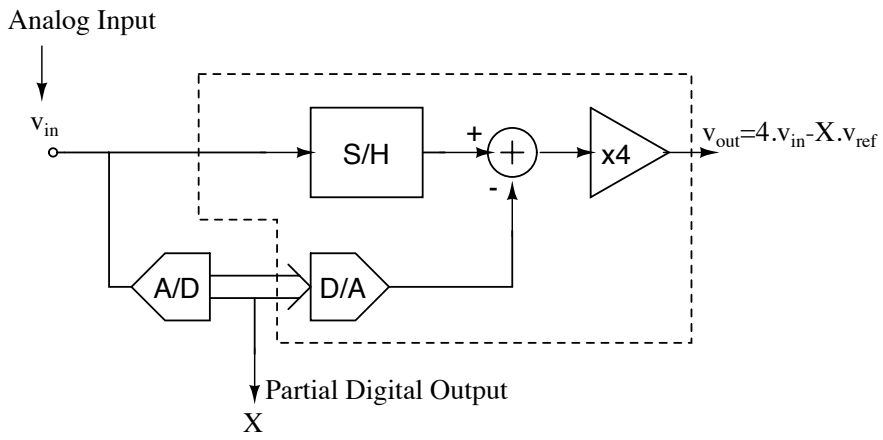
For further reading on pipelined A/D Converters, or to get a clear understanding, please refer to the following papers:

1. "A pipelined 5-Msample/s 9-bit analog-to-digital converter," S. H. Lewis & Paul Gray: IEEE Journal of Solid-State Circuits Dec. 1987

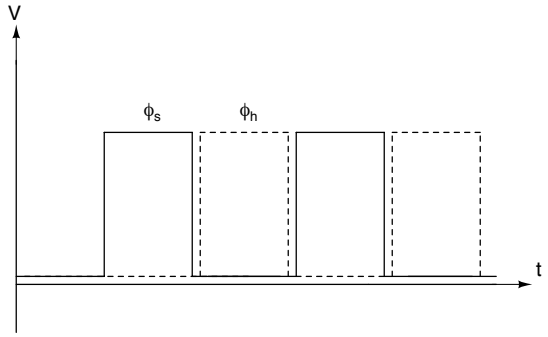
2. "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," Song, Tompsett & Lakshmikumar: IEEE Journal of Solid-State Circuits Dec. 1988

3. You can also refer to Johns and Martin, Analog Integrated Circuit Design (Second Edition), Chapter/Section 17.4 and 17.6 for a very brief introduction on pipelined ADCs.

4. For fundamentals on A/D conversion, definitions etc, refer to Johns and Martin, Analog Integrated Circuit Design (Second Edition), Chapter 15.



(a)



(b)

Figure 1: Background (a) Block diagram of a stage in a pipelined ADC (b) Sample and Hold Clock Phases

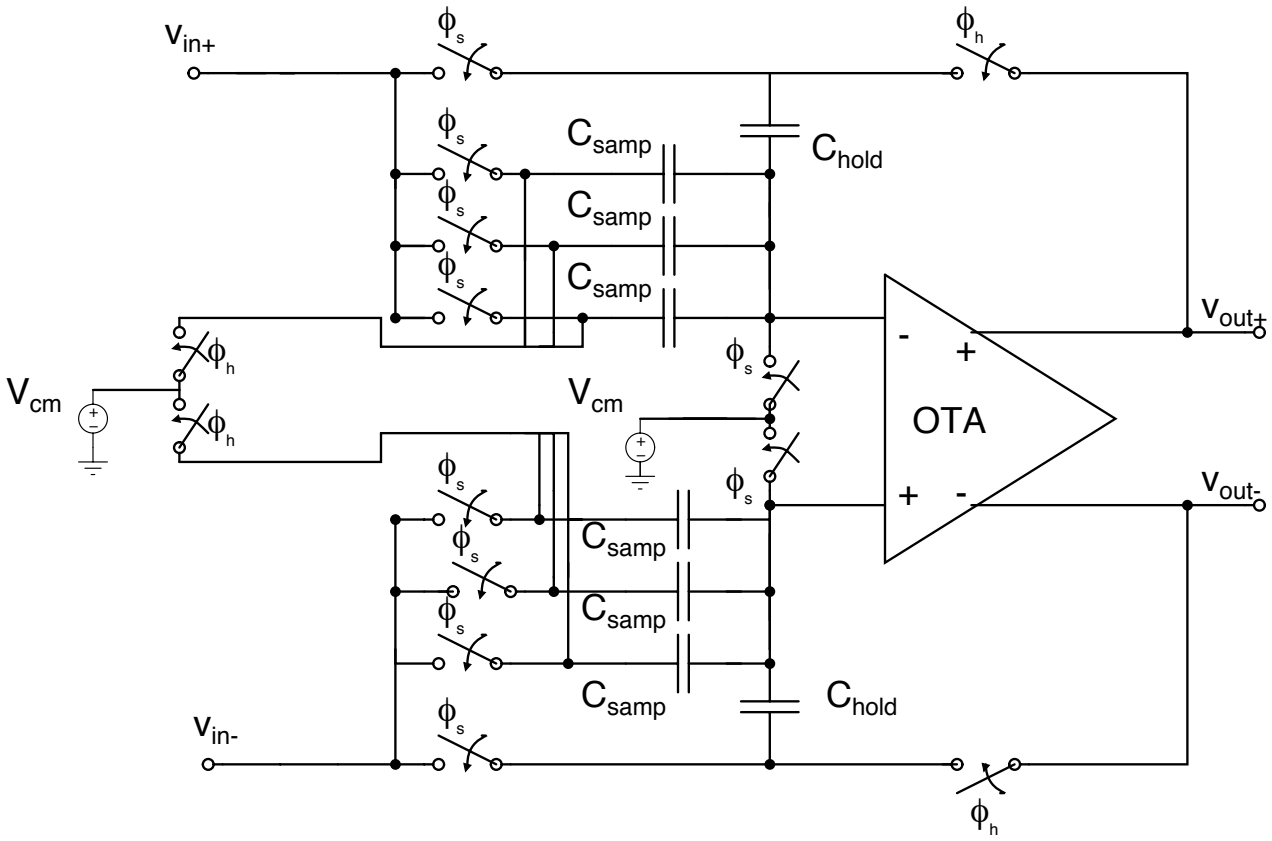


Figure 2: Circuit to be designed in this project: Fully differential switched capacitor sample-and-hold amplifier with a nominal gain of 4, $C_{samp} = C_{hold}$

Project Design Goal

Design the fully differential switched-capacitor sample-and-hold amplifier with a nominal gain of 4 shown in Fig. 2. **Assume $C_{samp} = C_{hold}$. Minimize the power consumption while meeting all the design specifications for typical process and operating conditions.** Each group will have its own set of speed and accuracy design specifications.

Groups

You should form groups of 2 students who collaborate on the project. An appropriate number of combinations of the sampling speed and number of bits will be made available for each group to choose.

Discussion with others is encouraged but genuine design work from each group is required. All sources used need to be properly referenced or acknowledged in your research report. Make sure to interact regularly with the TA during office hours on your progress, ideas and challenges.

Process and Typical Operating Conditions

- Nominal V_{DD}: 1.8 V.
- Nominal Temperature: 300 K.
- Nominal Process: TSMC018 Teaching model – tt corner. The model file is available under `http://www.ee.columbia.edu/~kinget/TOOLS/TSMC018_teaching.scs`.

PVT Simulations

Your design only needs to meet all specifications for typical process and operating conditions. But in addition you need to do all simulations in the following three cases and show the performance of your design against the given specifications:

- Typical case: tt (typical corner), Temp=27°C and VDD=1.8V.
- Worst case: ss (slow corner), Temp=100°C, VDD=1.6V.
- Best case: ff (fast corner), Temp=0°C, VDD=2V.

Variations in performance across PVT (process, voltage, temperature) are to be expected, but if your design exhibits substantial variation, you should verify.

Deadlines and Deliverables

The project is split in 4 steps:

1. System-Level Design (Switched-Capacitor Input Stage & OTA Parameters): April 15th.
   Design Review: April 18th.
2. OTA Transistor-Level Design: April 22th.
   Design Review: April 25th.
3. Complete Stage : April 29th.
   Design Review: May 2nd.

4. Complete Stage and Final Report Submission: **May 6th - Time: 1:00pm.**
   Design Review: **May 6th - Time: 4:00pm.**

After every step, it is recommended that you characterize and document your design for the design review. The documentation should include

- Transistor level schematics of the design. Tabulate all the component values and transistor sizes.
- Top-level schematic for all test setups. Create a symbol for your OTA and then create top-level test benches.
- Simulation plots for typical operation.
- Simulation results in a table for all three corners.

There will be design review sessions for the first three stages of the project on April 18th, April 25th, May 2nd. Each group must come to office hours to discuss their design with the assigned TA for their project. The grading is based on the every stage of the project. Each design review carries a grade of **10 points**.

The final report carries **70 points**. Final design review will be on May 6th after the class time (starting at 4:00pm). Project report/files for the final submission must be submitted through CourseWorks. Please follow the instructions (below) for the final report exactly.

The deadline for final submission is fixed and will not be changed.

Figure of Merit

For the final report, you need to normalize your power consumption for operating speed and accuracy by computing the figure of merit (FOM) of your design given by: $FOM = \frac{Power}{2^{ENOB} f_s}$, where f_s is the sampling speed; the effective number of bits, $ENOB$, is defined as $\frac{SINAD-1.76}{6.02}$ where $SINAD$ is the maximum signal-to-noise-and-distortion ratio measured with a full scale sinusoidal input.

By normalizing the performance with a figure of merit, the performance of different designs can be compared. In particular the figure of merit assumes that doubling the sampling speed should result in doubling of power. Similarly, increasing the number of bits by 1, i.e. improving the $SINAD$ by 6 dB, should require twice the amount of power. This is a generally used figure of merit in the literature, however, there are limitations as to how accurate or applicable some of the design normalization assumptions are.

For ease of calculation, you can plug in the number of bits specified for your team in the FOM equation as ENOB.

Extra Credit [5 points]: Do a transient or PSS simulation of your sample and hold using a full scale sinusoidal input with a frequency close to the Nyquist frequency and determine the ENOB from the output spectrum; ENOB is defined as $\frac{SINAD-1.76}{6.02}$ where $SINAD$ is the maximum signal-to-noise-and-distortion ratio.

Final Report

- For your report, please arrange all simulation plots and tabular results in one PDF file, briefly explain/comment when appropriate. Cadence plots and schematics usually do not look clear on reports. You should use xcircuit for making schematics and matlab for plotting. Do not print pages of simulations and schematics, but rather select the key simulations to show and extract key performance metrics and organize them.
- Performance summary of the individual blocks and overall design in a datasheet. Tabulate performance parameters (DC gain, phase margin and bandwidth of the fully differential OTA and FOM, power consumption of the overall design etc.) for each corner.
- Estimate and report the area of the fully differential switched capacitor sample-and-hold amplifier you design. Use the following formulas for the area calculations. For transistors area estimation use $W * (L + L_{diff}) * \alpha$, where $L_{diff} = 0.48\mu m$ is the length of drain or source diffusion and $\alpha = 1.3$ to

account for wiring sizes. Assume a unit capacitance of $C_{unit-area} = 1fF/\mu m^2$ and use $C/C_{unit-area}$ for the capacitor area estimations. Assume a unit resistance of $R_s = 10\Omega/\mu m^2$ and use R/R_s for the resistor area estimations.

- For the OTA design, you need to submit the following simulation results:
  1. Differential frequency response of OTA indicating DC gain, bandwidth and phase margin.
  2. Common mode frequency response of OTA.
- For the overall design including the OTA, capacitors and switches, you need to submit the following simulation results:
  1. Transient simulations to prove the 4x amplification happens with the right accuracy; show that you have enough settling time, etc.
  2. Transient simulations for a small signal step at the input, going from V_{LSB} to $-V_{LSB}$ and back to V_{LSB}.
  3. Transient simulations for a sawtooth ramp with a period of Tclk/20, covering the full-scale input range of the design $[-V_{FS}, V_{FS}]$.
  4. Transient simulations for a large signal step at the input, going from V_{FS} to $-V_{FS}$ and back to V_{FS}.

You need to hand in a **clear** report. It should allow the educated reader to understand how the design was performed. The report needs to focus on the design procedure that you followed. Make sure to include the trade-offs considered, steps taken to optimize power consumption, reason for the choice of circuit topology etc. You are not graded based only on the performance of your design, but also on explaining what design techniques you used to achieve the reported results or what design challenges limited you from further improving the performance.

The length of the report should not exceed **6 pages** (not including figures/ tables). It should contain all circuit schematics, mention sizes of all components and include important simulation plots. The figures and the tables should be at the end of the report, and large enough so everything is readable.

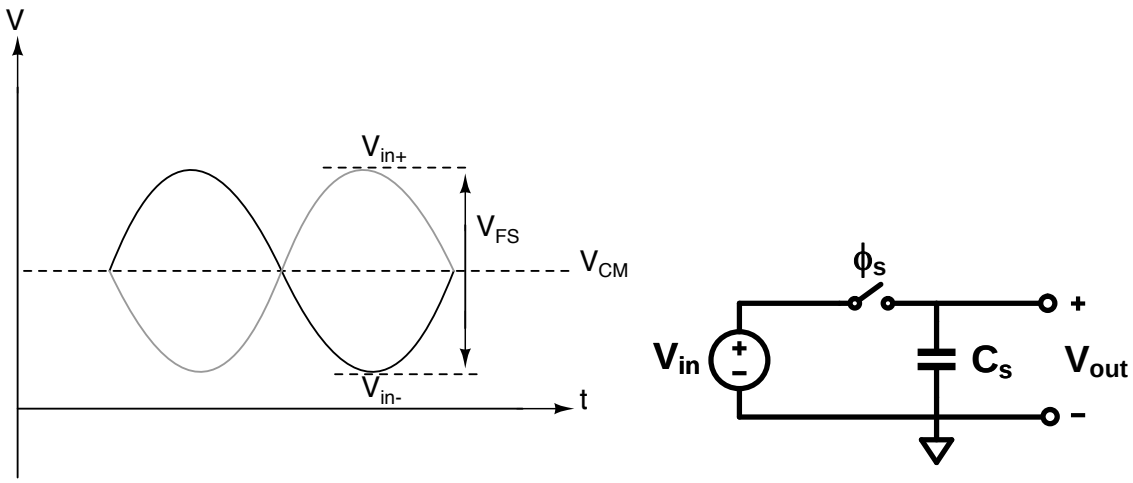
A clear, concise and well-written report is key to receiving a favorable grade.

Design Procedure

The following subsections give an idea of where to start. The final goal is to meet the overall requirement of the receiver and not for individual blocks. Expect that a few iterations may be required before you meet the specifications.

1. System-Level Design

- Choose a reasonable value for full-scale voltage (V_{FS}) and common mode voltage (V_{CM}) for a supply voltage of V_{DD} shown in Fig. 3(a) and calculate the size of least significant bit (V_{LSB}). What constitutes a reasonable V_{FS} or V_{LSB}? Note that the differential input range of your sample and hold circuit is $[-V_{FS}, V_{FS}]$.



(a) (b)

Figure 3: (a) Definition of the Full Scale Differential Input Voltage and Common Mode Voltage; (b) Schematic of an ideal sampler.

A. Switched-Capacitor Input Stage

(10 Points)

- A single-ended sampler (Fig. 3(b)) consisting of a switch with a sampling capacitor C_s, will have a white noise output voltage with a variance given by $\overline{V^2_{out,n,RMS}} = kT/C_s$, with k the Boltzmann constant and T the absolute temperature. Note that for your design you will need to take into account the right sampling capacitor value and the fact that you have a differential design.
- The quantization noise for an A/D converter with a N-bit resolution will have an quantization error with a variance of $V^2_{LSB}/12$, where $V_{LSB} = (2 * V_{FS})/2^N$.
- The design specification for this project is to keep the variance of the thermal noise due to the sampler below the variance of the quantization error by a factor of 2. Again, note that you need to take into account the differential nature of your circuit.
- Derive the transfer function for the switched capacitor gain block.
- Assume an ideal OTA (very large Gain-Bandwidth (GBW) and DC gain), and find the largest switch resistance you can tolerate for your settling constraints.
- Choose the switch MOSFET sizes.
- Pay attention to the switch resistance and the charge injection[1]

B. OTA Parameters

(10 Points)

[1] You can consider bottom-plate sampling to reduce the charge injection; it means that the switches connecting the sampling and hold capacitors to V_{cm} at the OTA's inputs are opened slightly in advance of the sampling switches which connect these capacitors to the input; you will have to generate a special clock signal in your clock buffer/generator to achieve this. See e.g., R. Jacob Baker, *"CMOS: Circuit Design, Layout, and Simulation"*, page 841, 3^{rd} Edition.

- Determine the OTA specifications using the ideal OTA model provided to you under CourseWorks/ Files & Resources (gain, bandwidth, phase margin, slewing) based on the settling requirements.
- Use the OTA model and MOSFET switches derived in Section A and verify the functionality of your design.
- Make sure that you get an input referred settling error of less than $\frac{V_{LSB}}{4}$ when you input a full-scale amplitude step.

2. OTA Transistor-Level Design

(10 Points)

- Design an OTA that satisfies these requirements: choose the topology, size transistors, verify specs.
- Pay a lot of attention to the design of the common mode feedback circuit for your OTA that has sufficient bandwidth as well as phase margin.

3. Complete Stage

(Submission Deadline: May 6th - No extensions will be granted.) (70 Points)

At this point, if you are unable to reach the specs as decided by phase I of your project, assume a reasonable set of parameters for the rest of the project. If you do change the specs, consult the TA for a sanity check. If you need any kind of help with the OTA design, do not hesitate to approach the TA.

- Plug the OTA in the fully differential switched capacitor sample-and-hold amplifier with MOSFET switches and run through the clock phases. Prove the 4x amplification happens with the right accuracy. Show that you have enough settling time, etc.
- Make sure that you get an input referred settling error of less than $\frac{V_{LSB}}{2}$ when you input a full-scale amplitude step.
- You need to show results for the following two transient simulations at least:
  1. Apply at the input a small signal step going from V_{LSB} to $-V_{LSB}$ and back to V_{LSB}.
  2. Apply a sawtooth ramp with a period of Tclk/20, covering the full-scale input range of the design $[-V_{FS}, V_{FS}]$.
  3. Apply at the input a large signal step going from V_{FS} to $-V_{FS}$ and back to V_{FS}.

Important Remarks

1. As an input source you can use an ideal voltage source with a 50Ω source resistance for each of the differential input branches.
2. As a load assume 4 parallel capacitors of size $C_{samp}/4$ representing the sampling capacitor of the next stage.
3. The input and output common mode voltages need to be equal.
4. You can use ideal voltage sources to generate all your clocks; use a 50Ω series resistance for each of the differential clock inputs. You need to design a 3-stage inverter chain as the clock driver; i.e. your switches are not connected to the ideal clock source but rather to your clock buffer. Include the power dissipation of the clock driver in your total reported power. You can also consider designing a simple non-overlapping clock generator; e.g. refer to Fig. 14.3 in Johns and Martin (Second Edition).
5. Maximum and minimum length and width values you can use for transistor finger sizes are specified as: $0.18\mu m < L < 10\mu m$ and $0.18\mu m < W < 20\mu m$. You can use as many multipliers as you want.