EE6312-HOMEWORK II

Problem 1

For a nMOS transistor of size $\frac{1\ \mu m}{0.18\ \mu m}$ biased at $V_{GS} = 0.8\ V$ and $V_{BS} = 0\ V$, plot Cgs, Cgd, Cbd as a function of V_{DS}. Use the 0.18 μm CMOS teaching model for all simulations. Use AC analysis with a thoughtfully selected test circuit to perform the measurements, and compare them with those obtained from DC operating point simulations.

You can also consult the tutorial. Remember the capacitance is the ratio between charge an voltage, or alternatively the current through a capacitor is related to voltage by frequency and capacitance, $V_C = \frac{I_C}{2\pi f C}$.

Please provide the circuit simulation setups that you used for each of the simulations.

Problem 2

In this exercise you will investigate the common-source (Fig1), common-drain (Fig2) and common-source with cascode (Fig3) basic amplifier configurations. All device sizes are indicated in the following table and $I_{REF} = 60\ \mu A$. Use the 0.18 μm CMOS teaching model for all simulations. For each of the configurations perform the following.

Parameter vs. Value	
Parameter	Value
$W/L(M1)$	2.5 μm/0.25 μm
$W/L(M2)$	2.5 μm/0.25 μm
$W/L(M3)$	2.5 μm/0.25 μm
$W/L(M4)$	2.5 μm/0.25 μm

- Replace the bias current source with an appropriate transistor realization. Also replace the BIAS block with an appropriate circuit realization. For the biasing you can assume you have transistors, capacitors, and resistors at your disposal. You can even assume you have very large valued R or C elements available if that helps you (e.g., if you think that you can obtain better results with a 1 F capacitor and 10 $M\Omega$ resistor, do not hesitate to use them). Additional connections to BIAS block are allowed.

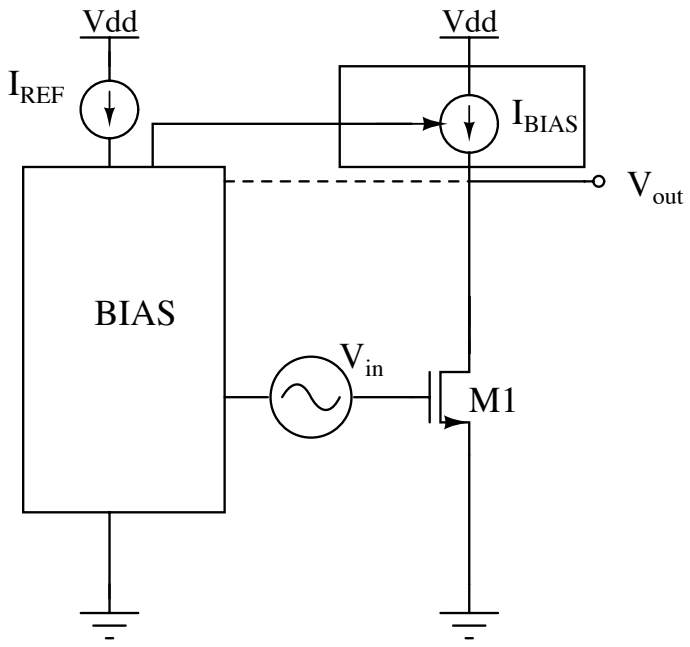

Figure 1: Common-source Amplifier

- Choose an appropriate bias point for maximum low-frequency gain in the circuit. You do not have to worry about bandwidth considerations.
- Simulate the magnitude of the low-frequency gain in the passband over PVT corners. Tabulate the results. Try to obtain as constant a gain over PVT as possible.

  For the nominal process conditions estimate the magnitude of the gain based on small signal parameters obtained from an operating point analysis.

  Typical case: tt (typical corner), $Temp = 27\ C$ and $V_{DD} = 1.8\ V$.

  Worst case: ss (slow corner), $Temp = 85\ C$ and $V_{DD} = 1.6\ V$.

  Best case: ff (fast corner), $Temp = -20\ C$ and $V_{DD} = 2\ V$.
- Apply a low-frequency sinusoid at the input of the circuit and do a transient analysis. Determine what the largest input and output swing is that the circuit can process with satisfactory performance. Make a plot of the transient waveforms.

  Estimate the largest signal swing based on parameters available from the operating point analysis.

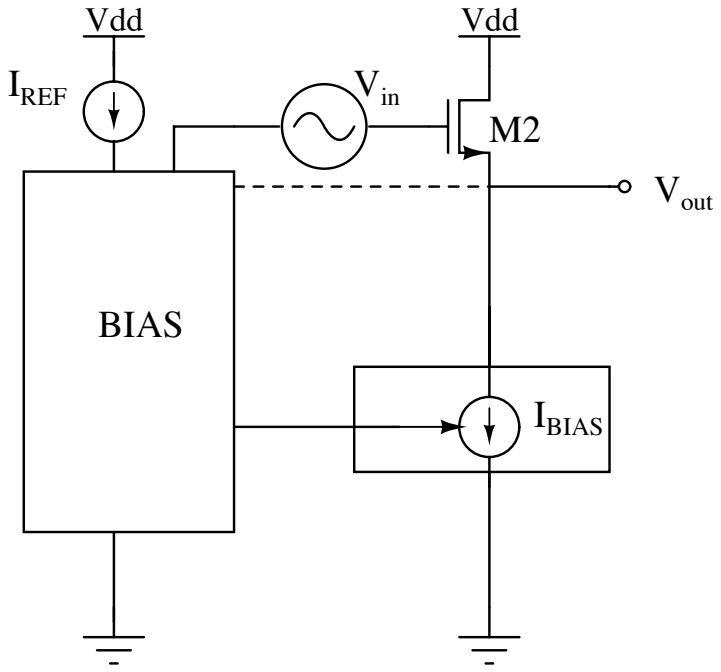

Figure 2: Common-drain Amplifier

- Additional credit for the common-source with cascode configuration: Determine the small signal gain Vout/Iin both in simulation and using small signal hand calculations.

Describe your reasoning for your design and calculations. Provide the simulations set-ups you used for this problem set and provide the necessary simulation results (operating point, plots, ...) to document your findings. Make sure you provide sufficient information, but not too much information either. The grade will depend both on the quality of the results as well as the quality of the succinct, but insightful description of your reasoning and calculations.

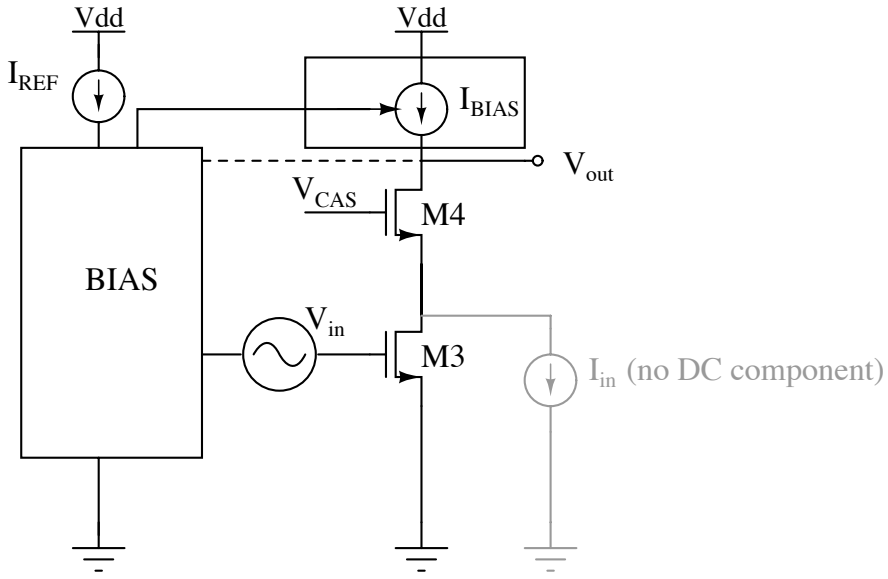

Figure 3: Common-source with Cascode Amplifier - Current signal source should be used for additional credit part