

E6312: Problem Set 2

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1 Problem 1

1.1

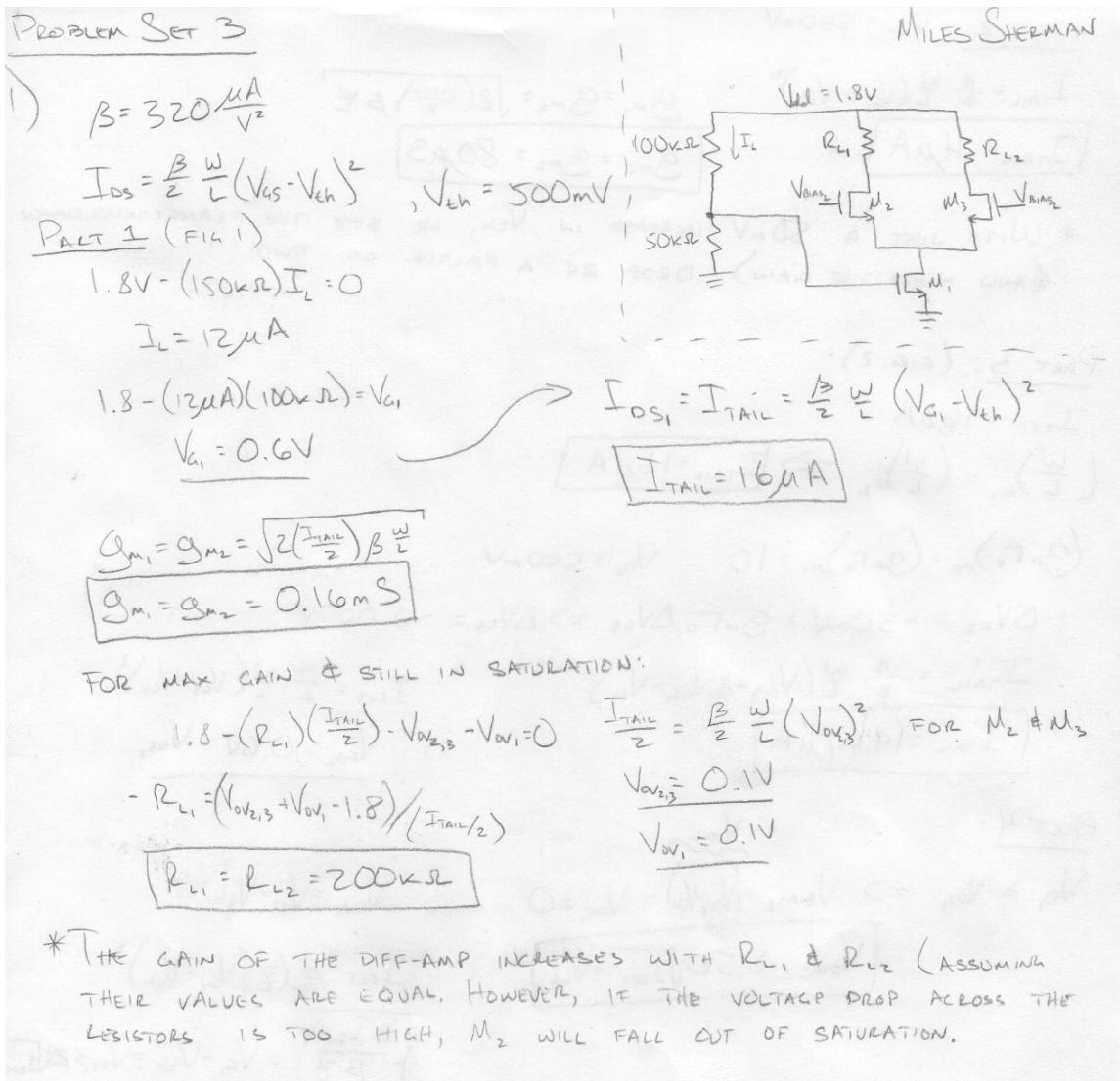


Figure 1: Hand-Written Work for Problem 1.1

1.2

PART 2 : $V_{th} = 550\text{mV}$

$$I_{TAIL} = \frac{\beta}{2} \frac{w}{L} (V_{G_1} - V_{th})^2$$

$$\boxed{I_{TAIL} = 4\mu\text{A}}$$

$$g_m = g_{m2} = \sqrt{2 \left(\frac{I_{TAIL}}{2} \right) \beta \frac{w}{L}}$$

$$\boxed{g_m = g_{m2} = 80\mu\text{S}}$$

* With just a 50mV increase in V_{th} , we see the transconductance drop by a factor of two.
(And hence the gain)

Figure 2: Hand-Written Work for Problem 1.2

1.3

PART 3 : (Fig. 2)

$$I_{REF} = 16\mu\text{A}$$

$$\left(\frac{w}{L}\right)_{M_0} = \left(\frac{w}{L}\right)_{M_1} \Rightarrow \boxed{I_{TAIL} = 16\mu\text{A}}$$

$$(g_m r_o)_{M_0} = (g_m r_o)_{M_1} = 10 \quad V_{D_1} = 550\text{mV}$$

$$\Delta V_{DS} = -50\text{mV} = g_m r_o \Delta V_{GS} \Rightarrow \Delta V_{GS} = -0.005\text{V}$$

$$I_{TAIL}' = \frac{\beta}{2} \frac{w}{L} (V_{G_2} + \Delta V_{GS} - V_{th})^2$$

$$\boxed{I_{TAIL}' = 14.4\mu\text{A}}$$

$$I_{REF} = \frac{\beta}{2} \frac{w}{L} (V_{GS} - V_{th})^2$$

$$V_{GS_0} = 0.6\text{V} = V_{GS_1}$$

Figure 3: Hand-Written Work for Problem 1.3

1.4

PART 4:

$$V_{D_1} \geq V_{ov_1} \Rightarrow V_{BIAS_2} - (V_{ov_2} + V_{th}) - V_{ov_1} = 0$$

$$V_{BIAS_2} = 50\sqrt{I_{REF}} + V_{th}$$

$$V_{ov_1} = V_{G_1} - V_{th}$$

$$I_{REF} = \frac{\beta}{2} \left(\frac{w}{L}\right) (V_{G_1} - V_{th})^2$$

$$\frac{2 I_{REF}}{\beta \frac{w}{L}} = V_{G_1} - V_{th} = V_{ov_1} = 25\sqrt{I_{REF}}$$

$$I_{REF} = \frac{\beta}{2} \left(\frac{w}{L}\right) V_{ov}^2$$

$$V_{ov_2} = \sqrt{625 I_{REF}}$$

$$V_{ov_2} = 25\sqrt{I_{REF}}$$

Figure 4: Hand-Written Work for Problem 1.4

* TO GENERATE V_{BIAS_2} WITHOUT AN ADDITIONAL CURRENT SOURCE I WILL USE THE TOPOLOGY BELOW:

$$I_{REF} = \frac{\beta}{2} \left(\frac{w}{L}\right)_S (V_{BIAS_2} - 25\sqrt{I_{REF}} - V_{th})^2$$

$$\left(\frac{w}{L}\right)_S = \frac{2 I_{REF}}{\beta (V_{BIAS_2} - 25\sqrt{I_{REF}} + V_{th} - V_{th})^2}$$

$$\left(\frac{w}{L}\right)_S = \frac{2 I_{REF}}{\beta (25\sqrt{I_{REF}} + V_{th})^2}$$

* SENSITIVE TO PROCESS VARIATION.

* THIS CIRCUIT IS SENSITIVE TO V_{BIAS} BECAUSE IT DIRECTLY AFFECTS THE CURRENT (AND HENCE THE TRANSCONDUCTANCE AND GAIN) THROUGH M_2 & M_3 .

Figure 5: Hand-Written Work for Problem 1.4 (ctnd)

1.5 (including additional credit problem)

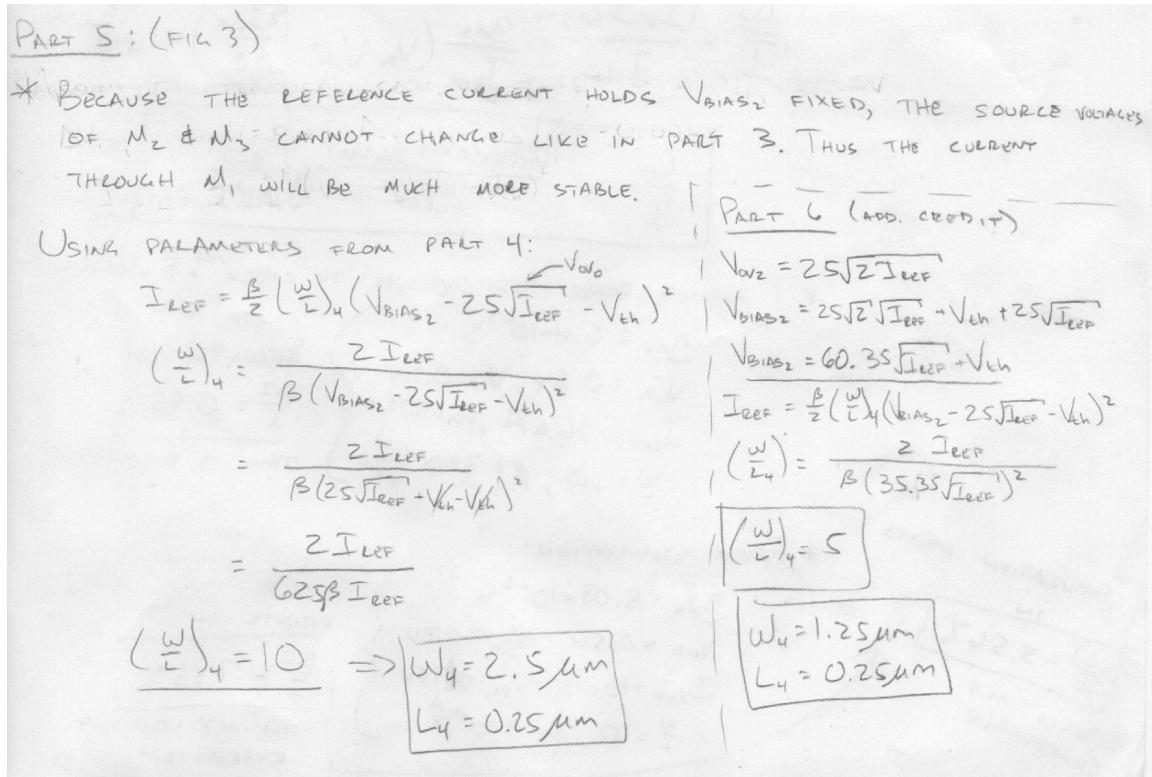


Figure 6: Hand-Written Work for Problem 1.5

2 Problem 2

2.1

For this problem, I performed hand-written calculations and verified my calculations with simulations (see Figures 8 and 9). It should be noted that while my calculated values were not identical to those from simulations, they were reasonably close considering the assumptions made. These assumptions include $\beta = 320 \frac{\mu A}{V^2}$ and $V_{th} = 500mV$.

2) PART 1.

$$g_{ds} = \frac{2I_{ds}}{2V_{ds}}$$

V_{ds} = FIXED VALUE

$V_{ds\text{-MATCH}}$ = IDEAL VALUE
BASED ON $V_{ds2} = V_{ds1}$

PERFECT CURRENT MATCH CONDITION.

(IDEAL)
FOR MATCHED CURRENTS:

$$I_{ds1} = \frac{\beta}{2} \frac{w}{L} (V_{ds1} - V_{th})^2$$

$$V_{ds1} = V_{ds2} = \sqrt{\frac{2I_{REF}}{\beta w}} \Rightarrow V_{ds\text{-MATCH}} = V_{th} + \sqrt{\frac{2I_{REF}}{\beta w L}}$$

$$\Delta V_{ds} = V_{ds} - V_{ds\text{-MATCH}} \Leftarrow \text{ASSUMING } V_{ds} > V_{ds\text{-MATCH}}$$

$$\Delta I_{ds} = g_{ds} \Delta V_{ds}$$

$$\boxed{\Delta I_{ds} = g_{ds} (V_{ds} - V_{th} - \sqrt{\frac{2I_{REF}}{\beta w L}})}$$

$$I_o = I_{REF} + \Delta I_{ds}$$

$$\boxed{I_o = I_{REF} + g_{ds} (V_{ds} - V_{th} - \sqrt{\frac{2I_{REF}}{\beta w L}})}$$

$$\frac{\Delta I}{I} = \frac{(I_o - I_{REF}) \cdot 100}{I_{REF}} = \frac{g_{ds}}{I_{REF}} (V_{ds} - V_{th} - \sqrt{\frac{2I_{REF}}{\beta w L}}) \times 100$$

$$\boxed{\frac{\Delta I}{I} = \frac{100(g_{ds} V_{ds} - g_{ds} V_{th})}{I_{REF}} - g_{ds} \sqrt{\frac{20}{\beta w L I_{REF}}}}$$

* I APPLIED SOME TEST VALUES TO CHECK MY WORK:

$$g_{ds} = 6.4 \times 10^{-7} \text{ S}$$

$$V_{th} = 0.5 \text{ V}, V_{ov} = 0.2 \text{ V}$$

$$I_{REF} = 16 \mu\text{A}, V_{ds} = 0.75 \text{ V}$$

$$\frac{w}{L} = 10, \beta = 320 \frac{\mu\text{A}}{\text{V}^2}$$

RESULTS IN

$$\frac{\Delta I}{I} = 0.98 \%$$

THIS IS REASONABLE!

SIMULATION RESULTS
 $\frac{\Delta I}{I} = 5.56\%$
RESULTS ARE COMPARABLE.

* FROM SIMULATION:

$$g_{ds} = 5.08 \times 10^{-6} \text{ S}$$

$$V_{th} \approx 0.5 \text{ V}, V_{ov} \approx 0.2 \text{ V}$$

$$I_{REF} = 16 \mu\text{A}, V_{ds} = 0.75 \text{ V}$$

$$\frac{w}{L} = 10, \beta = 320 \frac{\mu\text{A}}{\text{V}^2}$$

RESULTS IN

$$\frac{\Delta I}{I} = 7.83 \%$$

FROM MY DERIVED EXPRESSION

Figure 7: Hand-Written Work for Problem 2.1

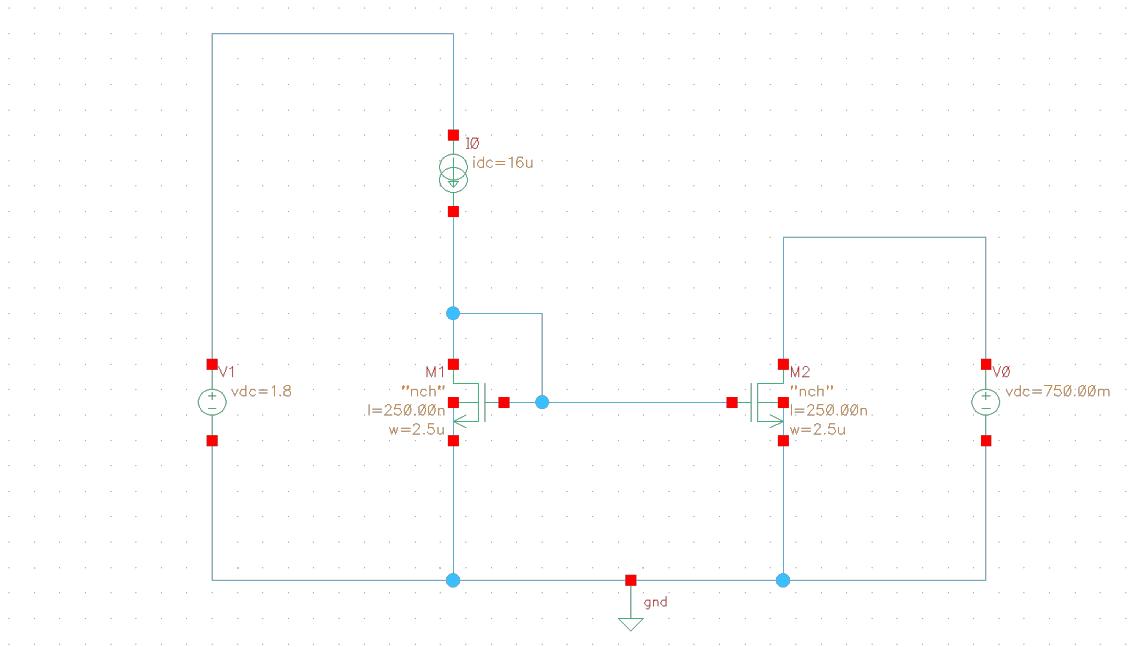


Figure 8: Schematic to Verify Sizing Calculations

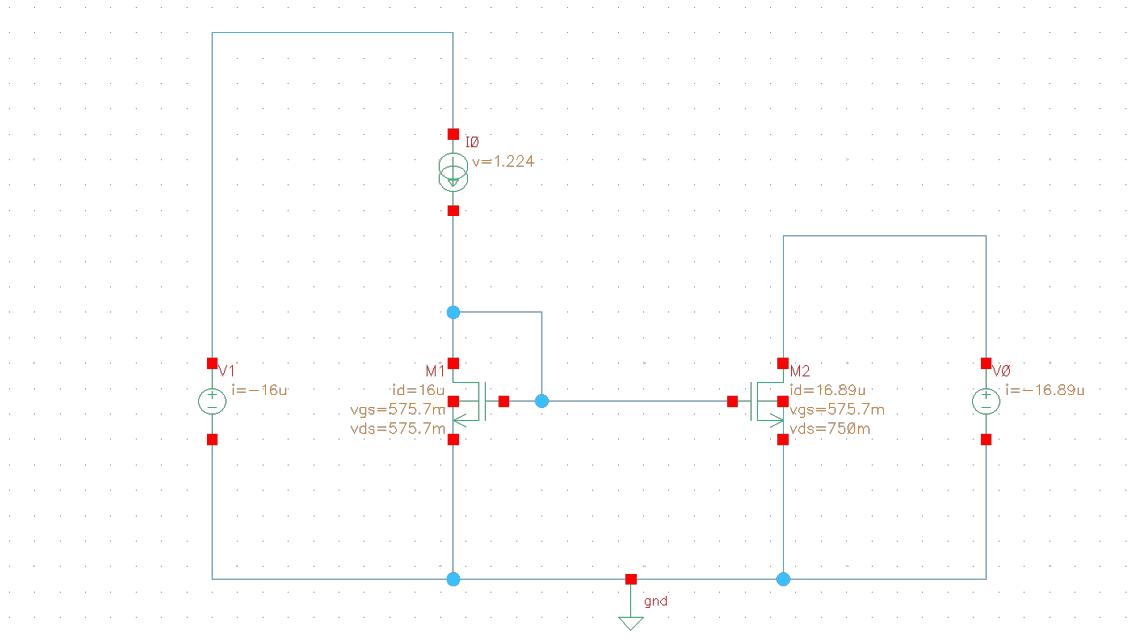
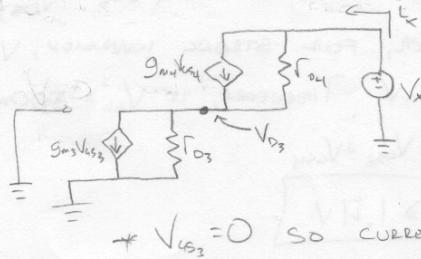
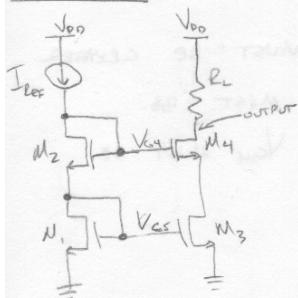


Figure 9: Schematic with DC Operating Point Annotations To Verify Calculations

2.2

For this problem, I performed hand-written calculations and verified my calculations with simulations (see Figures 11, 12, 13, and 14). Again because I made assumptions in my hand calculations, I had to slightly modify my size values in simulation to attain the correct current error. However, it was still very necessary to perform the calculations before simulating because they streamlined the design process. Without my calculations to determine at least a ballpark for each component parameter, the design would have been much more difficult and confusing.

PART 2



* $V_{DS3} = 0$ so current source off

M_3 is open circuited.

$$R_o = \frac{V_x}{i_x}$$

$$V_x - i_x R_{o4} - i_x R_{o3} - i_x (G_{m4} R_{o4} R_{o3}) = 0$$

$$V_{DS} = 200\text{mV}, I_{REF} = 1\text{mA}, R_L = 500\Omega$$

$$\beta = 320 \frac{\mu\text{A}}{\text{V}^2}, V_{th} = 0.5\text{V}$$

$$V_{DS} = V_{DS1} = 700\text{mV}, V_{DS1} = V_{DS2} = 700\text{mV}$$

$$I_{REF} = \frac{\beta}{2} \left(\frac{W}{L} \right)_3 (V_{DS3} - V_{th})^2 \left(1 + \frac{V_{DS3}}{V_A} \right)$$

$$\left(\frac{W}{L} \right)_3 = \left(\frac{W}{L} \right)_4 = 122.07$$

$$W_1 = W_2 = 30.52\mu\text{m}$$

$$L_1 = L_2 = 0.25\mu\text{m}$$

$$R_{o_{DS}} = G_{m4} R_{o4} R_{o3} + R_{o3} + R_{o4}$$

$$R_{o_{DS}} \approx G_{m4} R_{o3} R_{o4}$$

$$R_o = R_{o_{DS}} \parallel R_L$$

$$R_o = \frac{G_{m4} R_{o3} R_{o4} R_L}{G_{m4} R_{o3} R_{o4} + R_L}$$

$$V_A = V_{AL} \cdot L \quad \text{choose } L = 250\text{nm},$$

$$V_A = 2.5\text{V} \quad V_{AL} = 10 \frac{\text{V}}{\mu\text{m}}$$

FOR 1% ACCURACY

$$1.01 I_{REF} = \frac{\beta}{2} \left(\frac{W}{L} \right)_3 (V_{DS3} - V_{th})^2 \left(1 + \frac{V_{DS3}}{V_A} \right) \quad V_{DS3} = V_{DS4} = 200\text{mV}$$

$$\left(\frac{W}{L} \right)_3 = \left(\frac{W}{L} \right)_4 = 146.122$$

$$\Rightarrow \left[\begin{array}{l} W_3 = W_4 = 36.53\mu\text{m} \\ L_3 = L_4 = 0.25\mu\text{m} \end{array} \right]$$

FOR 10% ACCURACY

$$1.1 I_{REF} = \frac{\beta}{2} \left(\frac{W}{L} \right)_3 (V_{DS3} - V_{th})^2 \left(1 + \frac{V_{DS3}}{V_A} \right)$$

$$\left(\frac{W}{L} \right)_3 = \left(\frac{W}{L} \right)_4 = 159.14$$

$$\Rightarrow \left[\begin{array}{l} W_3 = W_4 = 39.79\mu\text{m} \\ L_3 = L_4 = 0.25\mu\text{m} \end{array} \right]$$

Figure 10: Hand-Written Work for Problem 2.1

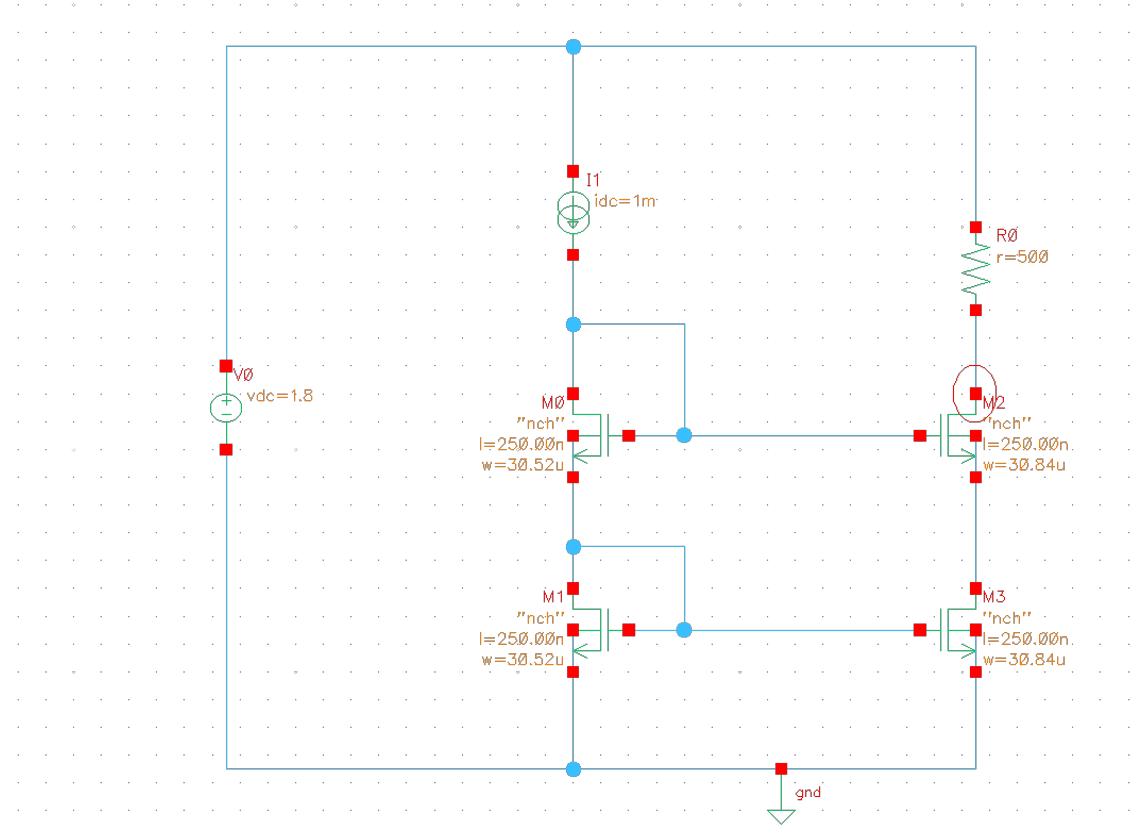


Figure 11: Schematic to Verify Sizing Calculations for 1% Current Error

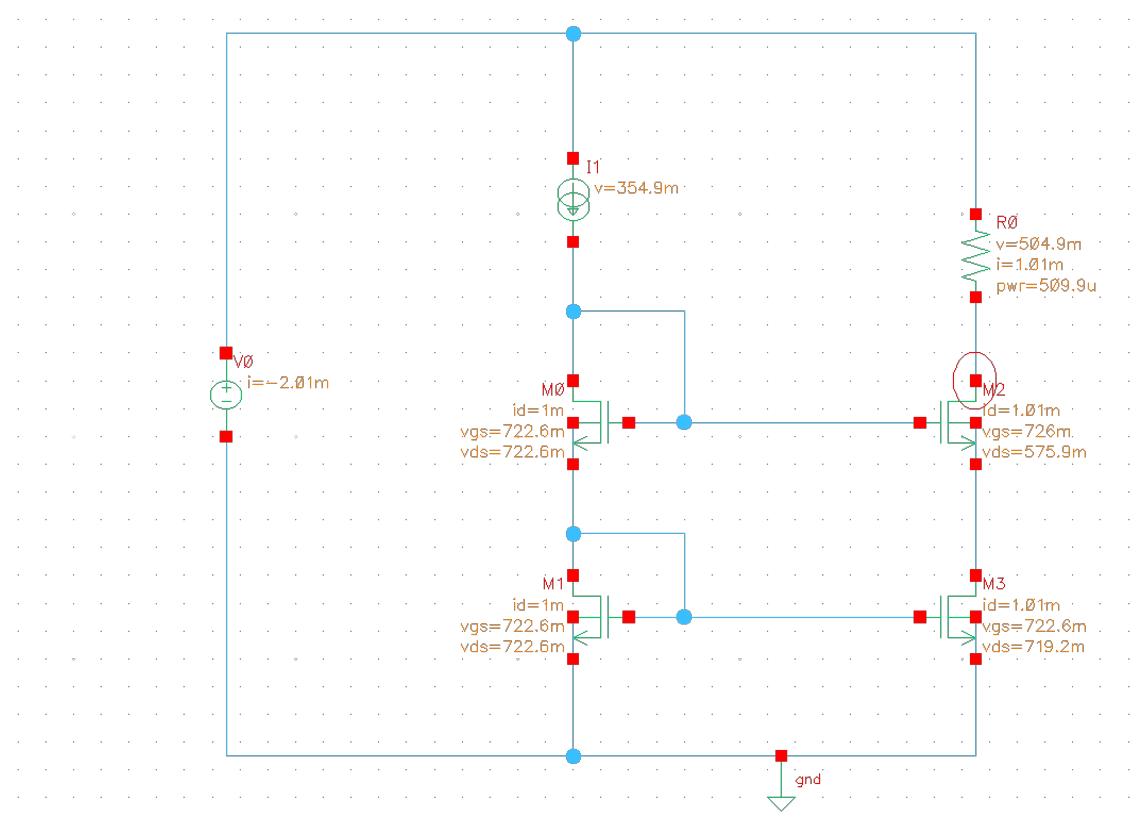


Figure 12: Schematic with DC Operating Point Annotations Verifying Sizing Calculations for 1% Current Error

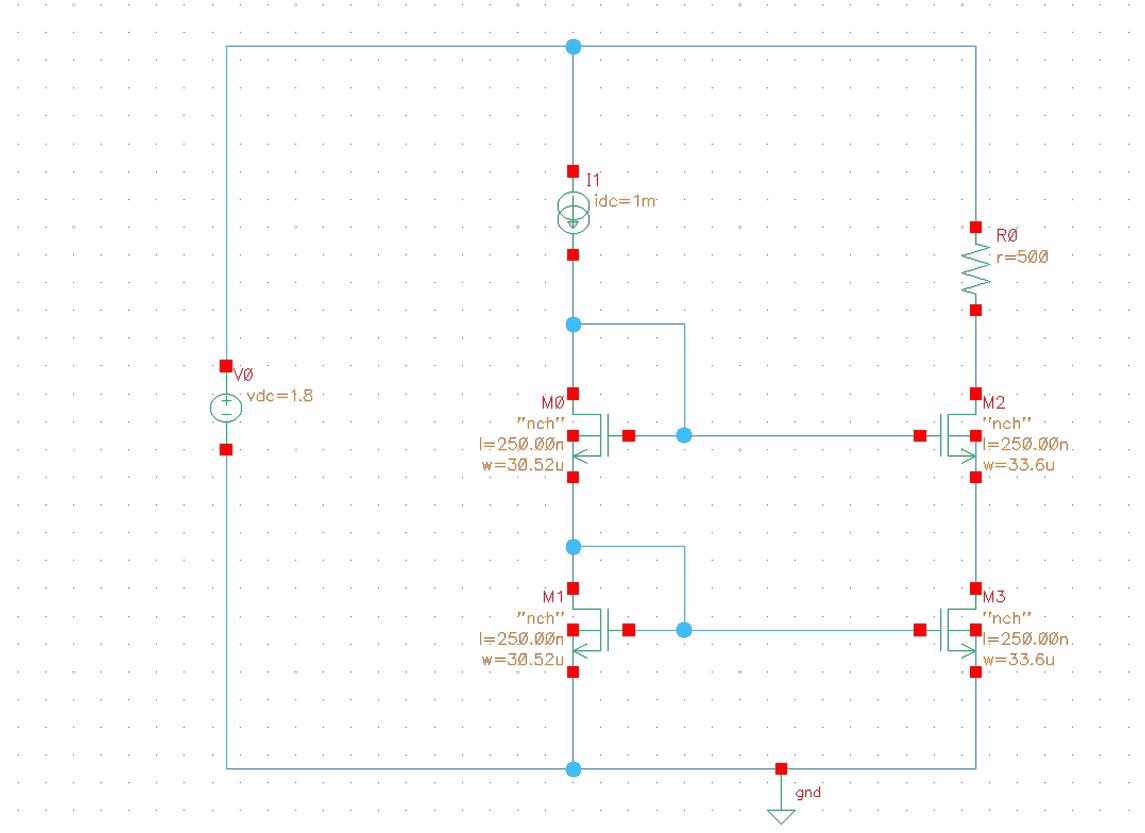


Figure 13: Schematic to Verify Sizing Calculations for 10% Current Error

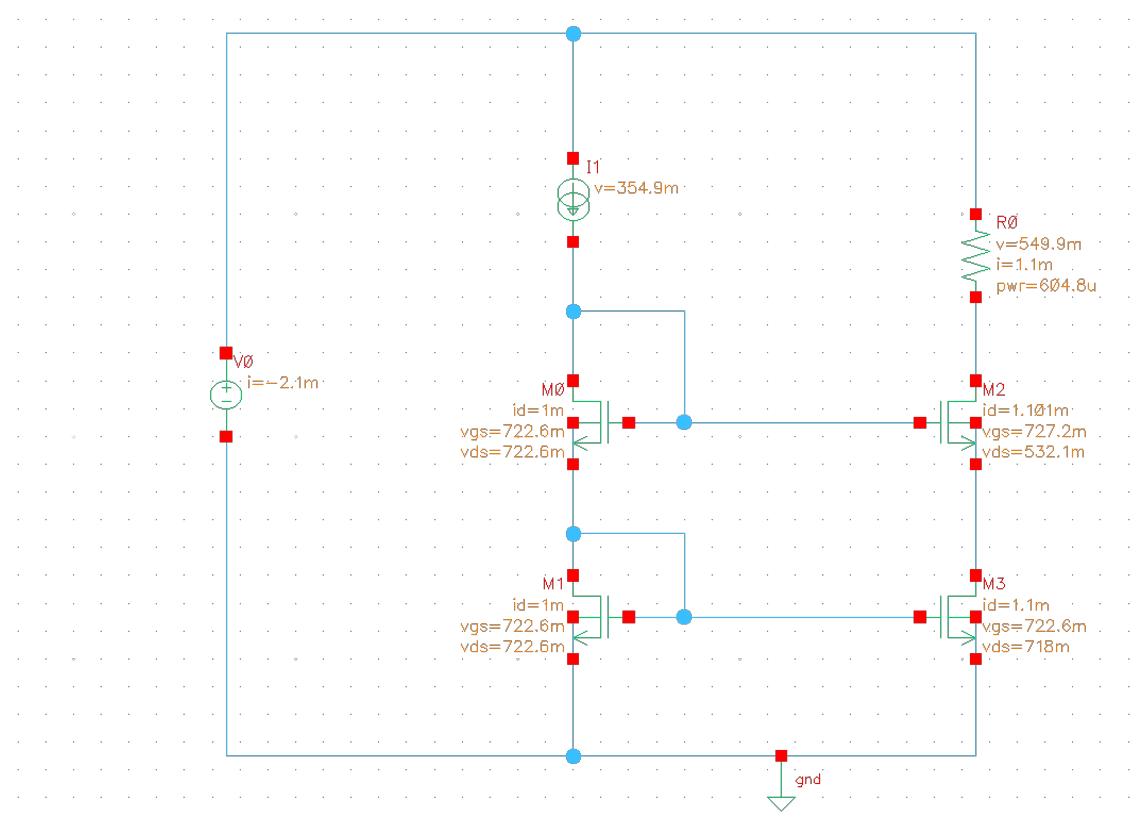


Figure 14: Schematic with DC Operating Point Annotations Verifying Sizing Calculations for 10% Current Error

2.3

For this problem, I simulated current against Drain Voltage to show how the error trends. For Figure 5 from the original assignment write-up, I swept V_{DS} and the current error is shown in Figure 15. In this plot, the current error is somewhat consistent for most voltage values but drops off around 200mV. This voltage is the compliance of this circuit because it is the minimum voltage to keep M2 in saturation.

For Figure 6 from the original assignment write-up, I swept the drain voltage of M4 using a voltage source and this time the current is seen to saturate around 400mV (the minimum voltage to keep both M3 and M4 in saturation). This plot can be seen in Figure 16.

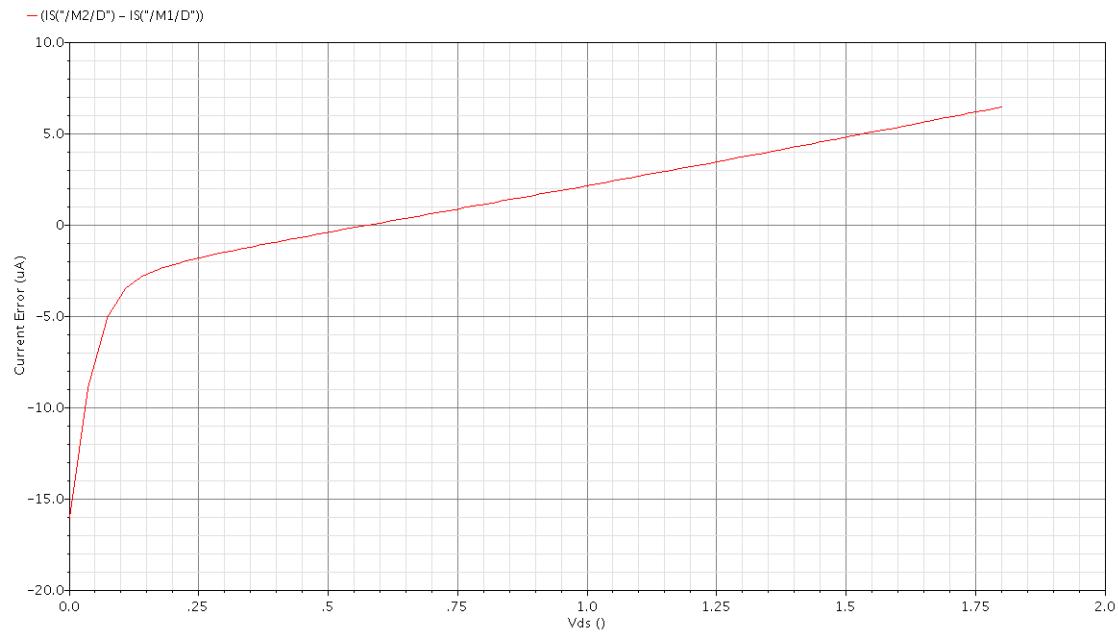


Figure 15: Current Gain vs. V_{DS} for the Basic Current Mirror Configuration

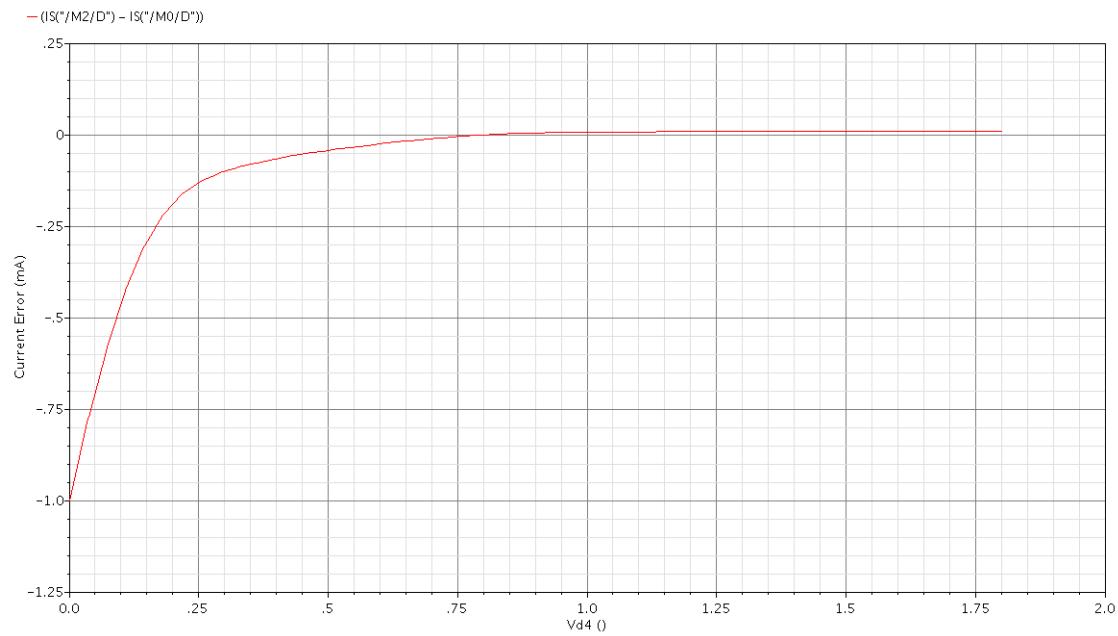


Figure 16: Current Gain vs. V_{D-4} for the Cascode Current Mirror Configuration

2.4

PART 4 Assuming $V_{ov} = 200mV$

* V_{G4} CONTROLS THE DRAIN VOLTAGES OF M_1 & M_3 . V_{DS3} MUST BE GREATER THAN $200mV$. HOWEVER, FOR STRONG INVERSION, V_{DS3} MUST BE GREATER THAN $700mV$. THEREFORE, IF $V_{th} = 500mV$, V_{G4} MUST BE AT LEAST: $V_{G4} \geq V_{GS3} + V_{GS4}$

$$V_{G4} \geq 1.4V$$

* IN PART 2 I ASSUMED THAT $V_{DS3} = 200mV$ WHICH WOULD ACTUALLY MEAN THAT M_1 WAS NOT IN STRONG INVERSION. WITH $V_{G4} = 1.4V$, $V_{DS3} = 700mV$.

FIGURE 7:

$V_{G3} = 700mV$, $V_{th} = 500mV$, $I_{REF} = 1mA$, $V_{ov} = 200mV$, $R_L = 500\Omega$

$V_{R1} = 200mV$ $V_{G4} = V_{ov} + V_{GS4}$ $V_A = 2.5V$
 $R_1 = V_{L1}/I_{REF}$ $V_{G4} = 900mV$ (FROM PREVIOUS PROBLEM)

$$R_1 = 200\Omega$$

$V_{DS1} = 200mV$ $V_{DS4} = V_{DD} - V_{R2} - V_{DS3}$
 \quad $= 1.8 - (0.01I_{REF})(500\Omega) - 200mV$
 \quad $= 1.095V$

$I_{REF} = \frac{\beta}{2} \left(\frac{W}{L}\right)_1 (V_{ov})^2 \left(1 + \frac{V_{DS1}}{V_A}\right)$ $1.01I_{REF} = \frac{\beta}{2} \left(\frac{W}{L}\right)_4 (V_{ov})^2 \left(1 + \frac{V_{DS4}}{V_A}\right)$
 $\left(\frac{W}{L}\right)_1 = 144.68$ $\left(\frac{W}{L}\right)_4 = 109.74$

$$W_1 = 36.17\mu m, L_1 = 0.25\mu m$$

$$W_4 = 27.45\mu m, L_4 = 0.25\mu m$$

$I_{REF} = \frac{\beta}{2} \left(\frac{W}{L}\right)_2 (V_{ov})^2 \left(1 + \frac{V_{DS2}}{V_A}\right)$ $V_{DS2} = 700mV - 200mV$
 $\left(\frac{W}{L}\right)_2 = 130.21$ $V_{DS2} = 500mV$

$$W_2 = 32.55\mu m, L_2 = 0.25\mu m$$

$1.01I_{REF} = \frac{\beta}{2} \left(\frac{W}{L}\right)_3 (V_{ov})^2 \left(1 + \frac{V_{DS3}}{V_A}\right)$ $V_{DS3} = V_{G4} - V_{GS3}$
 $\left(\frac{W}{L}\right)_3 = 146.12$ $V_{DS3} = 200mV$

$$W_3 = 36.53\mu m, L_3 = 0.25\mu m$$

* M_1, M_2, M_3, M_4 ARE ALL IN STRONG INVERSION & SATURATION

Figure 17: Hand-Written Work for Problem 2.4

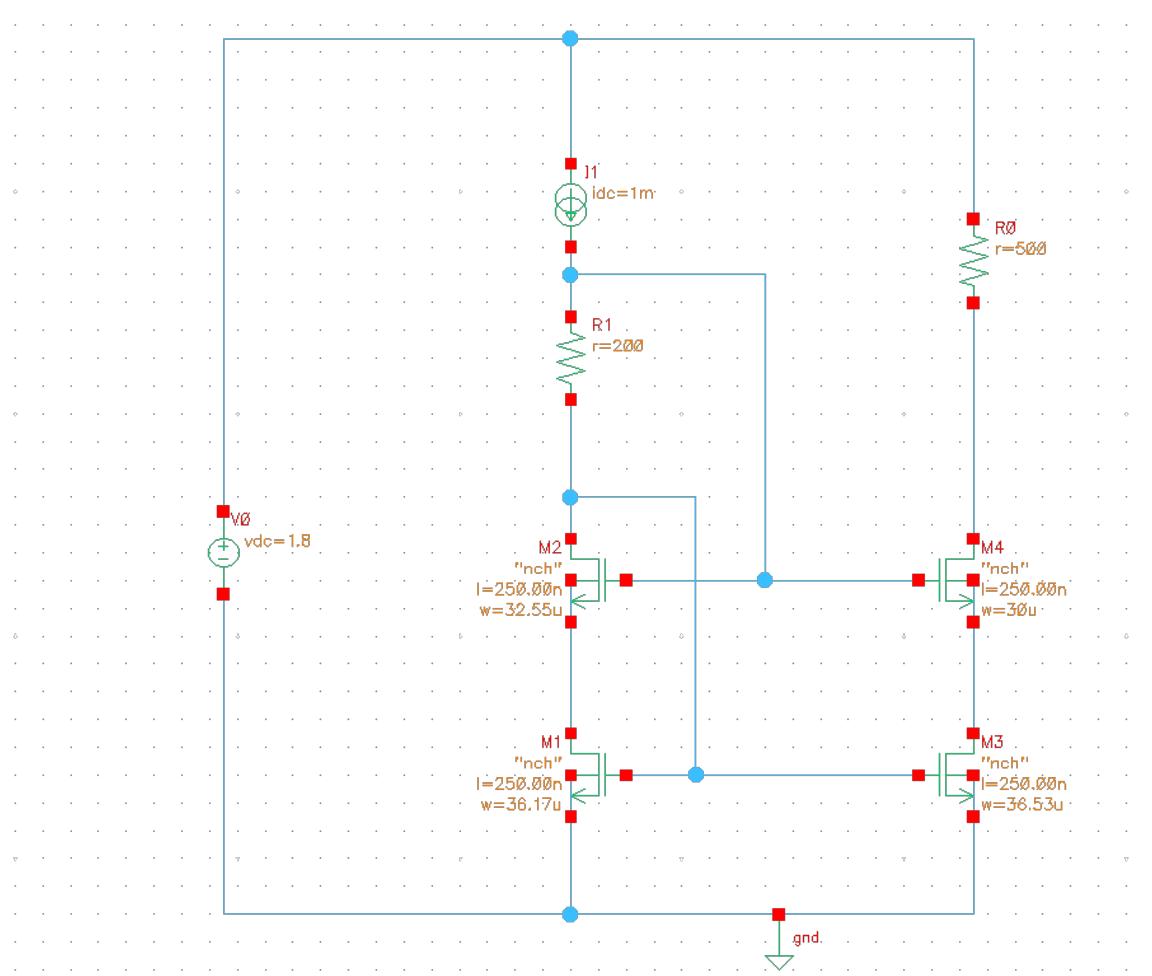


Figure 18: Schematic to Verify Sizing Calculations

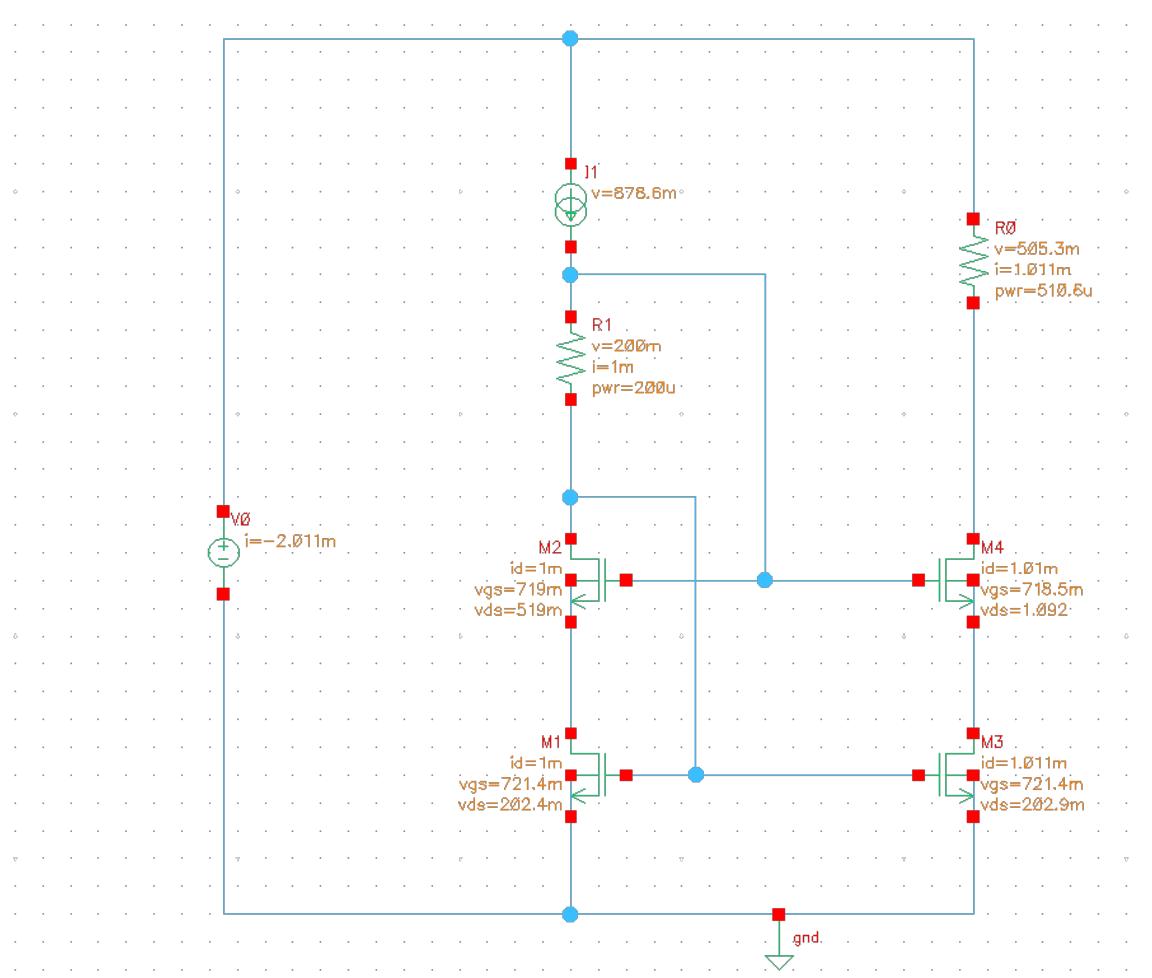


Figure 19: Schematic with DC Operating Point Annotations Verifying Sizing Calculations

2.5

PART 5 (FIG 8)

$$V_{ov} = 200mV, I_{ref} = 1mA, R_s = 500\Omega, V_A = 2.5V$$

$$I_{ref} = \frac{\beta}{2} \left(\frac{w}{L}\right)_2 \left(V_{ov}\right)^2 \left(1 + \frac{V_{ds2}}{V_A}\right) \quad V_{ds2} = 200mV$$

$$\left(\frac{w}{L}\right)_2 = 144.68$$

$$W_2 = 36.17\mu m, L_2 = 0.25\mu m$$

$$I_{ref} = \frac{\beta}{2} \left(\frac{w}{L}\right)_1 \left(V_{ov}\right)^2 \left(1 + \frac{V_{ds1}}{V_A}\right) \quad V_{ds1} = V_{G2} - V_{ds2} = 500mV$$

$$\left(\frac{w}{L}\right)_1 = 130.21$$

$$W_1 = 32.55\mu m, L_1 = 0.25\mu m$$

$$I_{ref} = \frac{\beta}{2} \left(\frac{w}{L}\right)_6 V_{ov}^2 \left(1 + \frac{V_{ds6}}{V_A}\right) \quad V_{ds6} = V_{G5} - V_{G1} = 500mV$$

$$\left(\frac{w}{L}\right)_6 = 130.21$$

$$W_6 = 32.55\mu m, L_6 = 0.25\mu m$$

$$\left(\frac{w}{L}\right)_6 = 3 \left(\frac{w}{L}\right)_5$$

$$W_5 = 10.85\mu m, L_5 = 0.25\mu m$$

$$1.01 I_{ref} = \frac{\beta}{2} \left(\frac{w}{L}\right)_3 V_{ov}^2 \left(1 + \frac{V_{ds3}}{V_A}\right) \quad V_{ds3} = V_{G4} - V_{G5} = 200mV$$

$$\left(\frac{w}{L}\right)_3 = 146.12$$

$$W_3 = 36.53\mu m, L_3 = 0.25\mu m$$

$$1.01 I_{ref} = \frac{\beta}{2} \left(\frac{w}{L}\right)_4 V_{ov}^2 \left(1 + \frac{V_{ds4}}{V_A}\right) \quad V_{ds4} = V_{DD} - (1.01 I_{ref}) R_s - V_{ds3} = 1.095$$

$$\left(\frac{w}{L}\right)_4 = 109.74$$

$$W_4 = 27.44\mu m, L_4 = 0.25\mu m$$

* ALL TRANSISTORS IN STRONG INV. & SATURATION EXCEPT
FOR M₅ WHICH IS IN THE LINEAR REGION.

Figure 20: Hand-Written Work for Problem 2.5

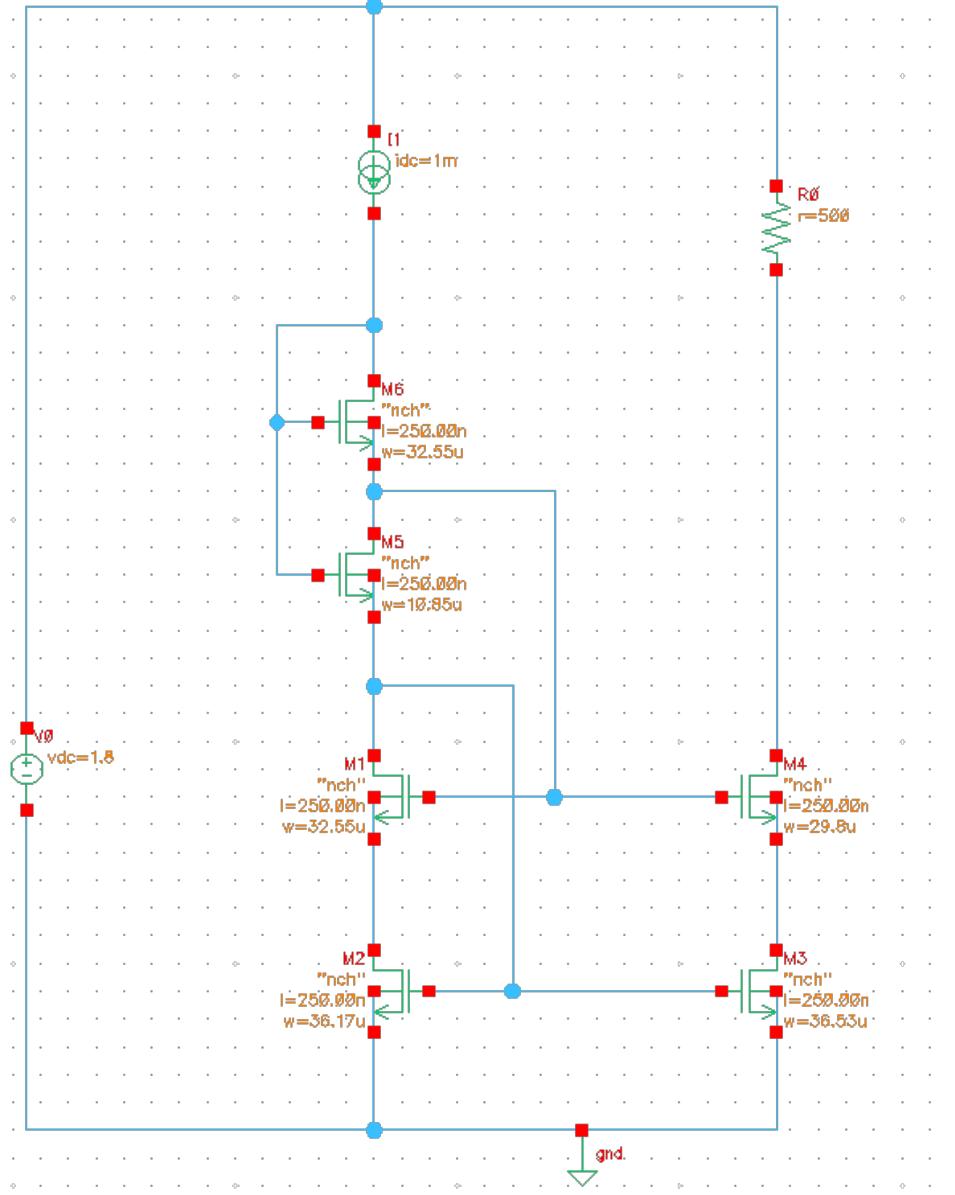


Figure 21: Schematic to Verify Sizing Calculations

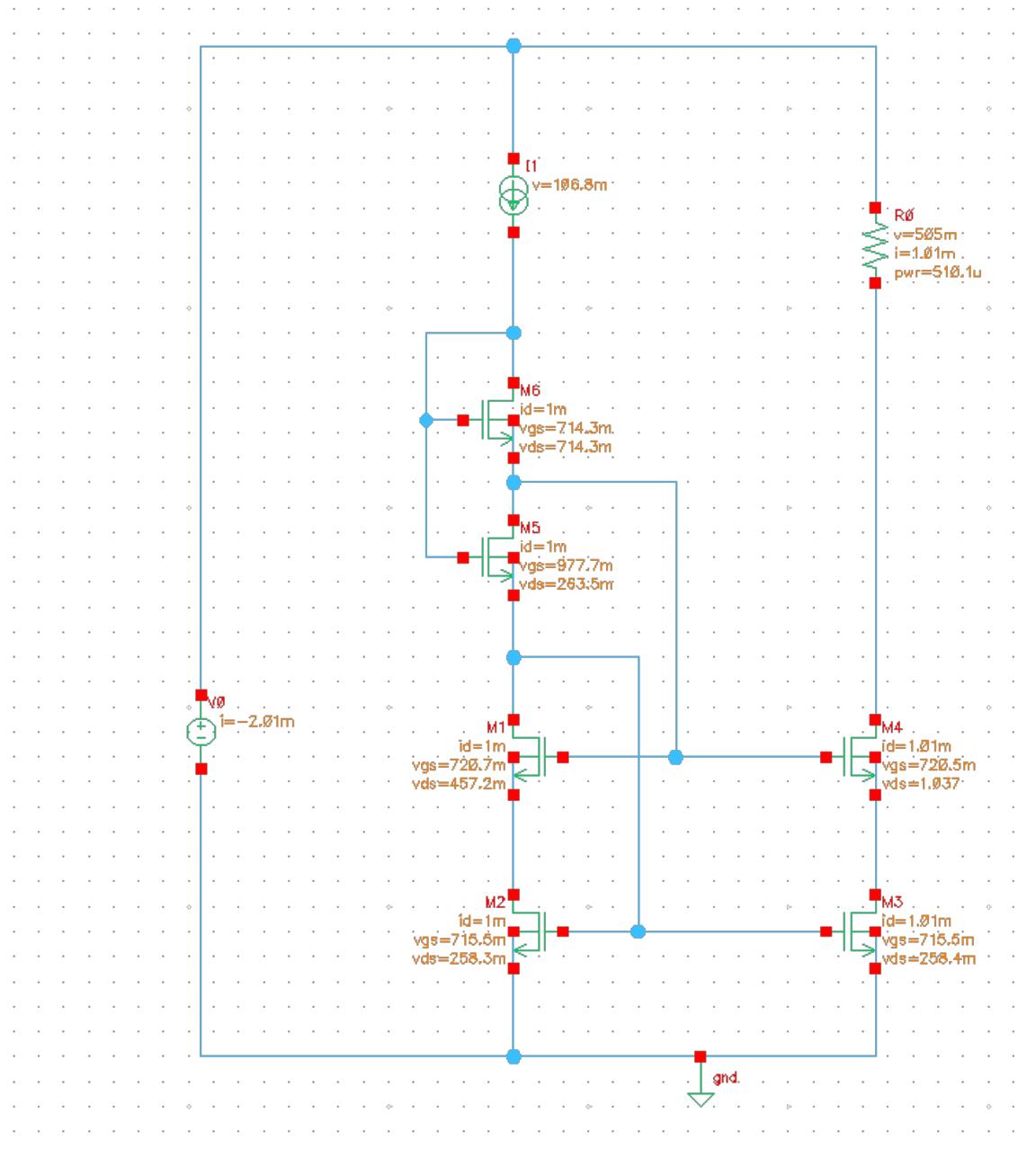


Figure 22: Schematic with DC Operating Point Annotations Verifying Sizing Calculations

2.6

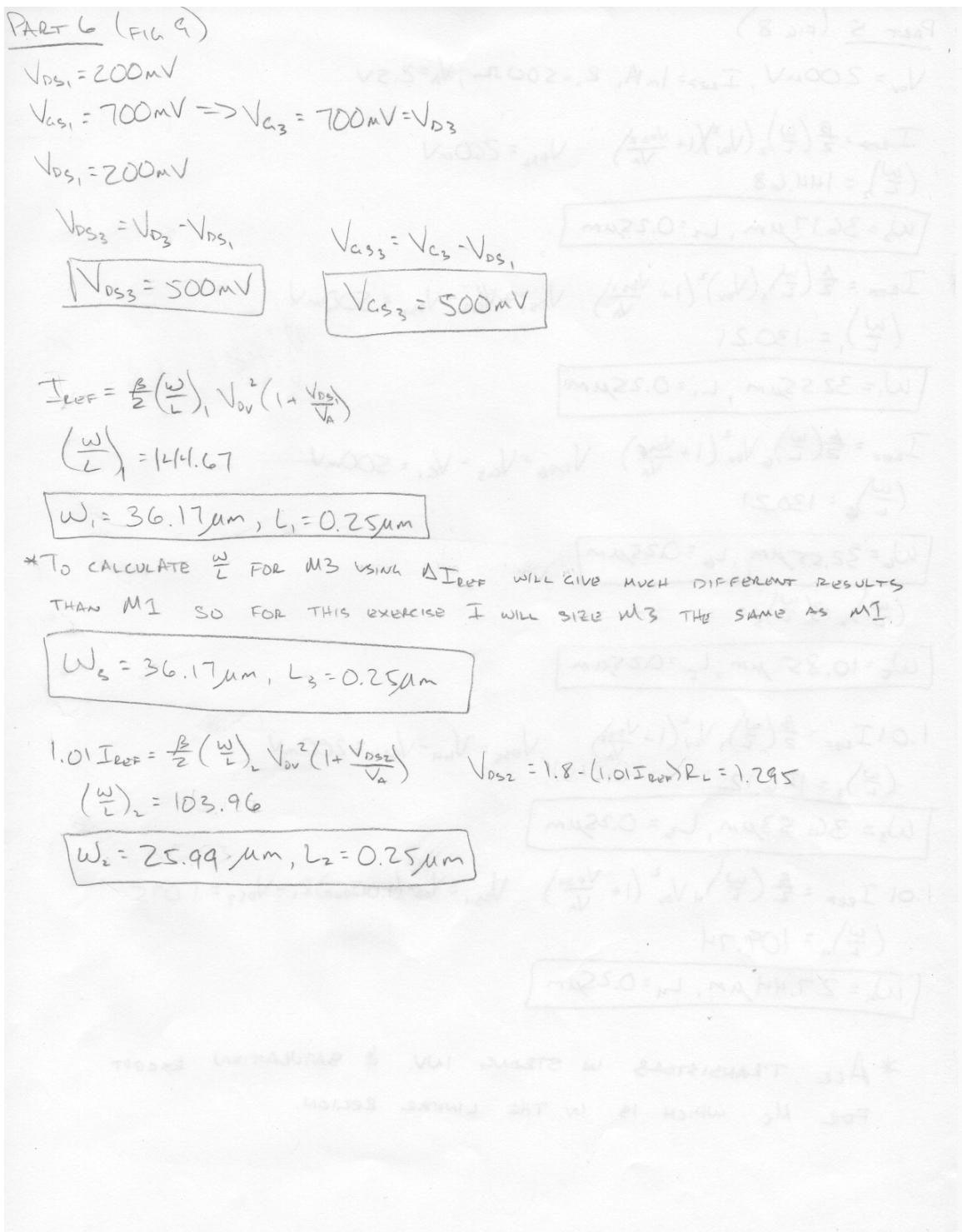


Figure 23: Hand-Written Work for Problem 2.6

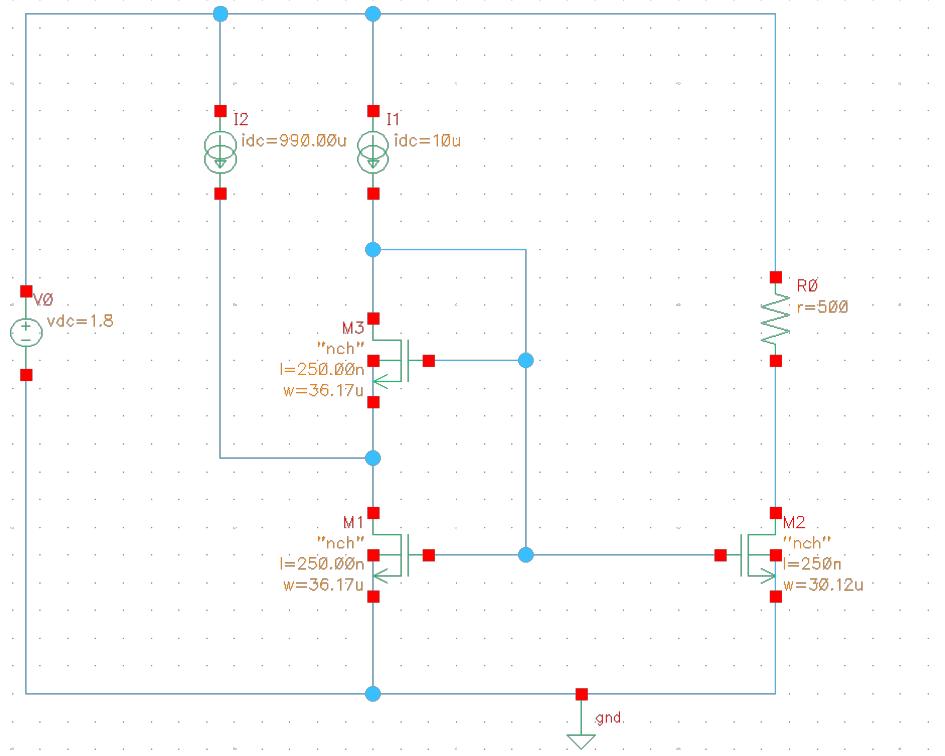


Figure 24: Schematic to Verify Sizing Calculations

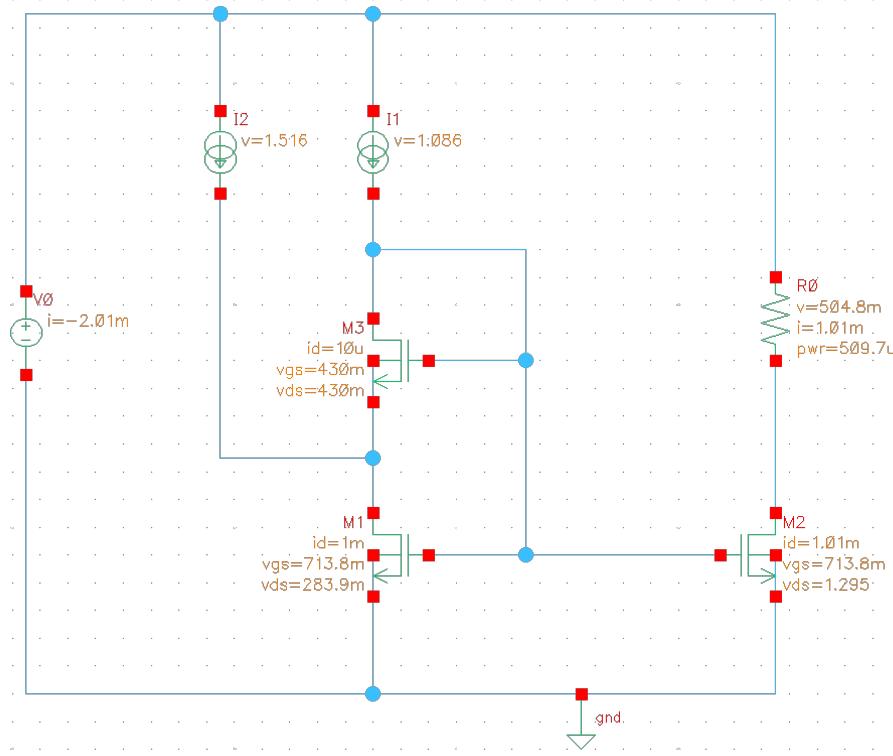


Figure 25: Schematic with DC Operating Point Annotations Verifying Sizing Calculations

3 Problem 3

3.1

3) PART 1

$\beta = 320 \frac{mA}{V^2}$, assume $V_{I_{TAIL}} = 200mV$, $V_A = 2.5V$, $V_{DS_1} = 900mV$

FIG 11 :

$$A_d = -g_m R_o$$

$$R_o = R_L \parallel r_o$$

$$I_{TAIL/2} = \frac{\beta(\omega)}{2} V_{ov}^2 \left(1 + \frac{V_{DS_1}}{V_A}\right)$$

$$I_{TAIL} = 348 \mu A$$

$$r_o = \frac{V_A}{I_{TAIL/2}}$$

$$R_L = 0.7 \sqrt{\frac{I_{TAIL}}{2}} \Rightarrow R_L = 4.02 k\Omega$$

$$r_o = 14.3 k\Omega$$

$$g_m = \sqrt{2 \left(\frac{I_{TAIL}}{2} \right) \beta \frac{W}{L}}$$

$$g_m = 1.49 mS$$

$$A_d = -4.68 V/V$$

FIG. 12 :

* Assume voltage across R_s is 50mV (to model transistor in triode)

$V_{ov} = 200mV$

$V_{DS_1} = 975mV$

$$R_s = \frac{50mV}{I_{TAIL}}$$

$$R_s = 140.85 \Omega$$

$$I_{TAIL/2} = \frac{\beta(\omega)}{2} V_{ov}^2 \left(1 + \frac{V_{DS_1}}{V_A}\right)$$

$$I_{TAIL} = 355 \mu A$$

$$R_L = \frac{775mV}{\left(\frac{I_{TAIL}}{2} \right)} \Rightarrow R_L = 4.366 k\Omega$$

$$r_o = \frac{V_A}{I_{TAIL/2}} \Rightarrow r_o = 14.08 k\Omega$$

$$g_m = \sqrt{2 \left(\frac{I_{TAIL}}{2} \right) \beta \frac{W}{L}}$$

$$g_m = 1.51 mS$$

$$r_o = 14.08 k\Omega$$

$$A_d = -5.03 V/V$$

Figure 26: Hand-Written Work for Problem 3.1

FIG 13 :

*BECAUSE FOR FIGURE 11 I CHOSE $V_{S1} = 200\text{mV}$, I WILL HAVE THE SAME GAIN AS IN THAT PART.

$$A_d = -4.68 \frac{V_o}{V_s}$$

ALSO, CURRENT WILL BE THE SAME SO I CAN CALCULATE I_{DC} .

$$I_{TANL} = 348\mu\text{A} = I_{DC}$$

$$V_o = 200\text{mV}$$

Figure 27: Hand-Written Work for Problem 3.1 (cntd)

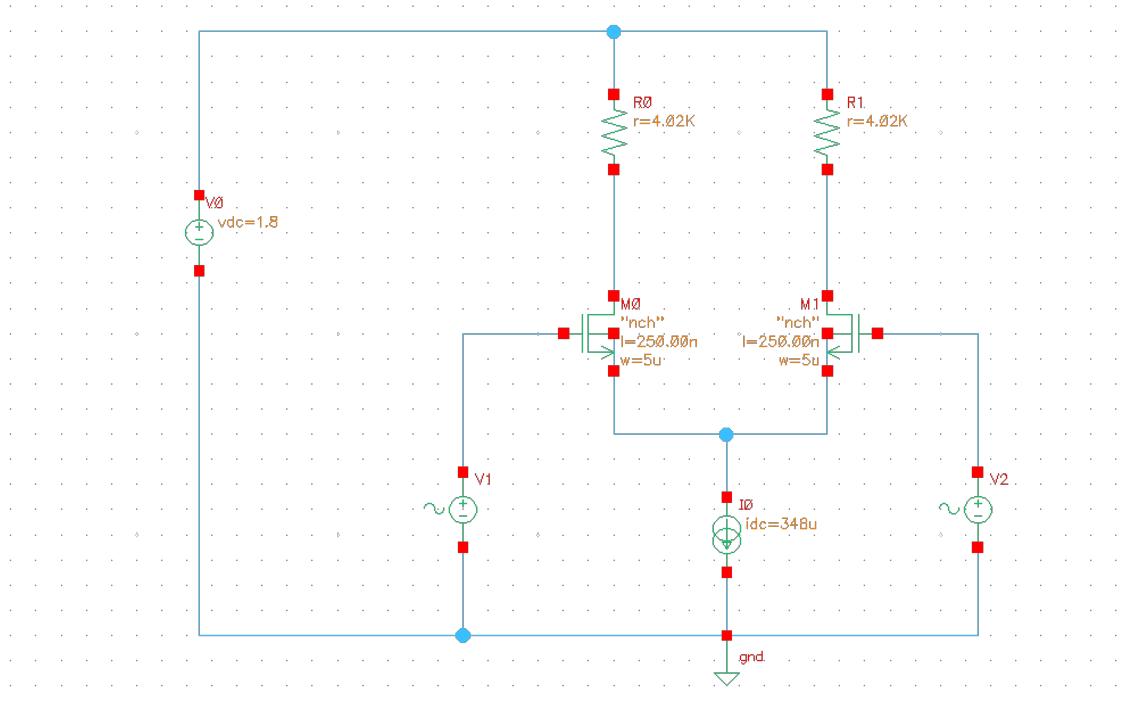


Figure 28: Schematic to Verifying Gain Calculations for Figure 11

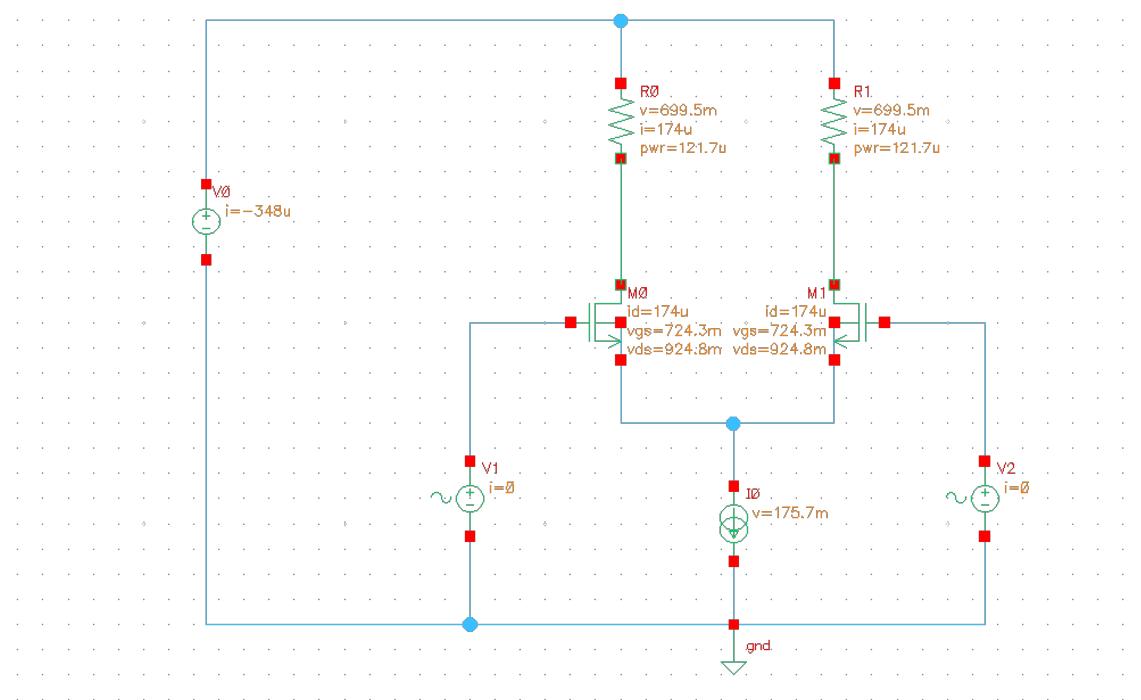


Figure 29: Schematic with DC Operating Point Annotations to Verifying Gain Calculations for Figure 11

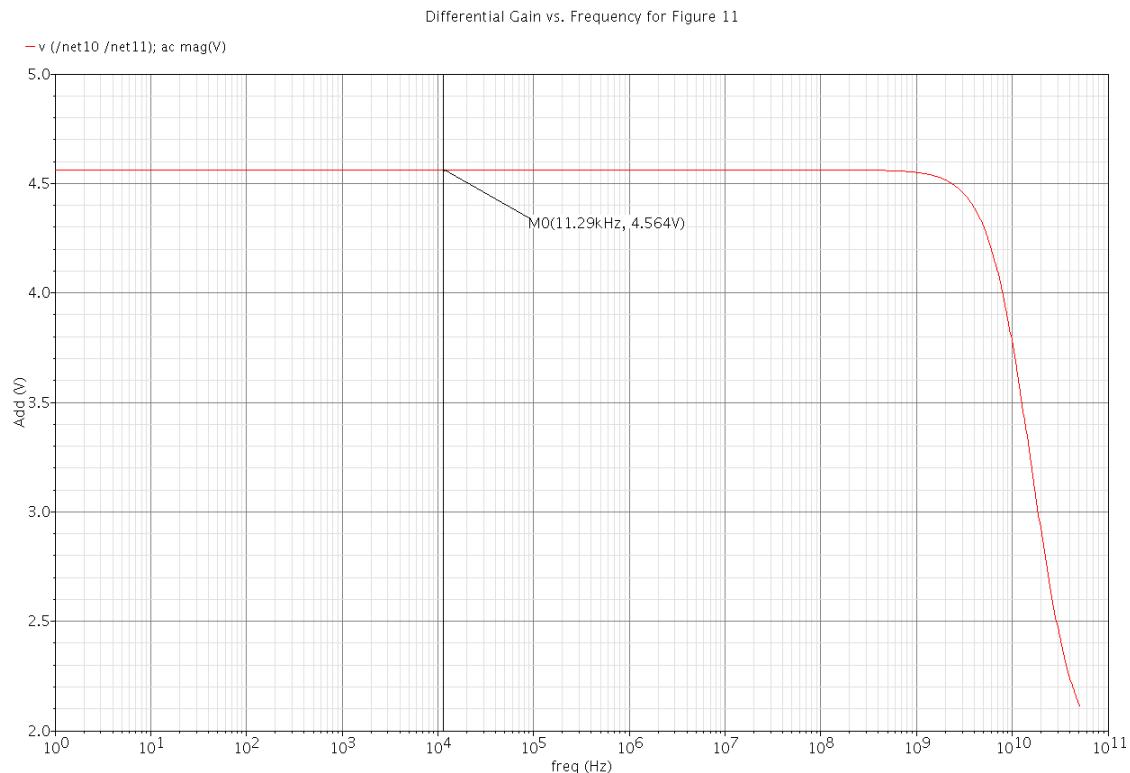


Figure 30: Gain vs. Frequency for Figure 11

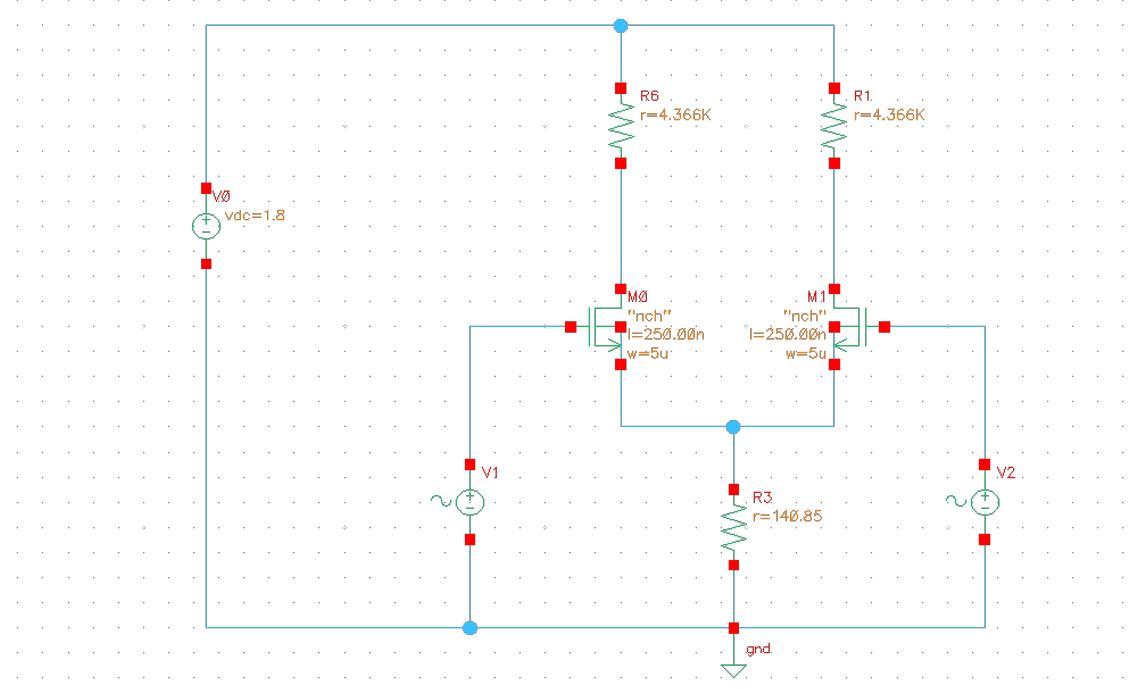


Figure 31: Schematic to Verifying Gain Calculations for Figure 12

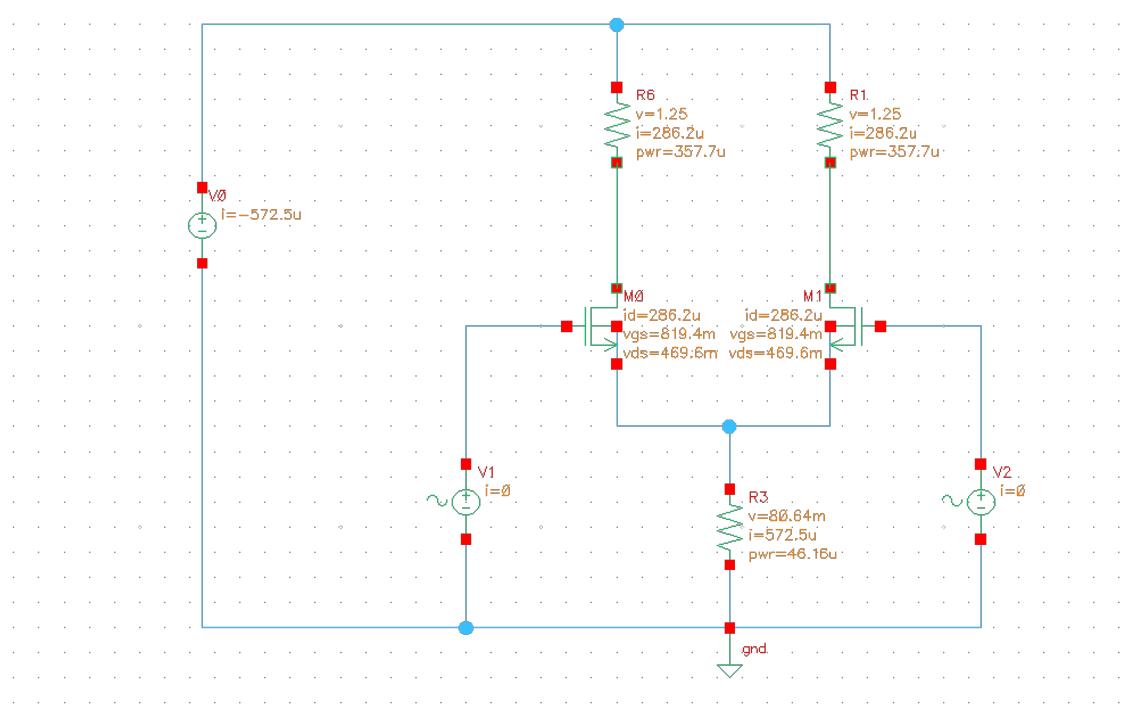


Figure 32: Schematic with DC Operating Point Annotations to Verifying Gain Calculations for Figure 12

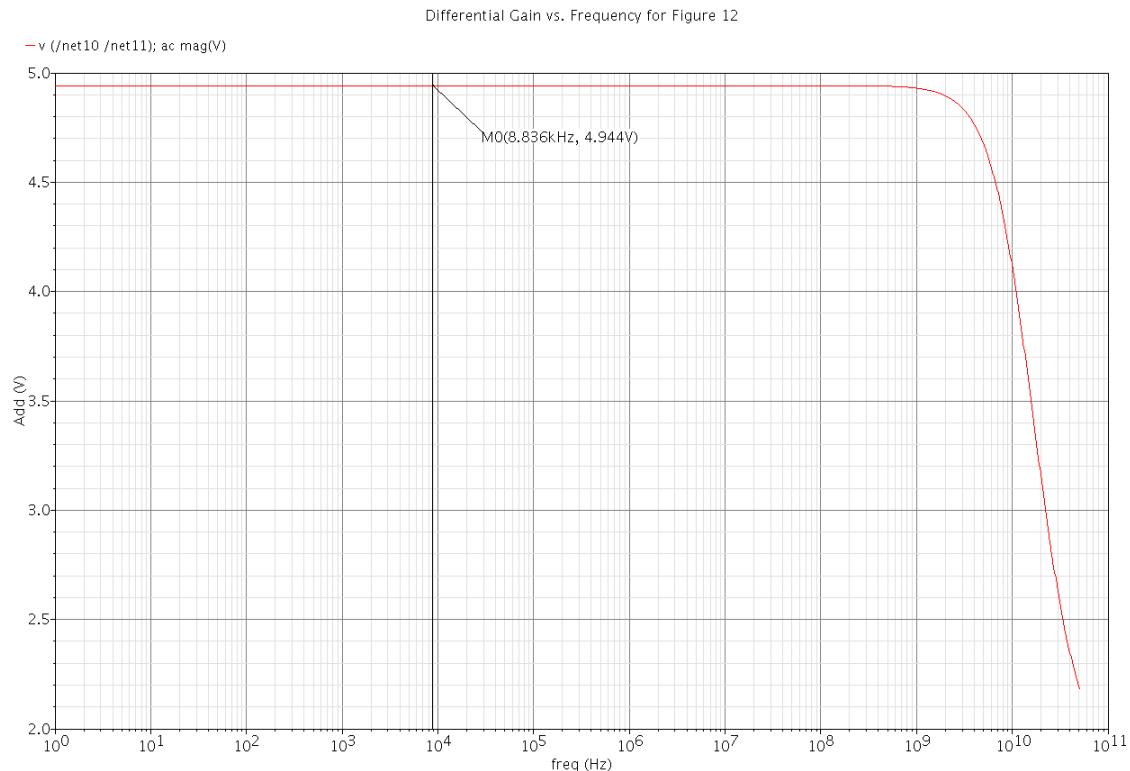


Figure 33: Gain vs. Frequency for Figure 12

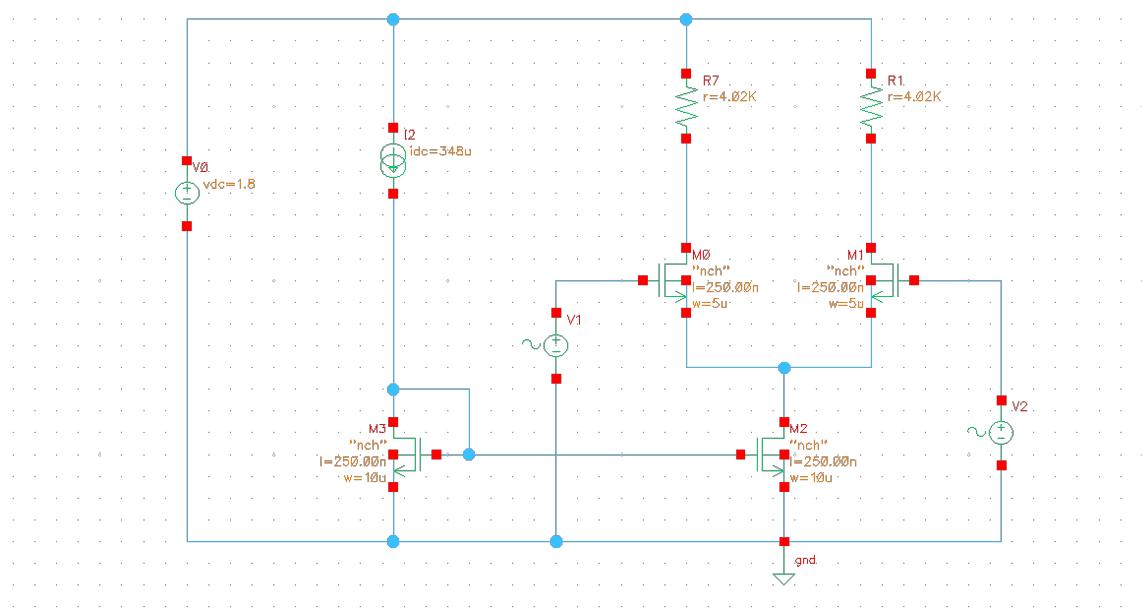


Figure 34: Schematic to Verifying Gain Calculations for Figure 13

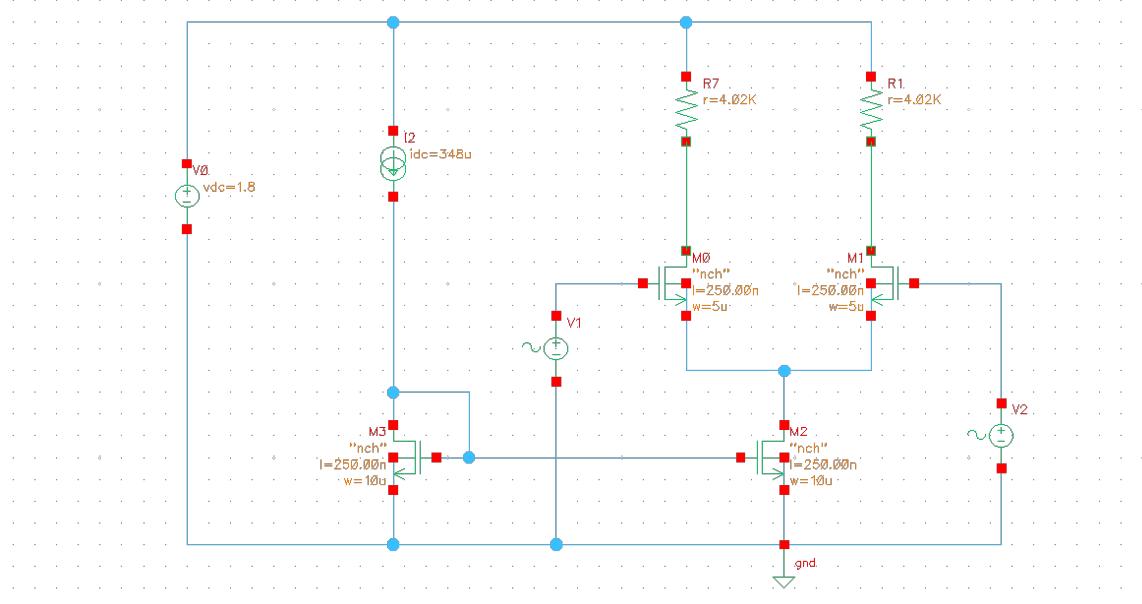


Figure 35: Schematic with DC Operating Point Annotations to Verifying Gain Calculations for Figure 13

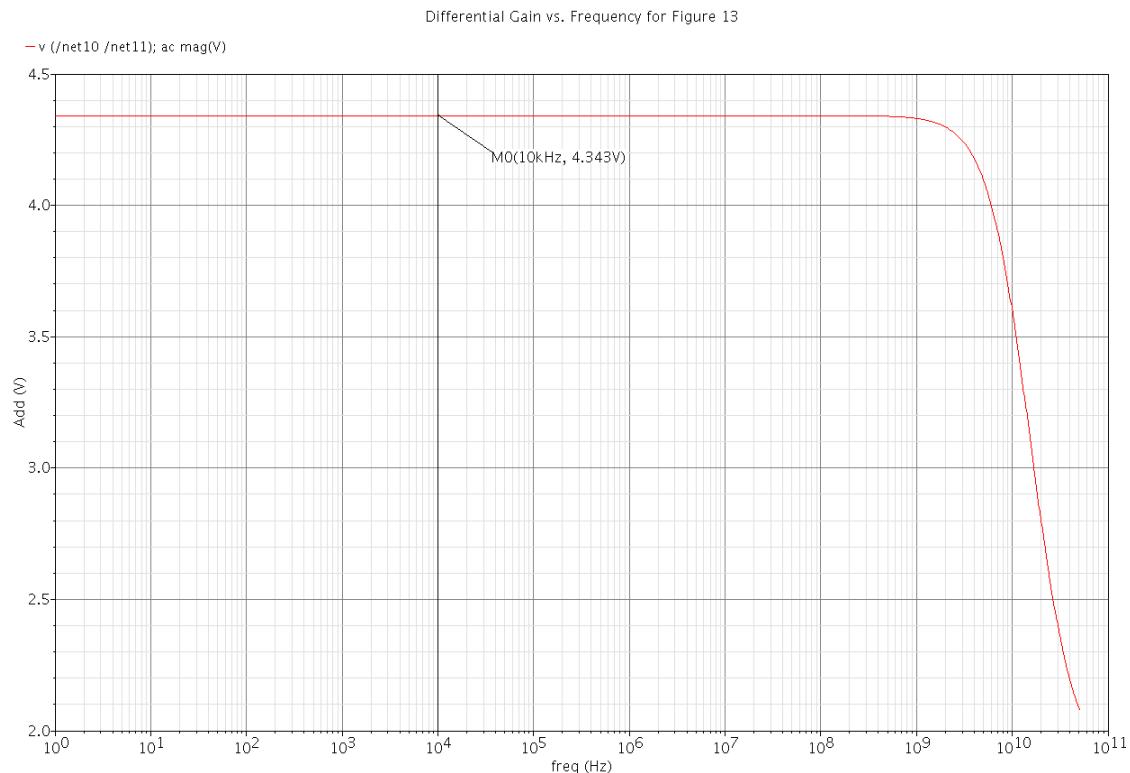


Figure 36: Gain vs. Frequency for Figure 13

3.2

In this problem I plotted the I-V transfer characteristics for the three differential stages. The first utilizes an ideal current source and thus has a close to perfect butterfly diagram plot. The second utilizes a resistor current source which does not hold the total current through the pair steady. As can be seen, the current actually rises above the $20\mu A$ current initially calculated. However, the butterfly curve can still be seen in the transfer characteristic of this configuration. The third circuit utilizes a current mirror source. Because the transistor cannot act as a perfect current source, the current never saturates and continues to rise as the drain voltage of M0 rises (as a result of the gate voltage of the "ON" transistor at any given time). Also, there is a section of the plot where both currents are off which is a result of the 500mV threshold voltage of each device.

The required voltage to switch on just one of the input transistors as discussed in class is

$$V_{ON} = \sqrt{2}V_{OV} = 0.28V \quad (1)$$

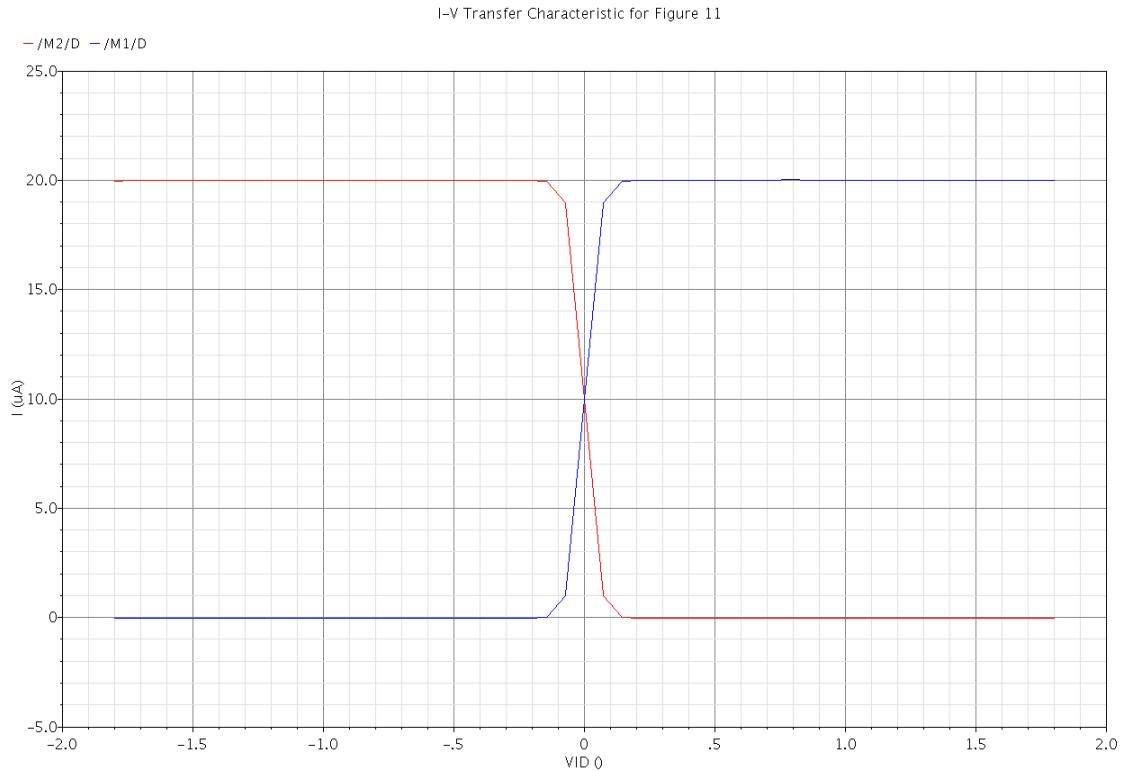


Figure 37: Current Through Each Transistor of the Diff Pair in Figure 11 vs. Differential Input Voltage

I-V Transfer Characteristic for Figure 12

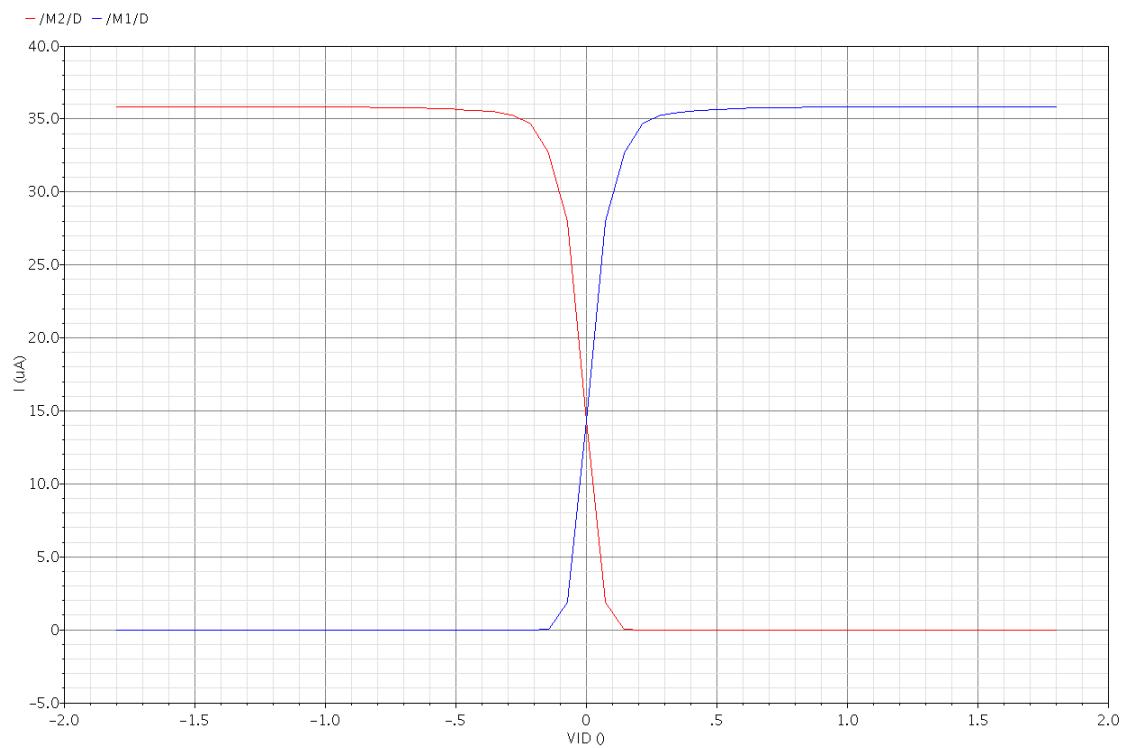


Figure 38: Current Through Each Transistor of the Diff Pair in Figure 12 vs. Differential Input Voltage

I-V Transfer Characteristic for Figure 13

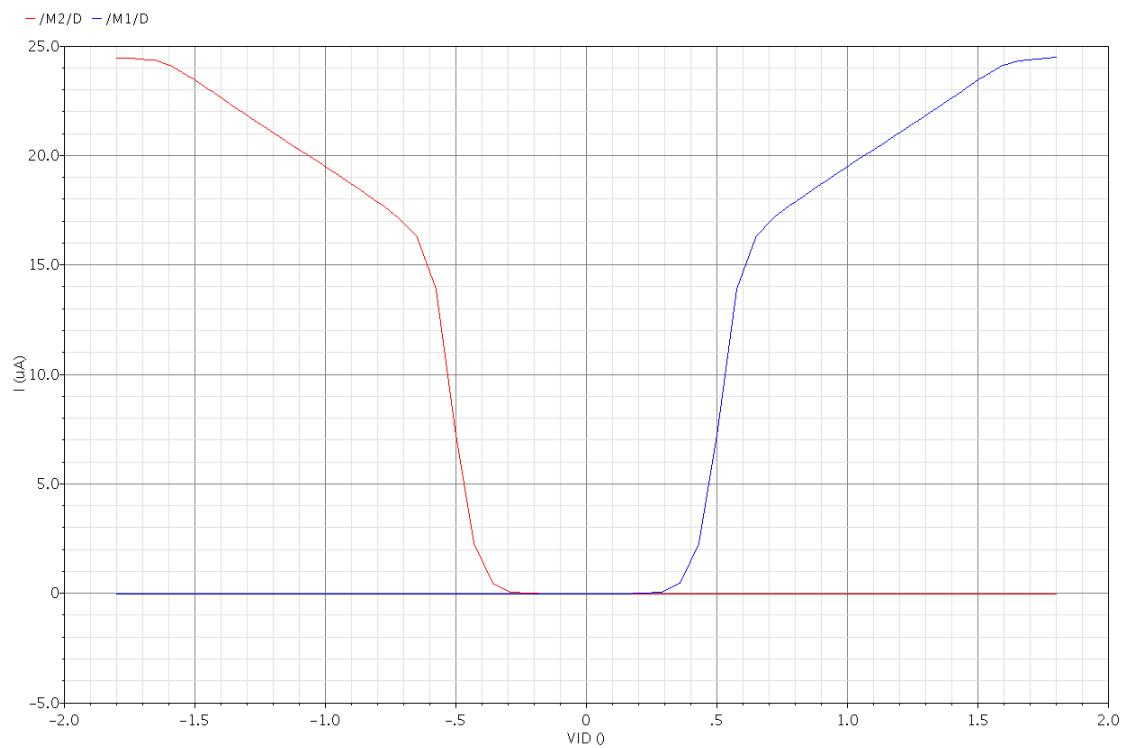


Figure 39: Current Through Each Transistor of the Diff Pair in Figure 13 vs. Differential Input Voltage

3.3

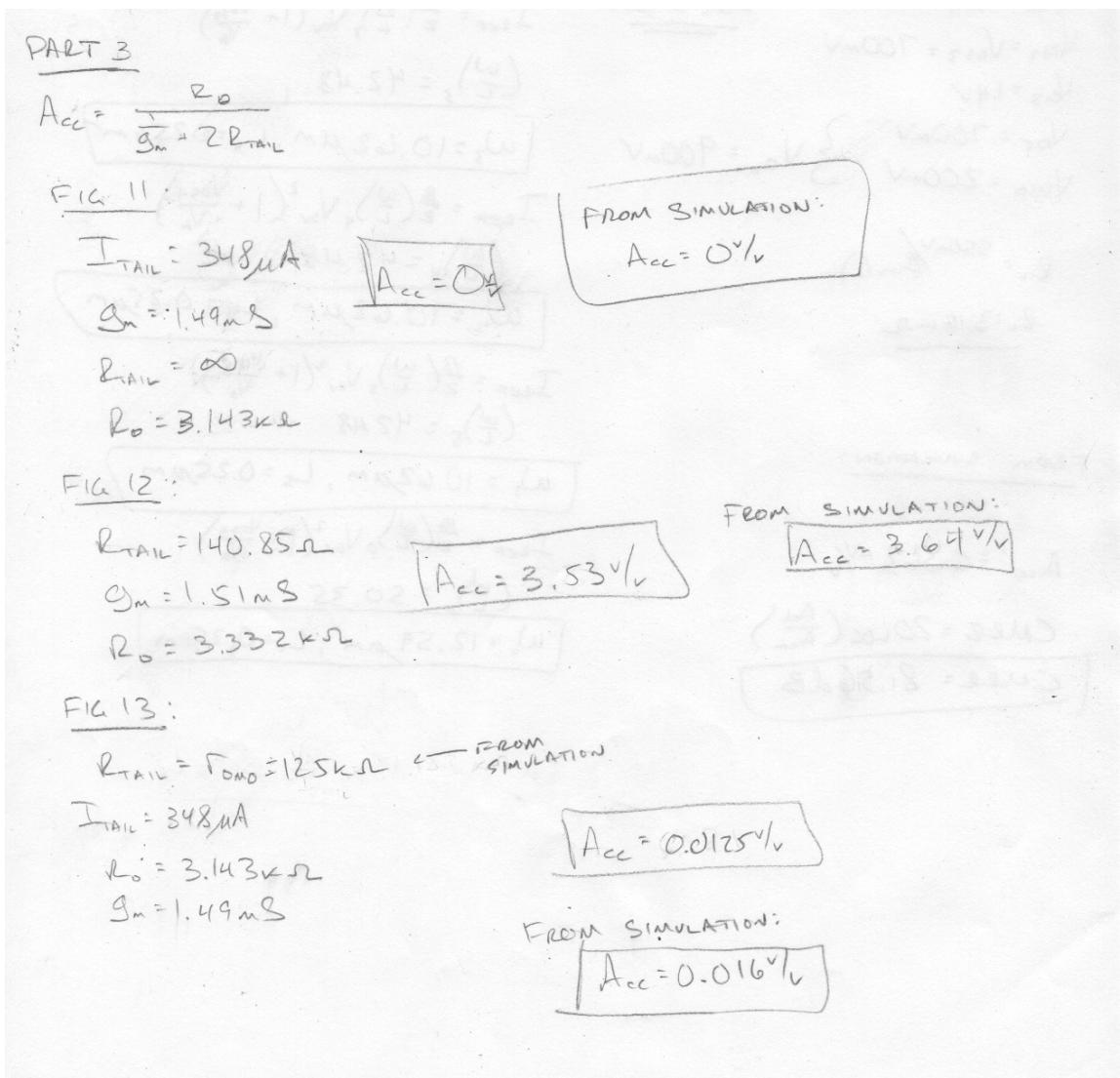


Figure 40: Hand-Written Work for Problem 3.3

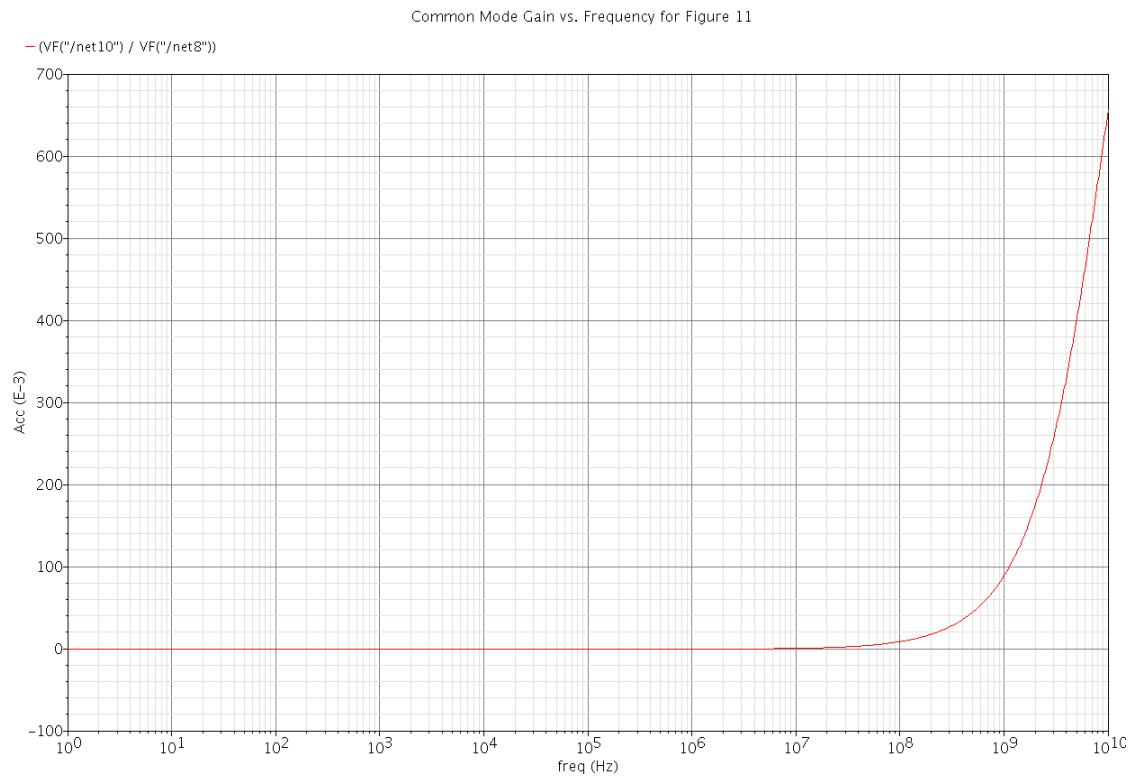


Figure 41: Common Mode Gain vs. Frequency for Figure 11

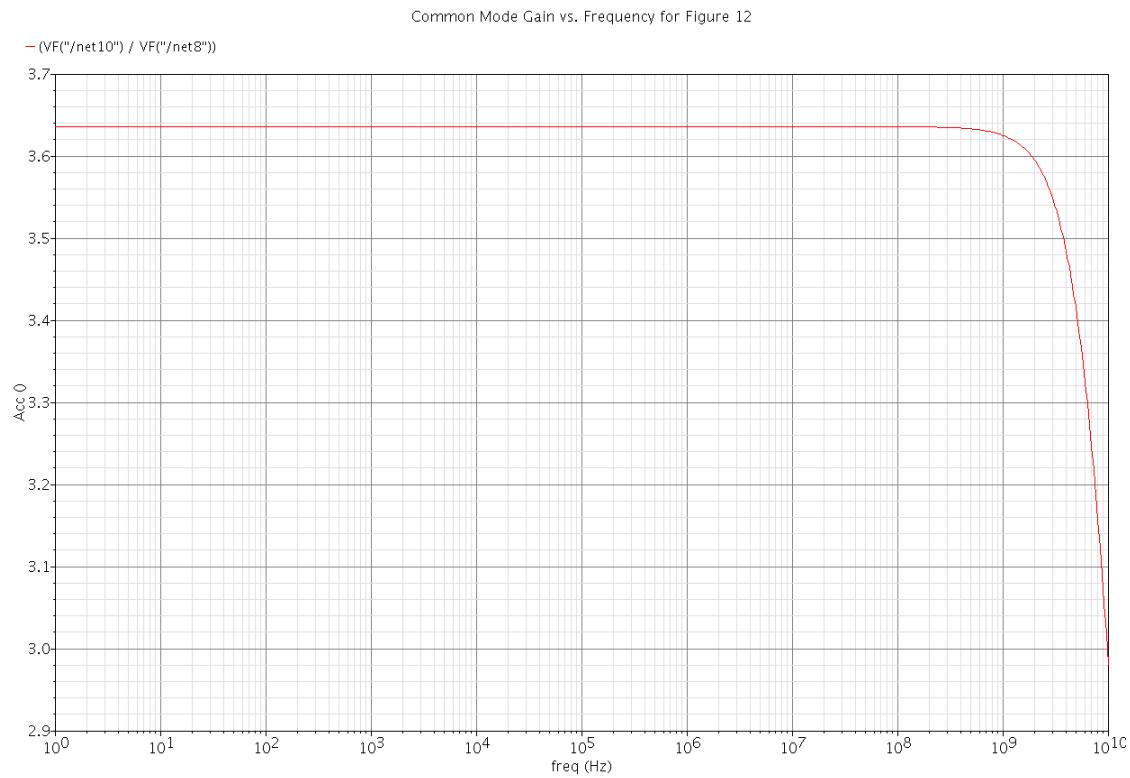


Figure 42: Common Mode Gain vs. Frequency for Figure 12

Common Mode Gain vs. Frequency for Figure 13

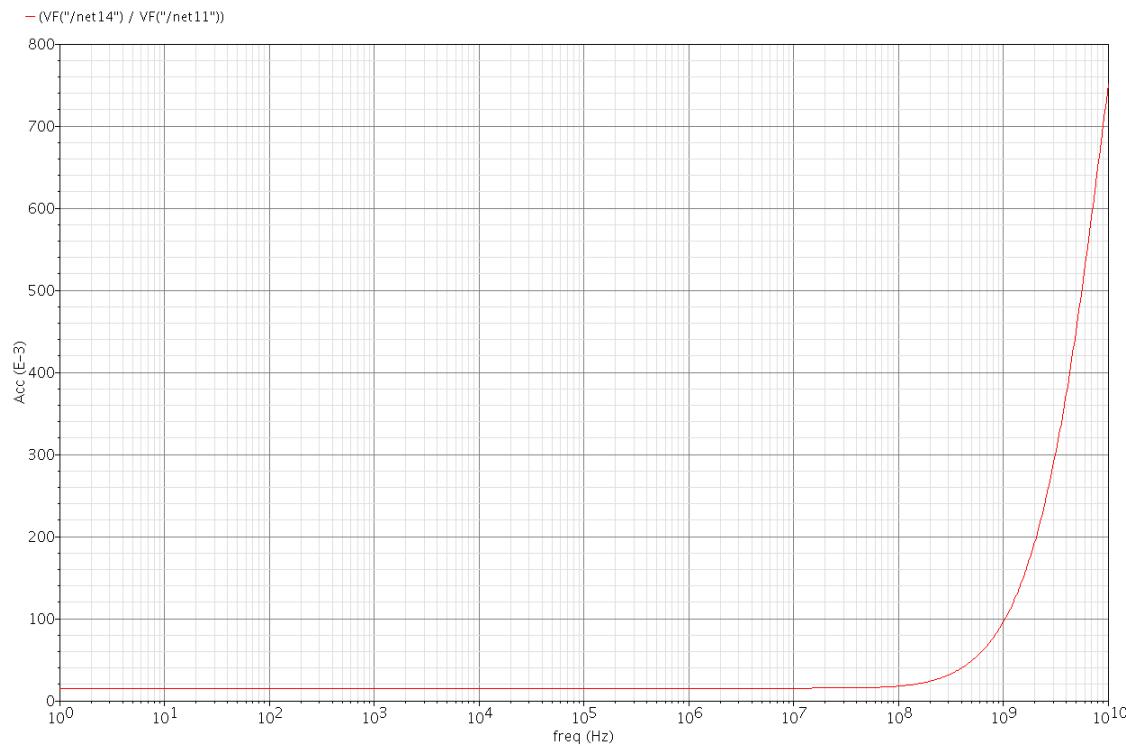


Figure 43: Common Mode Gain vs. Frequency for Figure 13

3.4

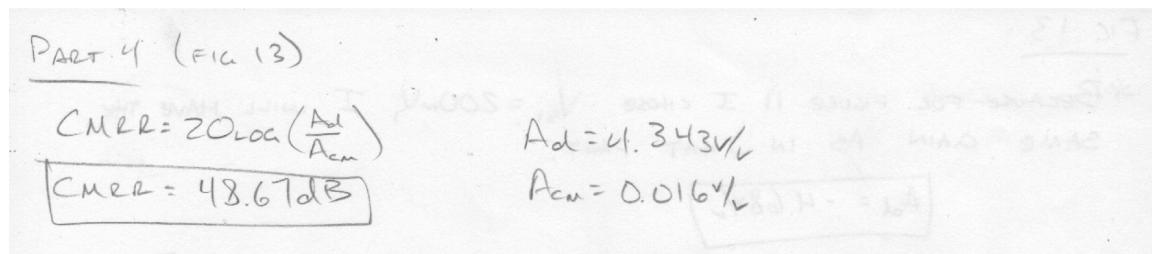


Figure 44: Hand-Written Work for Problem 3.4

3.5

CMRR can be increased by increasing the resistance of the current source (R_{SS}). To do this, we utilize the cascade current mirror as developed earlier in the problem set.

PART 5

FROM PART 1

$$\begin{aligned} V_{DS4} &= V_{GS4} = 700 \text{ mV} \\ V_{DS3} &= V_{GS3} = 700 \text{ mV} \\ V_{B3} &= 1.4 \text{ V} \\ V_{DS} &= 700 \text{ mV} \\ V_{DS0} &= 200 \text{ mV} \end{aligned}$$

$$\left. \begin{aligned} I_{T\text{AIL}} &= 348 \mu\text{A} \\ \left(\frac{w}{l}\right)_3 &= 42.48 \\ \boxed{W_3 = 10.62 \mu\text{m}, L_3 = 0.25 \mu\text{m}} \end{aligned} \right\} V_{O\text{o}} = 900 \text{ mV}$$

$$R_L = \frac{550 \text{ mV}}{(I_{T\text{AIL}}/2)}$$

$$\underline{R_L = 3.16 \text{ k}\Omega}$$

$$\begin{aligned} I_{REF} &= \frac{\beta}{2} \left(\frac{w}{l} \right)_3 V_{ov}^2 \left(1 + \frac{V_{DS3}}{V_A} \right) \\ \left(\frac{w}{l} \right)_4 &= 42.48 \\ \boxed{W_4 = 10.62 \mu\text{m}, L_4 = 0.25 \mu\text{m}} \end{aligned}$$

$$\begin{aligned} I_{REF} &= \frac{\beta}{2} \left(\frac{w}{l} \right)_4 V_{ov}^2 \left(1 + \frac{V_{DS4}}{V_A} \right) \\ \left(\frac{w}{l} \right)_5 &= 42.48 \\ \boxed{W_5 = 10.62 \mu\text{m}, L_5 = 0.25 \mu\text{m}} \end{aligned}$$

FROM SIMULATION:

$$A_{ac} = 0.363 \text{ mV/V}$$

$$\boxed{CMRR = 20 \log \left(\frac{A_{ac}}{A_{cm}} \right)}$$

$$\boxed{CMRR = 81.56 \text{ dB}}$$

$$\begin{aligned} I_{REF} &= \frac{\beta}{2} \left(\frac{w}{l} \right)_0 V_{ov}^2 \left(1 + \frac{V_{DS0}}{V_A} \right) \\ \left(\frac{w}{l} \right)_0 &= 50.35 \\ \boxed{W_0 = 12.59 \mu\text{m}, L_0 = 0.25 \mu\text{m}} \end{aligned}$$

Figure 45: Hand-Written Work for Problem 3.5

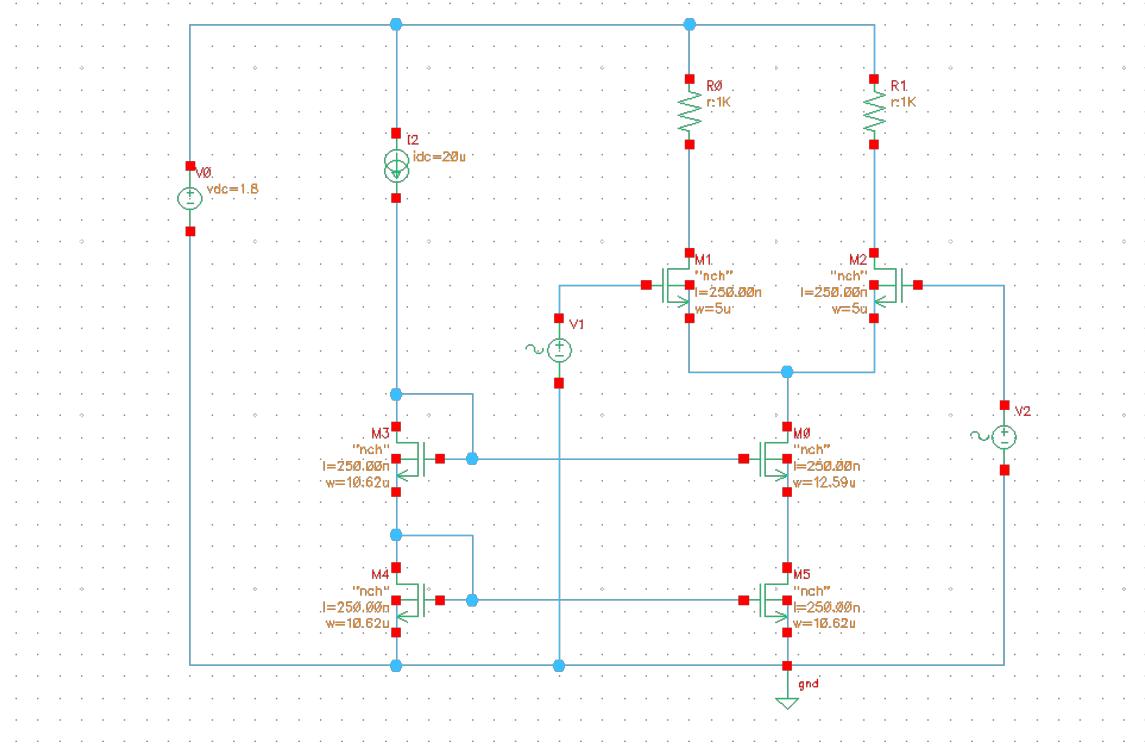


Figure 46: Schematic to Improve CMRR of the Differential Amplifier