EE6312-HOMEWORK III

Describe your reasoning for your design and calculations. Provide the simulations set-ups you used for this problem set and provide the necessary simulation results (operating point, plots, ...) to document your findings. Make sure you provide sufficient information, but not too much information either. The grade will depend both on the quality of the results as well as the quality of the succinct, but insightful description of your reasoning and calculations.

Problem 1

In this problem, we investigate biasing schemes for IC design. Unlike discrete component design, in IC design we prefer to avoid AC coupled stages unless otherwise necessary and hence proper design of bias circuits is essential.

Consider the biasing of the differential pair shown in Fig1, Fig2, Fig3. All device sizes are indicated in the following table. The differential pair is intended to be operated with all transistors in saturation in strong inversion. In other words, assume that the input signals to the differential pair are small and swing around some bias voltage v_{bias2}(or equivalently the current through the two transistors M2, M3 varies around $\frac{I_{tail}}{2}$).

Parameter vs. Value	
Parameter	Value
$W/L(M0)$	2.5 μm/0.25 μm
$W/L(M1)$	2.5 μm/0.25 μm
$W/L(M2)$	1.25 μm/0.25 μm
$W/L(M3)$	1.25 μm/0.25 μm

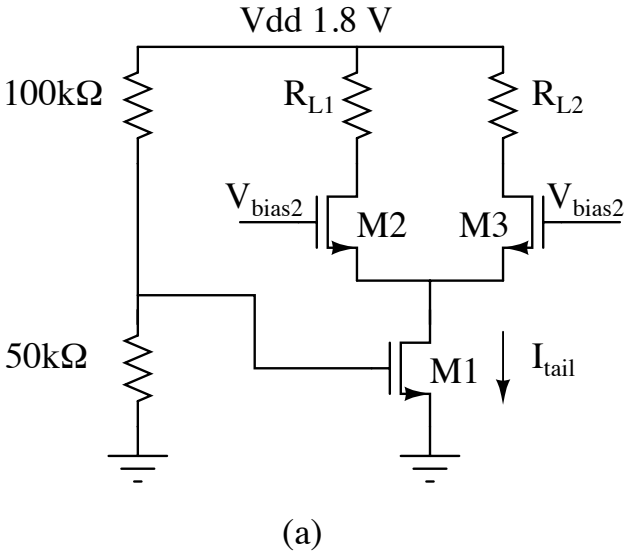

Figure 1: Biasing Scheme (a)

- Assuming a square law model with $\beta = 320\ \frac{\mu A}{V^2}$ where
  $I_{DS} = \frac{\beta}{2}\frac{W}{L}(V_{GS} - V_{th})^2$ and a $V_{th} = 500\ mV$, calculate the tail current I_{tail} marked in the circuit. Calculate the g_m of the transistors M2, M3. Find the values of R_{L1} and R_{L2} for maximum gain. What are the limitations and trade-offs?

- Due to various imperfections in IC fabrication, temperature variations and other reasons, the parameters β, V_{th} etc., change from one chip to another. These are termed process corner and temperature variations. A slow corner is one in which V_{th} is higher than typical and a fast corner is one in which V_{th} is lower than typical.

  Suppose due to process corner variations, V_{th} changes to 550 mV. Calculate I_{tail} and g_m of M2, M3 now. What do you observe? This is the reason why biasing with a voltage is to be avoided in IC design.

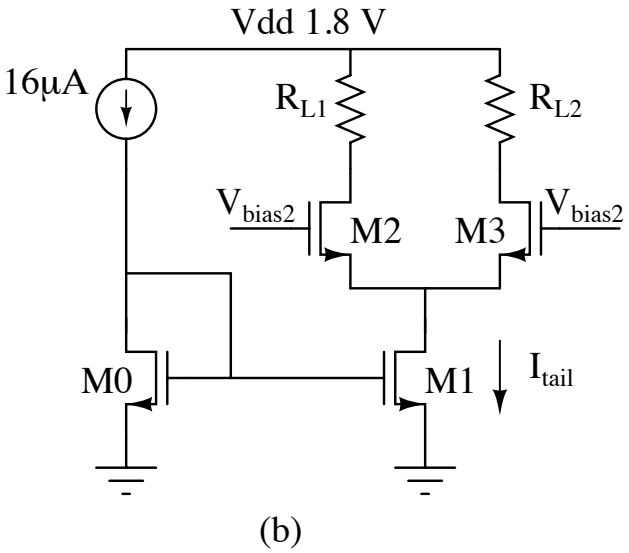

Figure 2: Biasing Scheme (b)

- Here (Fig2) the gate voltage applied to the transistor M1is obtained by biasing a similar transistor (M0) using a reference current source. If we assume all transistors have infinite output impedance, what is the current I_{tail}? If instead the transistors M0 and M1 have a $g_m r_o$ of 10, and the drain of M1 is assumed to be at 550 mV, what is the value of I_{tail}? (Hint: use small signal analysis to provide a rough estimate of the current)

- Assuming square law, what is the minimum bias voltage (in terms of V_{th} and I_{ref}) required for the gates of M2 and M3? How will you generate this voltage without any additional current source? How sensitive is the circuit to this voltage?

- Here (Fig3) we try to further improve the current mirrored in to M1. What do you think is the reason behind a claim that this scheme is better than the scheme shown in Fig2? For best results, what should the size of the device M4?

- Additional credit: If instead of operating the transistors M2 and M3 such that both of them are in saturation and strong inversion, we operate such that the current is always present in either M2 or M3. In other words, at any point of time, one of M2 and M3 carries I_{tail} and the other will carry no current. Then what would be the best choice for the size of the device M4?

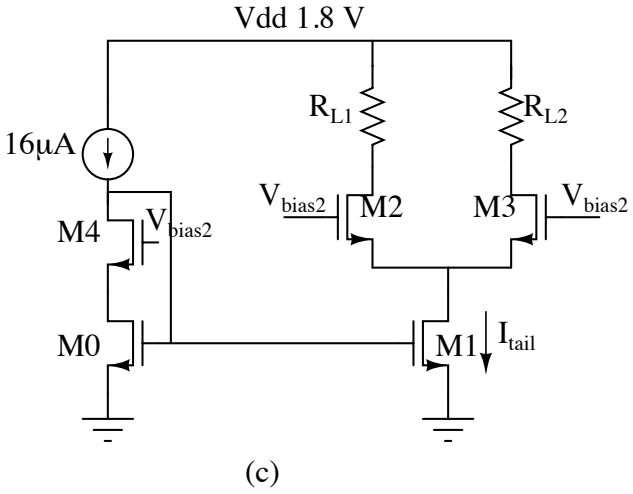

Figure 3: Biasing Scheme (c)

Problem 2

In this exercise you will investigate the various current mirror configurations and trade-offs. Consider the transistor M1 shown in Fig4. We wish to fix the current in M1 to I_{ref}. Due to the unilaterality of a transistor, feedback is required.

Let's start analyzing the circuit without a gate-drain diode connection. When the current I_1 through the transistor does not match with the desired current, I_{ref}, the drain node voltage is undefined (V_D). Consider the case $I_{ref} > I_1$, drain voltage of M1 increases and gate voltage of M1 should be increased or source voltage of M1 should be decreased to match the two currents. Due to non-inverting nature of feedback, a unity gain amplifier can be used to realize the feedback for simplicity. This collapses to the well known diode current mirror.

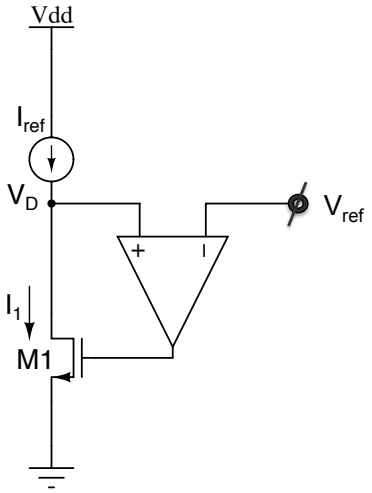

Figure 4: Basic Idea of Current Mirror

- Consider the basic current mirror configuration shown in Fig5. For a fixed V_{DS} voltage, calculate the actual current at the drain of M2 by considering g_{ds} of M2. What is the error of mirrored current ($\frac{\Delta I}{I} = \frac{I_o - I_{ref}}{Iref} * 100$)? This is the reason why high output impedance ($\frac{1}{g_{ds}}$) is preferred.

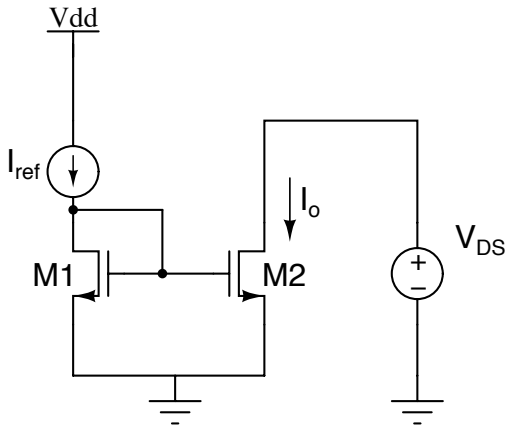

Figure 5: Basic Current Mirror Configuration

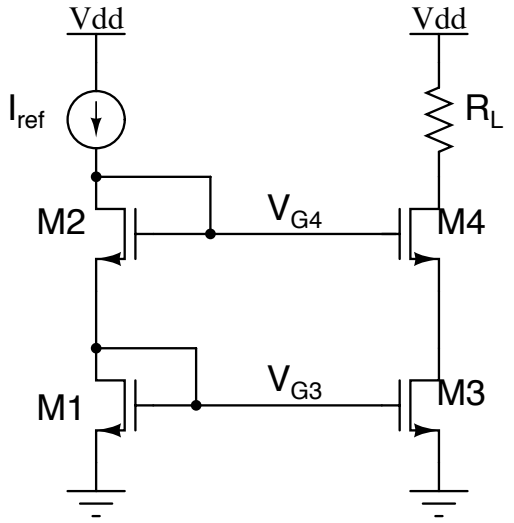

Figure 6: Cascode Current Mirror Configuration

- Calculate the output impedance of the cascode current mirror configuration shown in Fig6 in terms of small signal parameters. According to your calculations, size the transistors properly to get 1%, 10% accuracy from the cascode current mirror for $V_{GS} - V_{th} = 200\ mV$, $I_{ref} = 1\ mA$ and $R_L = 500\Omega$.
- Plot the error of mirrored current vs V_{DS} for the current mirrors in Fig5 by sweeping V_{DS}, in Fig6 by sweeping the drain voltage of M4 and observe when the error is largest. The compliance is the smallest voltage at the output of the current source. Calculate the compliance of the realized current source.
- What is the minimum voltage required at the gate of M4 to have all devices in saturation? Compare it against the voltage used in Fig6. Fig 7 is one of the ways to realize this voltage at the gate of M4. What should be the voltage drop on R_1 and calculate the required R_1 value. Size the transistors properly to get 1% accuracy from the cascode current mirror for $V_{GS} - V_{th} = 200\ mV$, $I_{ref} = 1\ mA$ and $R_L = 500\Omega$. Indicate the regions of operation of the transistors in Fig7.
- Generally we avoid using R_1 because the voltage drop on R_1 required will change with PVT variations. R_1 is replaced by transistor realization shown in Fig8. Size the transistors properly to get 1% accuracy from the cascode current mirror for $V_{GS} - V_{th} = 200\ mV$, $I_{ref} = 1\ mA$ and $R_L = 500\Omega$. Indicate the regions of operation of the transistors in Fig8.

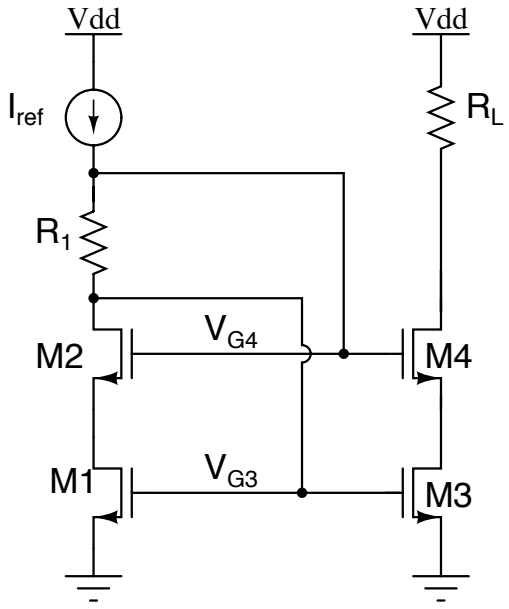

Figure 7: Self Biased Current Mirror Configuration 1

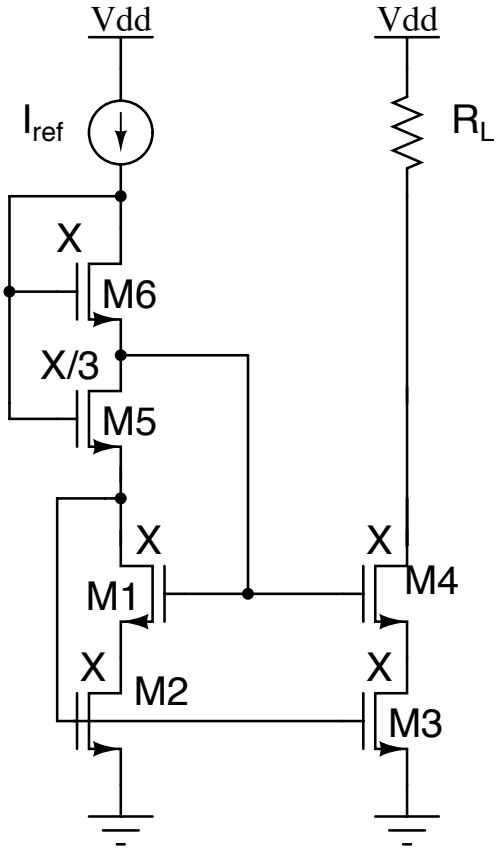

Figure 8: Self Biased Current Mirror Configuration 2

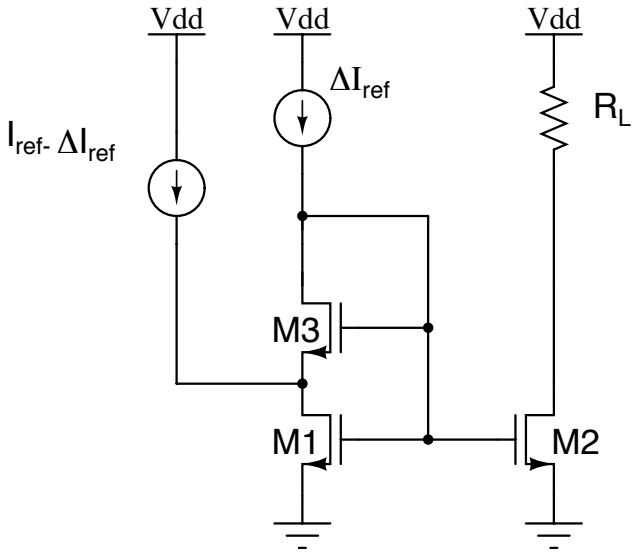

Figure 9: Current Mirror Configuration 3

- For highly scaled technologies, self-biased current mirror configuration shown in Fig8 isn't preferred because of threshold voltage dependence on L. Another current mirror configuration is shown in Fig9. Calculate the V_{GS} and V_{DS} of M3. To obtain the required V_{GS}, keep the widths of all the transistors comparable and length the same, and size them properly to get 1% accuracy from this current mirror for $V_{GS} - V_{th} = 200\ mV$ for M1 and M2, $I_{ref} = 1\ mA$ and $R_L = 500\Omega$. Assume ΔI_{ref} is really small.

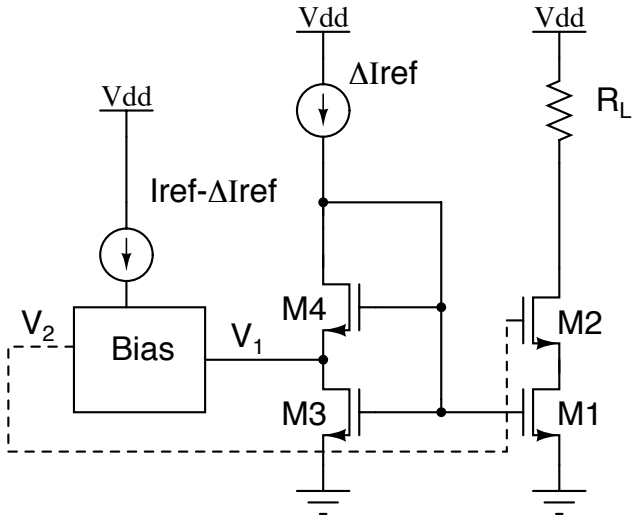

Figure 10: Current Mirror Configuration 4

- **Additional credit:** Find out the smallest the gate voltages of M1 and M2 for cascode configuration. To obtain these gate voltages, we use a current mirror configuration shown in Fig10. Calculate the V_1 and V_2 shown in Fig10. Replace the Bias block with an appropriate transistor realization. Size the transistors properly to get 1% accuracy from this current mirror for $V_{GS} - V_{th} = 200\ mV$, $I_{ref} = 1\ mA$ and $R_L = 500\Omega$.

Problem 3

In this exercise you will investigate the basic differential pair configuration, large signal analysis and small signal analysis. All device sizes are indicated in the following table and $V_{SB} = 0\ V$. Begin your analysis by assuming that M1 and M2 are perfectly matched.

Parameter vs. Value	
Parameter	Value
$W/L(M1)$	5 μm/0.25 μm
$W/L(M2)$	5 μm/0.25 μm
$W/L(M0)$	10 μm/0.25 μm
$W/L(M3)$	10 μm/0.25 μm

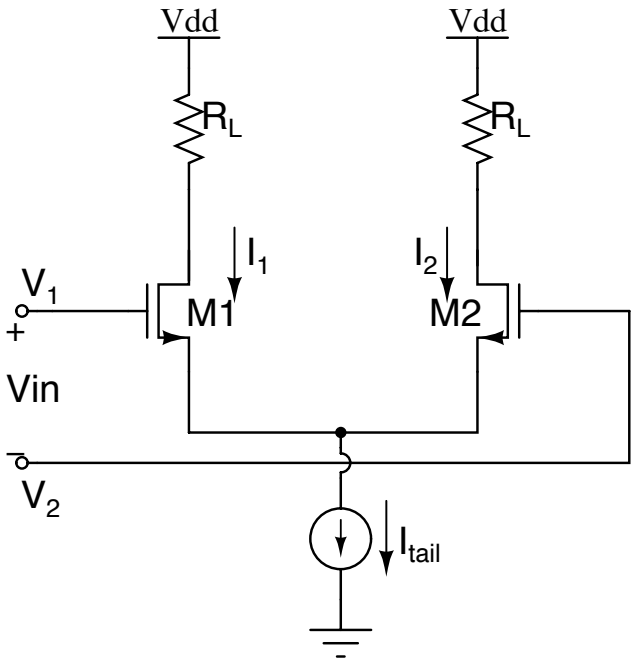

Figure 11: Basic Differential Pair Configuration with Ideal Current Source

- Calculate the differential mode gain (A_d) for Fig11, Fig12 and Fig13. Provide simulation result for differential mode gain ($V_1 = 0.5$, $V_2 = -0.5$ for AC analysis).
- Now analyze the large signal characteristic of basic differential pair. Plot I_1 and I_2 vs. V_{in} curve (I-V transfer characteristic) by sweeping differential input voltage from 0 to V_{DD} for $I_{tail} = 20\ \mu A$, $R_L = 30\ K\Omega$ and $R_S = 20\ K\Omega$. Calculate the required value of input voltage to switch current through just one of the input transistors.

- Calculate and simulate the common mode gain (A_{cm}) for the following cases shown in Fig11, Fig12 and Fig13 ($V_1 = 1$, $V_2 = 1$ for AC analysis).
- Common mode rejection ratio is defined as the tendency of the devices to reject the input signals common to both inputs of a differential pair and is given by $CMRR = 20 \log |\frac{A_d}{A_{cm}}|$. Calculate the CMRR for transistor realization of current source shown in Fig13.
- How do you increase the CMRR? Provide the circuit to increase CMRR considering your previous design background.

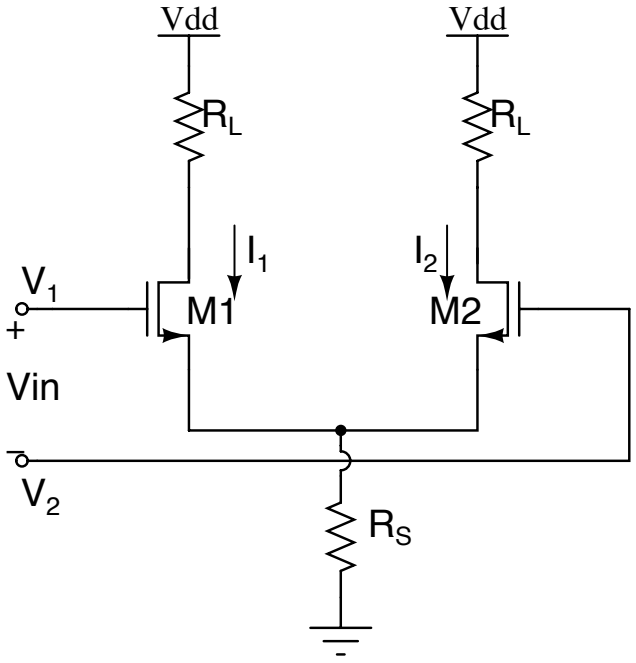

Figure 12: Basic Differential Pair Configuration with R_S

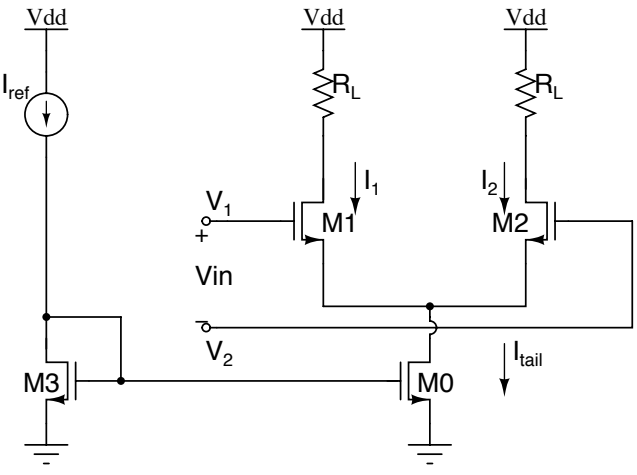

Figure 13: Basic Differential Pair Configuration with Current Source Transistor