EE6312-HOMEWORK IV

Describe your reasoning for your design and calculations. Provide the simulations set-ups you used for this problem set and provide the necessary simulation results (operating point, plots, ...) to document your findings. Make sure you provide sufficient information, but not too much information either. The grade will depend both on the quality of the results as well as the quality of the succinct, but insightful description of your reasoning and calculations.

Problem

In this exercise you will investigate a single-ended OTA configuration and its frequency response, settling and slew-rate.

DC Bias of OTA

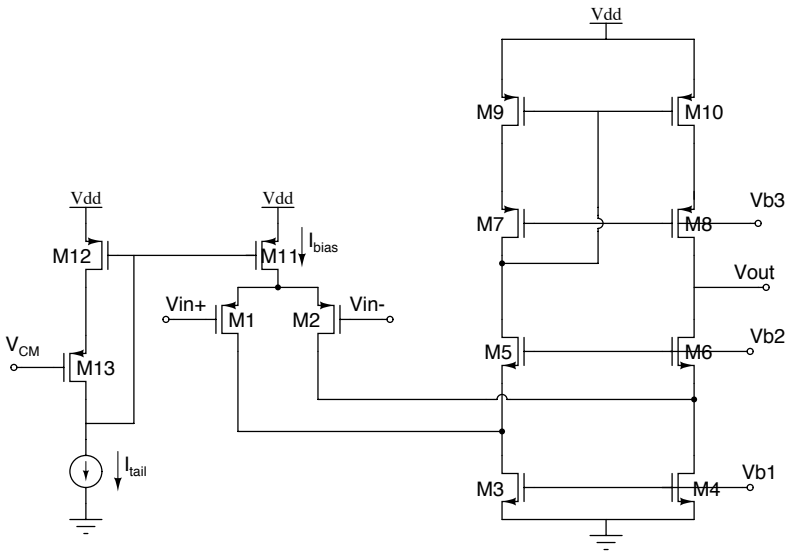
Consider the sized folded cascode OTA shown in Fig1(a). All device sizes are indicated in the following table. The OTA is going to be used in the application shown in Fig1(b).

Parameter vs. Value	
Parameter	Value
$W/L(M1)$	42 μm/0.4 μm
$W/L(M2)$	42 μm/0.4 μm
$W/L(M3)$	21 μm/0.4 μm
$W/L(M4)$	21 μm/0.4 μm
$W/L(M5)$	10.5 μm/0.4 μm
$W/L(M6)$	10.5 μm/0.4 μm
$W/L(M7)$	42 μm/0.4 μm
$W/L(M8)$	42 μm/0.4 μm
$W/L(M9)$	42 μm/0.4 μm
$W/L(M10)$	42 μm/0.4 μm

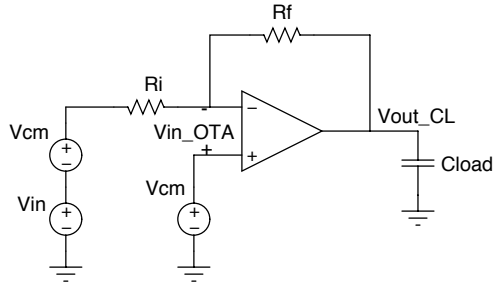
- [*Hand Calculation*] Determine V_{cm} for maximum signal swing ($V_{cm} = \frac{V_{in+}+V_{in-}}{2}$).
- [*Hand Calculation − Simulation*] As a first step, determine V_{b1}, V_{b2} and V_{b3} bias voltages for maximum signal swing and obtain these bias voltages by proper transistor realization for $I_{bias} = 320\mu A$, $V_{SB} = 0\ V$ and $V_{dd} = 1.8\ V$. Current through M3/M4 is $320\mu A$. Size M11, M12 and M13 bias transistors appropriately for $I_{bias} = 320\mu A$ by keeping length of the transistors same ($L = 0.4\ \mu m$).

OTA in Isolation

- [*Simulation*] Do a DC simulation to get V_{out_OL} vs. V_{in_OTA} when OTA is stand alone as shown in Fig2(a).
- [*Simulation*] Do an AC simulation by using schematic shown in Fig2(b) to get open loop gain A(s) of OTA which is V_{out_OL}/V_{in_OTA} (Bode plot). Estimate poles, zeros and gain-bandwidth product. Use the C_{load} value from the table. Replace the feedback box shown in Fig2(b) by the appropriate ideal circuit realization to provide the feedback necessary for simulation purposes.
- [*Hand Calculation*] Find dominant, non dominant poles and the gain-bandwidth product.



(a) Folded Cascode OTA



(b) Folded Cascode OTA in Feedback Configuration

Figure 1: (a) Folded Cascode OTA / (b) Folded Cascode OTA in Feedback Configuration

OTA in Feedback

- [*Simulation*] Determine β, the feedback factor.
- [*Simulation*] Determine the loop gain L(s) by simulation and account for the loading of the practical feedback circuit. Use the OTA placed in negative feedback shown in Fig1(b). All component sizes are indicated in the following table. Choose V_{cm} for maximum signal swing as derived above.

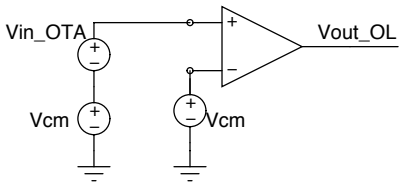
Parameter vs. Value	
Parameter	Value
Ri	2.5 $K\Omega$
Rf	2.5 $K\Omega$
$Cload$	3 pF

- [*Hand Calculation*] Compare L(s) to $\beta A(s)$ and explain the differences.
- [*Hand Calculation*] Derive a theoretical model of the OTA from small signal parameters (.OP information), account for the loading of the practical feedback circuit, and derive a small signal model for the input-output relationship of the feedback system. Find L(s), β analytically and compare to simulation results.

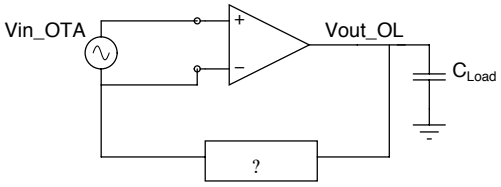
Settling

Small Input Step Settling

- [*Hand Calculation*] What is the ideal behavior? What do you expect theoretically (infinite gain and bandwidth)?
- [*Simulation*] Do a settling simulation for a small input step (i.e. no slewing) by using $\pm 10\ mV$, $\pm 20\ mV$ and $\pm 30\ mV$ input steps. Measure the output voltage (V_{out1}) at $t = 2\tau$ where $\tau \simeq 4.94\ ns$ and measure



(a) Folded Cascode OTA Open Loop Configuration - DC Analysis



(b) Folded Cascode OTA Open Loop Configuration - AC Analysis

Figure 2: (a) Folded Cascode OTA Open Loop Configuration-DC Analysis / (b) Folded Cascode OTA Open Loop Configuration-AC Analysis

the output voltage (V_{out2}) at $t = \infty$ (t=100T for simulation purposes). Then plot $V_{outideal}$ vs. V_{in}, V_{out1} vs. V_{in} and V_{out2} vs. V_{in} on the same graph. Identify the absolute error and the percentage error.

- [*Hand Calculation*] Explain the sources of error and predict them quantitatively by using the DC and AC simulations you did in previous sections.

Large Input Step Settling

- [*Simulation*] Extend the plot for $\pm 100\ mV$, $\pm 200\ mV$ and $\pm 500\ mV$ input steps.
- Explain the deviations from ideal behavior and the sources of error for the $\pm 500\ mV$ input step quantitatively.