

# E6312: Problem Set 4

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## 1 Bullet Point 1

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## 2 Bullet Point 2

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To build the folded cascade OTA, I began by sizing transistors M0, M1, and M2 (see figure 1 for instance names). Because I want  $160\mu A$  through transistor M9 and that transistor is sized with  $W = 42\mu m$  and I want  $320\mu A$  through transistor M2, I sized M2 at  $84\mu A$ . For the sake of convenience, I decided to use a  $320\mu A$  current source so I sized transistors M0 and M1 at  $84\mu A$  as well. In addition, because I will eventually put this circuit into feedback and I would like my output to be close to mid-rail, I set  $V_{cm} = 800mV$  which is close to the ceiling of input voltage. This is an acceptable value because the small signal input will never be above 1V.

To bias  $V_{b1}$ ,  $V_{b2}$ , and  $V_{b3}$  I utilized two branches of self-biasing current mirrors (see Figure 1). The first branch, which consists of one PMOS and four NMOS transistors, serves a number of purposes. The PFET (M21) mirrors current from M0 and cuts it in half (sized  $42\mu A$ ). The four NMOS receive the  $160\mu A$  of current and are sized as follows. M28 will have half the current of M14 and its gate voltage will bias  $V_{b1}$  so it must be half the width of M14,  $10.5\mu m$ . M29 will have the same current as M13 and its gate voltage will bias  $V_{b2}$  so it must be the same width as M13,  $10.5\mu A$ . M27 will also take the same width as M29 and M28. M20 will take one third of that width. Using a very similar methodology, I built the second self-biasing current mirror branch but this time mirroring the current with an NMOS and receiving the current with four PMOS transistors. M31 mirrors the current of  $160\mu A$  so it is sized the same as M28. M44, M45, and M40 will all have the same current as M10 and the gate of M45 will bias  $V_{b3}$  so they are all sized the same as M10 at  $42\mu A$ . M4 is sized one third of that. As can be seen in Figure 2, the biasing is successful.

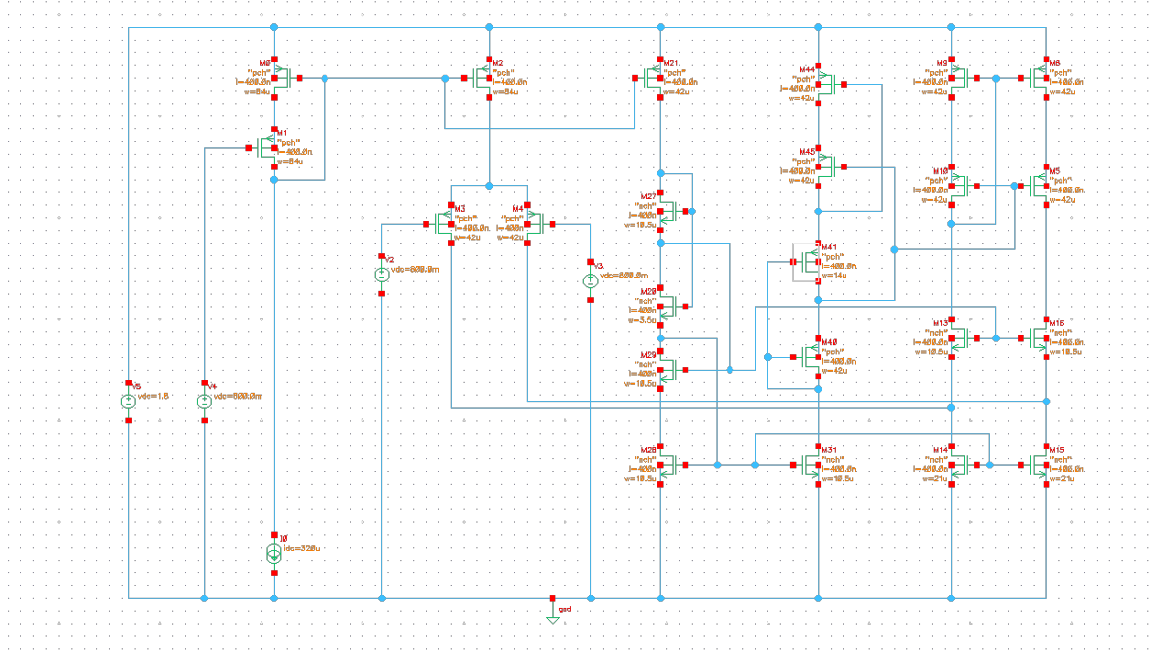


Figure 1: Schematic Diagram for the Folded Cascode OTA with Associated Biasing Circuitry

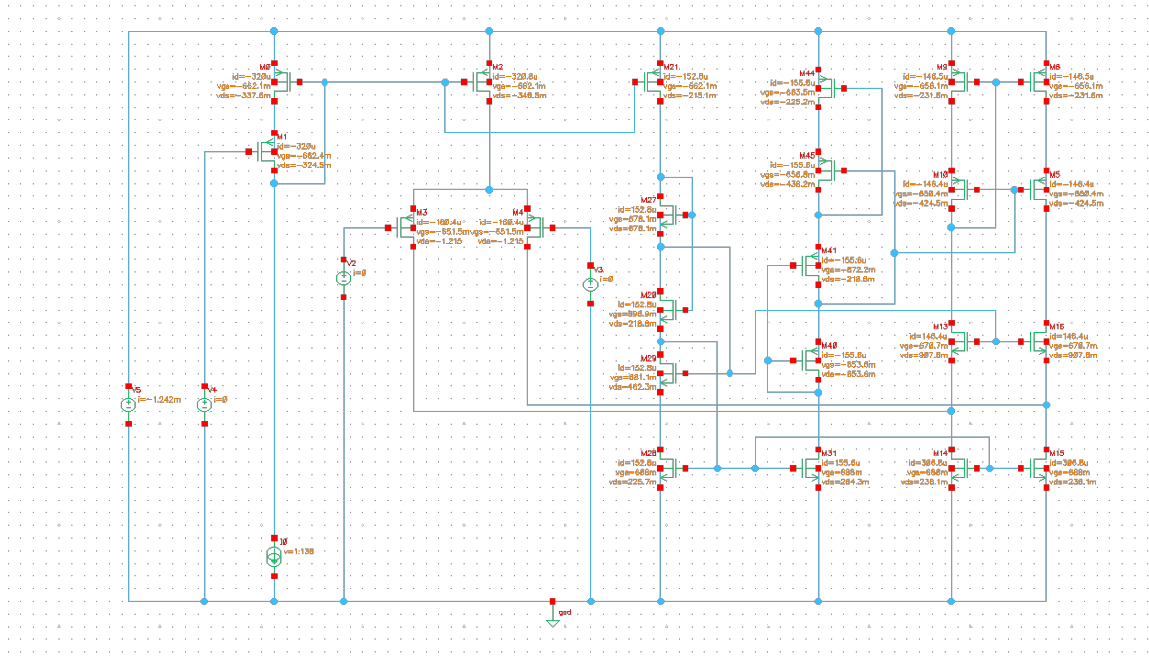


Figure 2: Schematic Diagram for the Folded Cascode OTA with Annotated DC Operating Point Values

### 3 Bullet Point 3

I performed a DC sweep of  $V_{out-OL}$  against  $V_{in-OTA}$  with the OTA in stand alone and the expected transfer function for a differential amplifier is attained (see Figure 3).

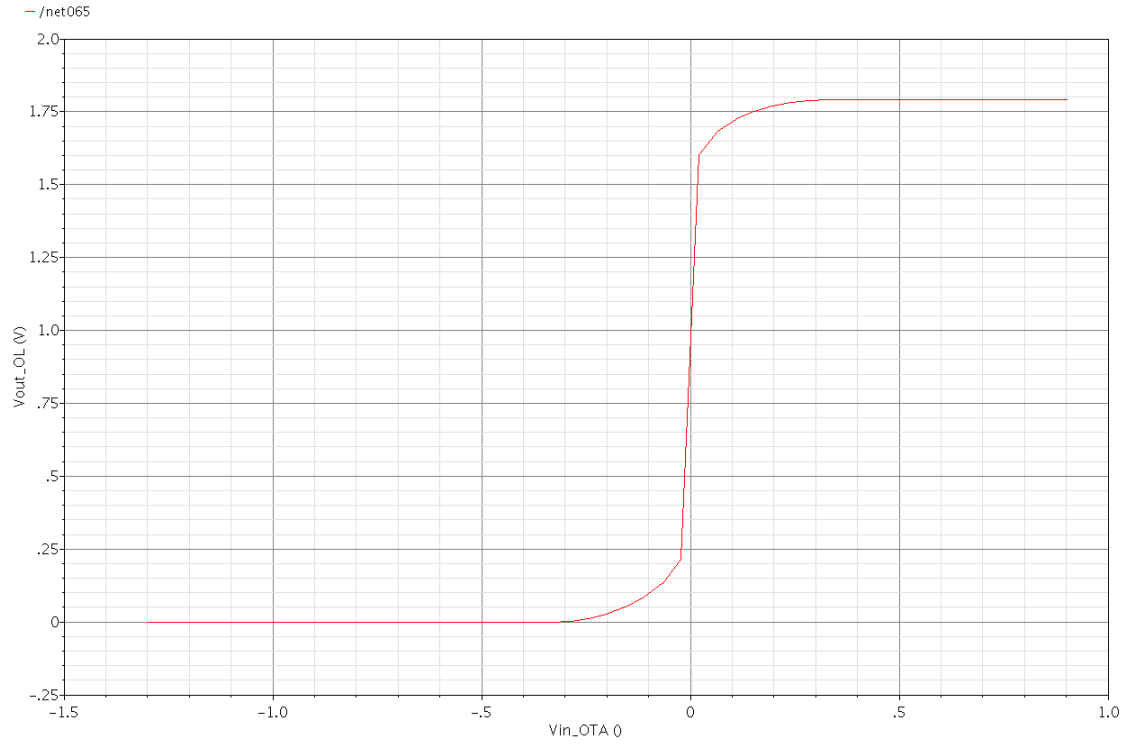


Figure 3: Voltage Transfer Characteristic for the Folded Cascode OTA in Stand Alone

## 4 Bullet Point 4

I applied a small-signal differential input as well as some DC feedback circuitry in order to simulate the open loop gain. Because the open loop gain does not consider small signal feedback, I wanted to build a circuit that would block all AC feedback. However, I wanted to use this feedback to bias  $V_{cm}$ . To do this I implemented an RC lowpass filter with a negligible cutoff voltage as can be seen in Figure 4. I performed an AC simulation of the open loop gain of the circuit (see Figure 5) and was able to attain  $A(s) = 485.40 \frac{V}{V} = 53.39dB$ . Please note that since transistor M44 does not directly affect the biasing, I was able to reduce its size to  $16\mu A$  and optimize my gain.

From the phase plot of my optimized open loop circuit (Figure ??), I estimate that there are poles at  $227kHz$  and  $471MHz$  and a zero at  $945MHz$ . I estimate the gain-bandwidth product (taken at -3dB from the maximum gain) to be  $72.2MHz$ .

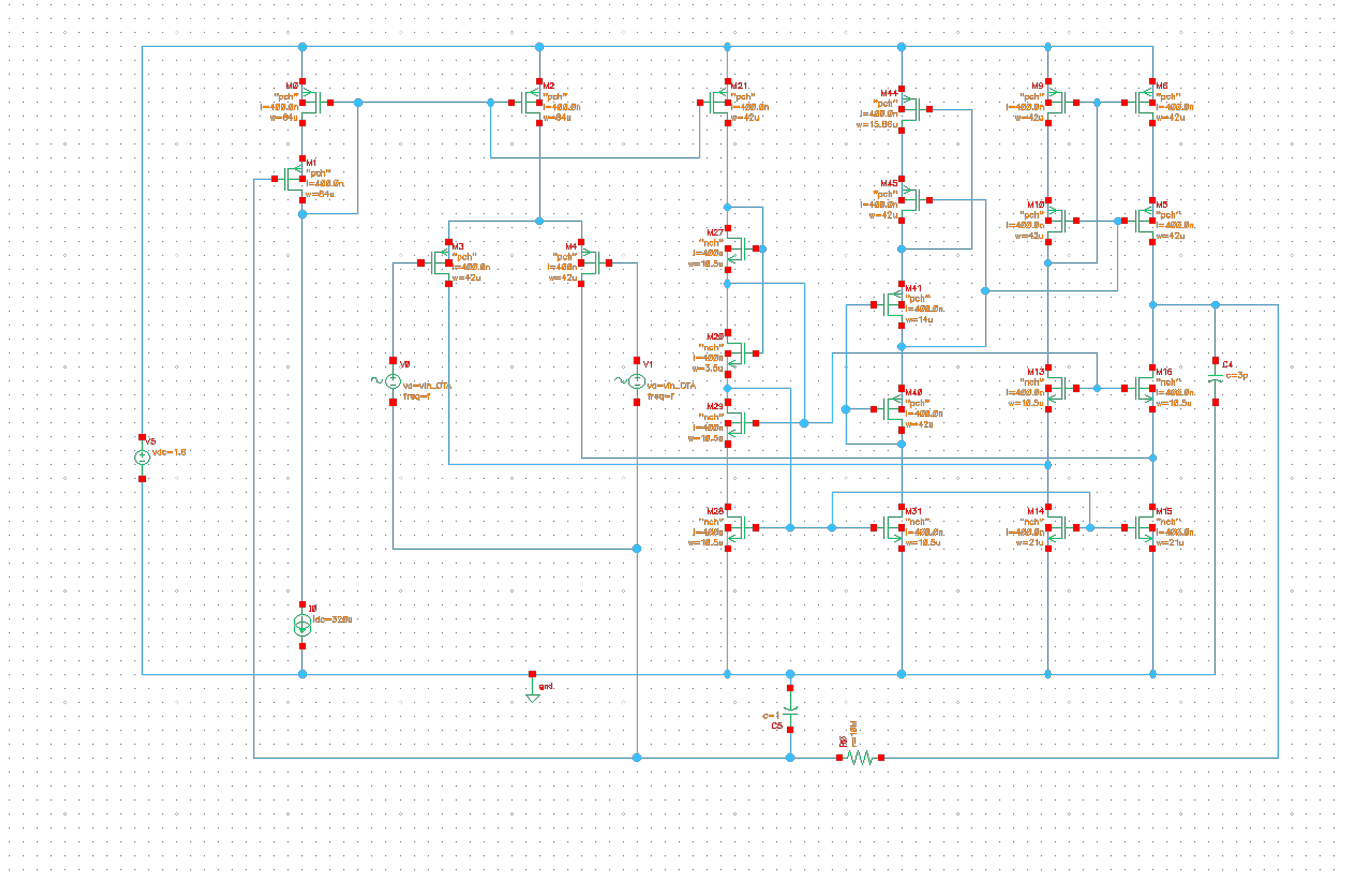


Figure 4: Schematic Diagram for the Folded Cascode OTA for Open Loop Gain Simulation

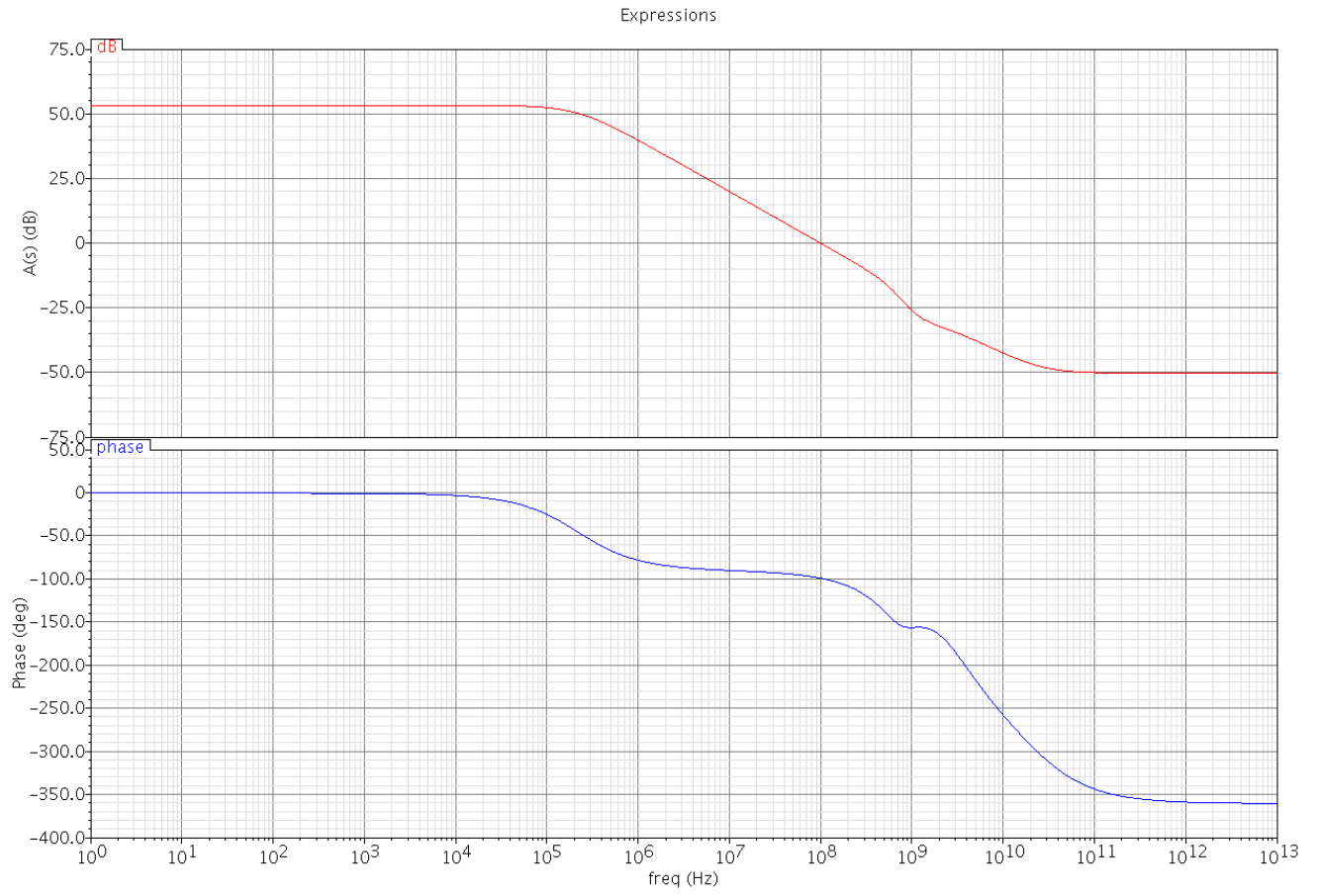


Figure 5: Bode Plot of the Open Loop Gain of the OTA

## **5    Bullet Point 5**

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## **6    Bullet Point 6**