

# E6312: Problem Set 4

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## 1 Bullet Point 1

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## 2 Bullet Point 2

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To build the folded cascade OTA, I began by sizing transistors M0, M1, and M2 (see figure 1 for instance names). Because I want  $160\mu A$  through transistor M9 and that transistor is sized with  $W = 42\mu m$  and I want  $320\mu A$  through transistor M2, I sized M2 at  $84\mu A$ . For the sake of convenience, I decided to use a  $320\mu A$  current source so I sized transistors M0 and M1 at  $84\mu A$  as well. In addition, because I will eventually put this circuit into feedback and I would like my output to be close to mid-rail, I set  $V_{cm} = 800mV$  which is close to the ceiling of input voltage. This is an acceptable value because the small signal input will never be above 1V.

To bias  $V_{b1}$ ,  $V_{b2}$ , and  $V_{b3}$  I utilized two branches of self-biasing current mirrors (see Figure 1). The first branch, which consists of one PMOS and four NMOS transistors, serves a number of purposes. The PFET (M21) mirrors current from M0 and cuts it in half (sized  $42\mu A$ ). The four NMOS receive the  $160\mu A$  of current and are sized as follows. M28 will have half the current of M14 and its gate voltage will bias  $V_{b1}$  so it must be half the width of M14,  $10.5\mu m$ . M29 will have the same current as M13 and its gate voltage will bias  $V_{b2}$  so it must be the same width as M13,  $10.5\mu A$ . M27 will also take the same width as M29 and M28. M20 will take one third of that width. Using a very similar methodology, I built the second self-biasing current mirror branch but this time mirroring the current with an NMOS and receiving the current with four PMOS transistors. M31 mirrors the current of  $160\mu A$  so it is sized the same as M28. M44, M45, and M40 will all have the same current as M10 and the gate of M45 will bias  $V_{b3}$  so they are all sized the same as M10 at  $42\mu A$ . M4 is sized one third of that. As can be seen in Figure 2, the biasing is successful.

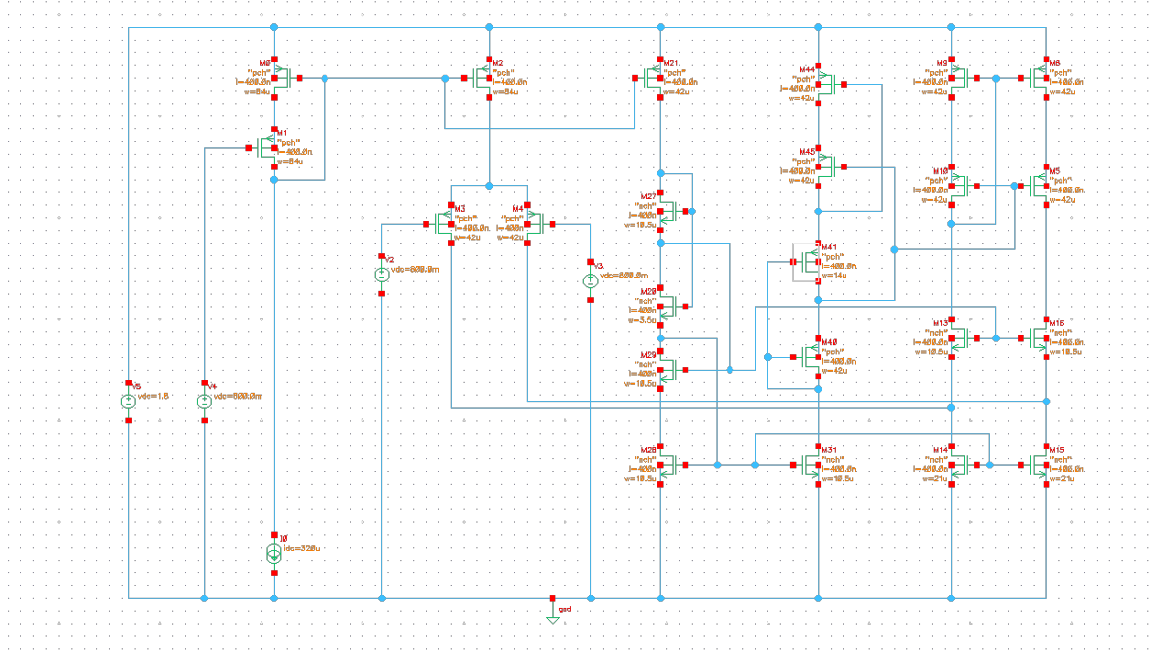


Figure 1: Schematic Diagram for the Folded Cascode OTA with Associated Biasing Circuitry

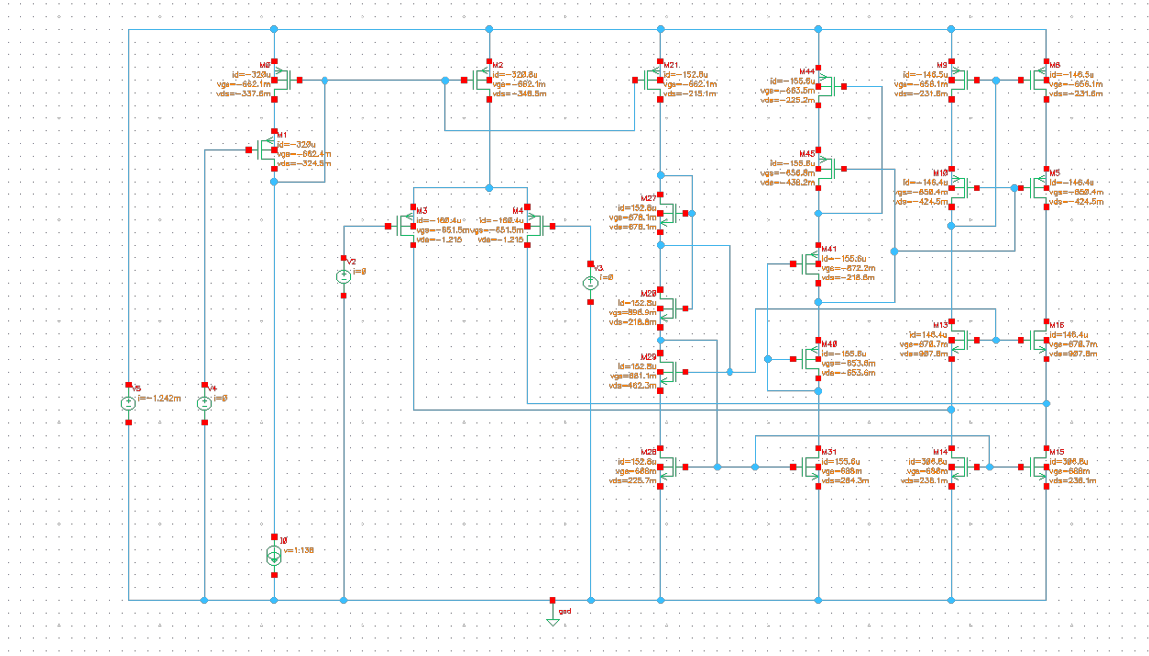


Figure 2: Schematic Diagram for the Folded Cascode OTA with Annotated DC Operating Point Values

### 3 Bullet Point 3

I performed a DC sweep of  $V_{out-OL}$  against  $V_{in-OTA}$  with the OTA in stand alone and the expected transfer function for a differential amplifier is attained (see Figure 3).

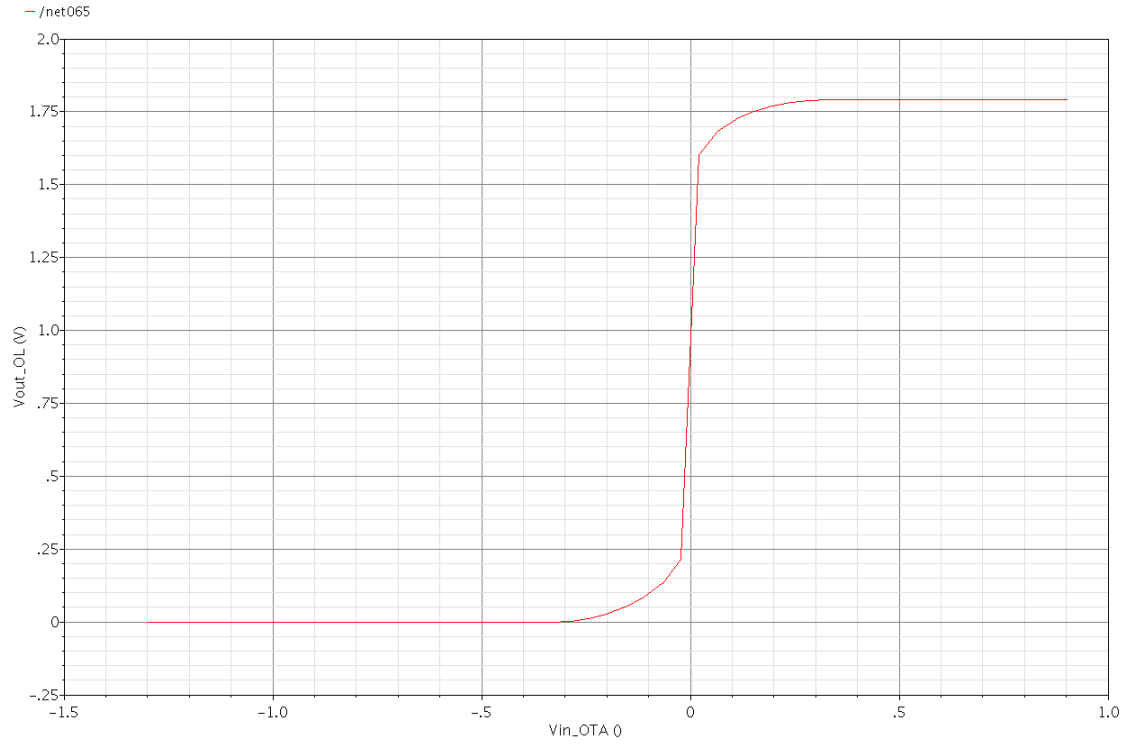


Figure 3: Voltage Transfer Characteristic for the Folded Cascode OTA in Stand Alone

## 4 Bullet Point 4

I applied a small-signal differential input as well as some DC feedback circuitry in order to simulate the open loop gain. Because the open loop gain does not consider small signal feedback, I wanted to build a circuit that would block all AC feedback. However, I wanted to use this feedback to bias  $V_{cm}$ . To do this I implemented an RC lowpass filter with a negligible cutoff voltage as can be seen in Figure 4. I performed an AC simulation of the open loop gain of the circuit (see Figure 5) and was able to attain  $A(s) = 521.19 \frac{V}{V} = 54.34dB$ . Please note that since transistor M44 does not directly affect the biasing, I was able to reduce its size to  $16\mu A$  and optimize my gain.

From the phase plot of my optimized open loop circuit (Figure 5), I estimate that there are poles at  $227kHz$  and  $471MHz$  and a zero at  $945MHz$ . I estimate the gain-bandwidth product (taken at -3dB from the maximum gain) to be  $72.2MHz$ .

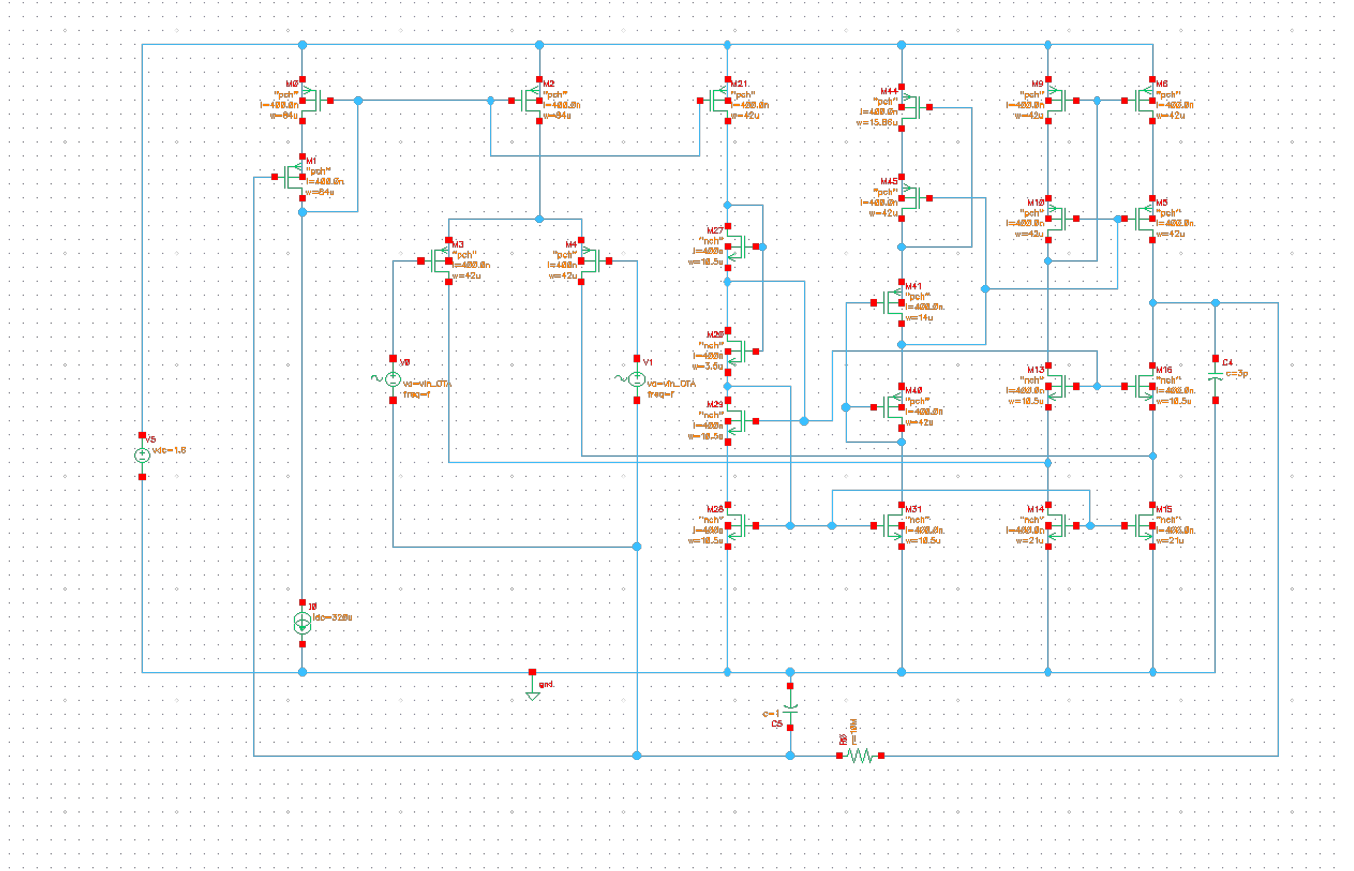


Figure 4: Schematic Diagram for the Folded Cascode OTA for Open Loop Gain Simulation

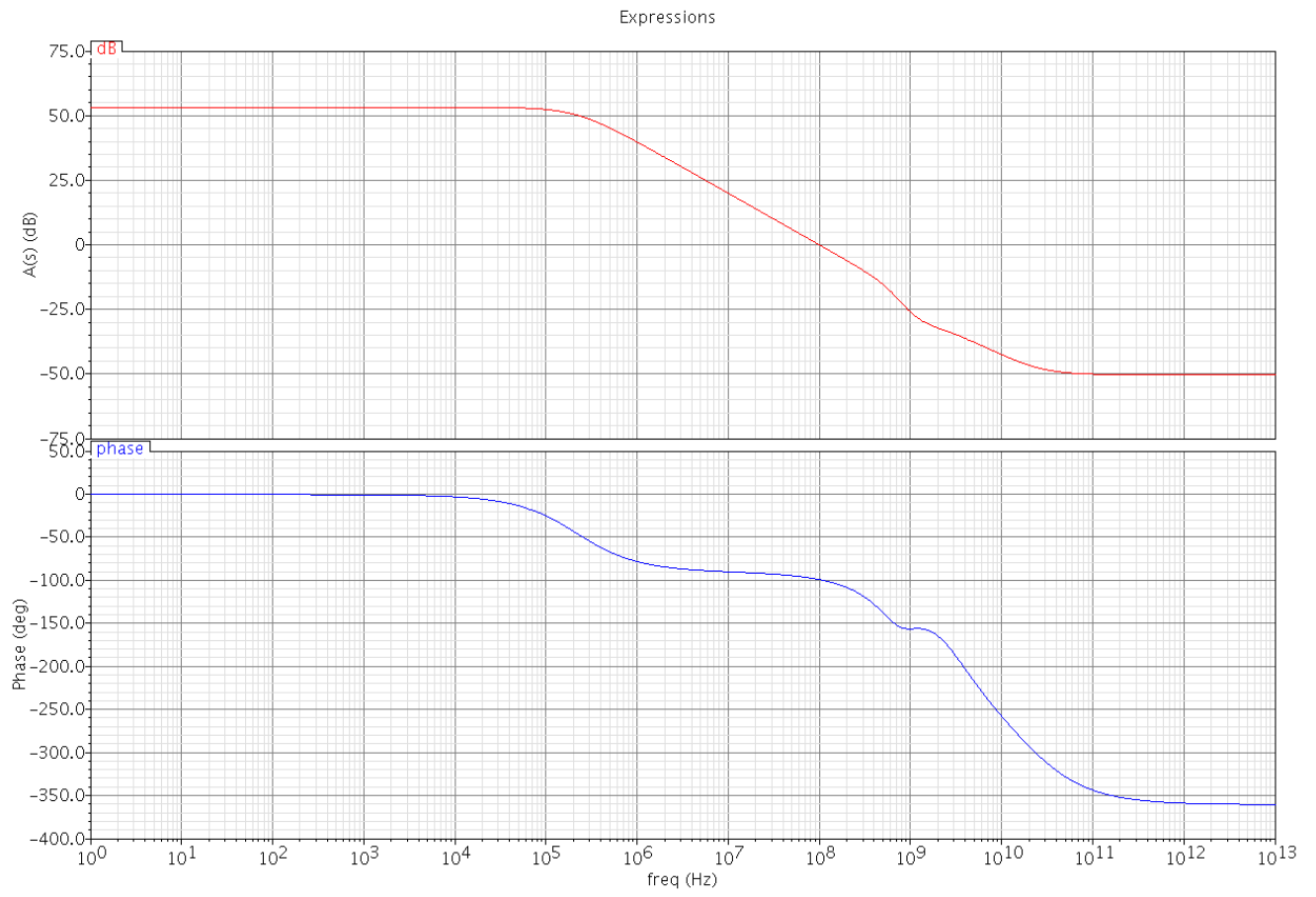


Figure 5: Bode Plot of the Open Loop Gain of the OTA

## 5 Bullet Point 5

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## 6 Bullet Point 6

I placed my OTA in AC feedback as shown in Figure 6 with  $V_{cm} = 0.8V$ . To find the feedback factor,  $\beta$ , from this configuration, I plotted the current through the feedback resistor over the voltage at the output (see Figure 7).

$$\beta = \frac{I_f}{v_{out}} \quad (1)$$

From my simulation, I attained a value of  $\beta = 0.577mA/V$ . This is comparable to the ideal value of

$$\beta_{ideal} = \frac{1}{R_f} = 0.4mA/V \quad (2)$$

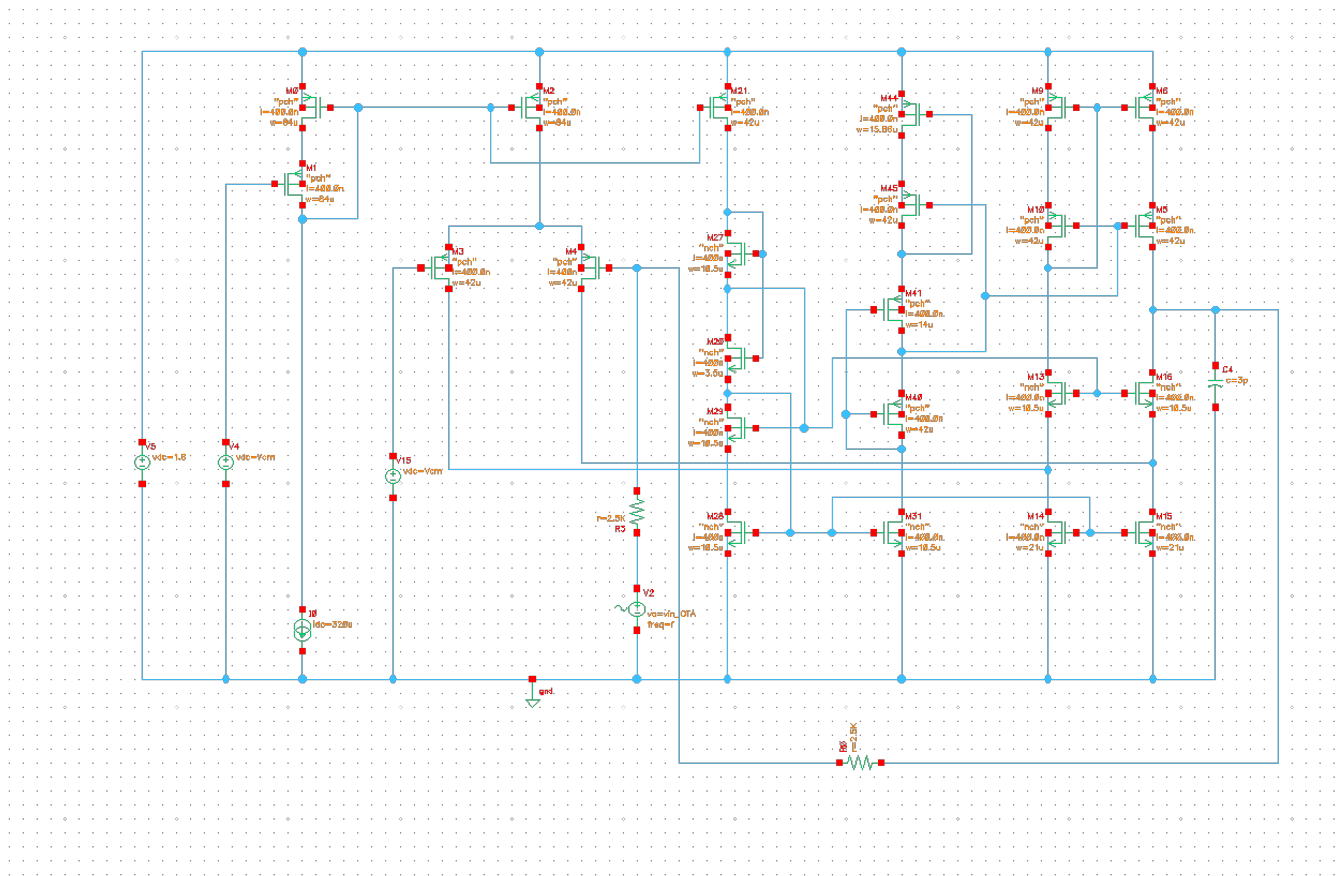


Figure 6: Schematic Diagram for the Folded Cascode OTA for Closed Loop Gain Simulation

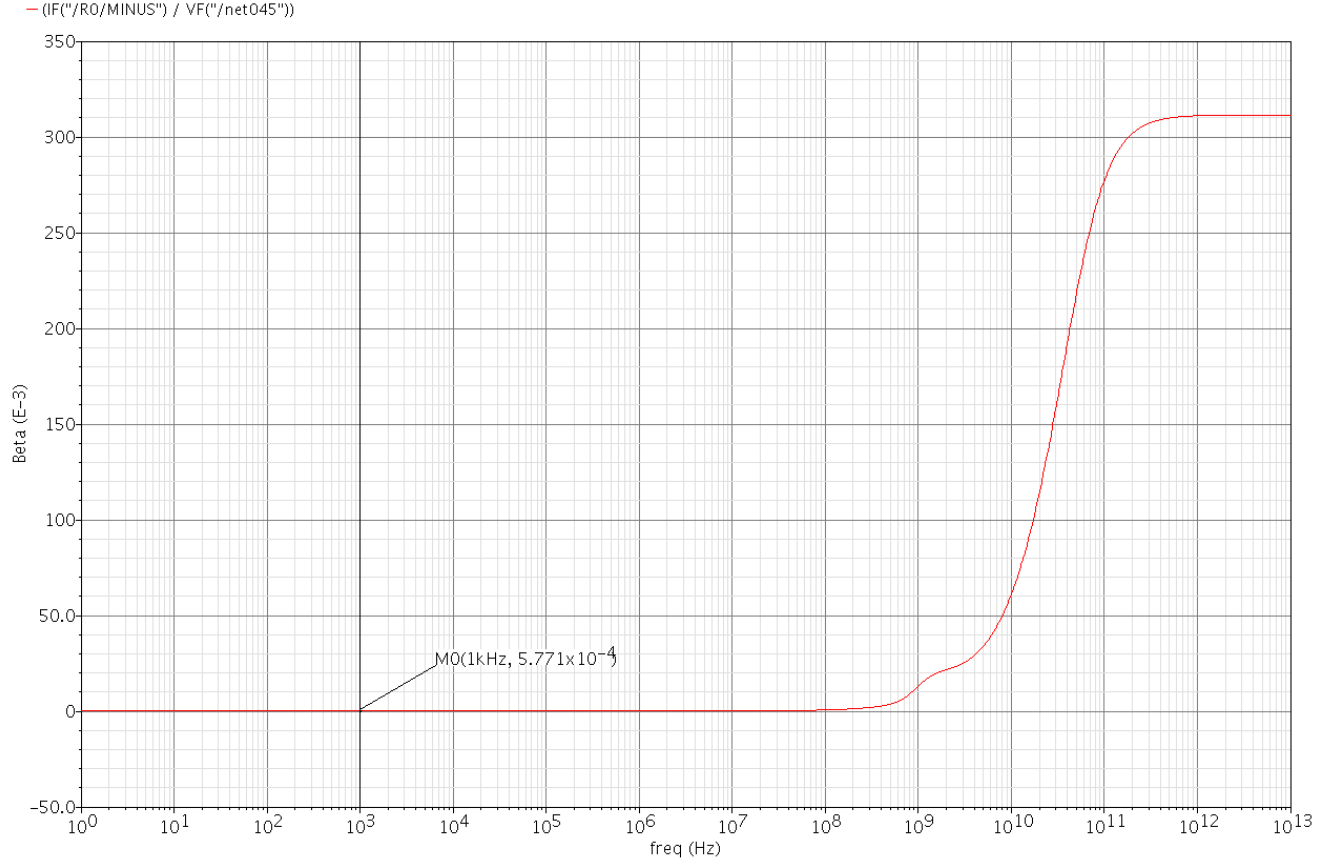


Figure 7: Frequency Response of the Feedback Network

## 7 Bullet Point 7

## 8 Bullet Point 8

## 9 Bullet Point 9

## 10 Bullet Point 10

With an ideal op-amp (infinite gain and bandwidth), a small-signal step at the input should cause an immediate small-signal step at the output. The reason for this is that with infinite bandwidth,  $\tau$  is defined as

$$\tau = \frac{1}{2\pi f_{3dB}} = \infty. \quad (3)$$

To determine the output function, we use the equation

$$v_{OUT} = \mu(t) \{1 - e^{-\frac{t}{\tau}}\} = \mu(t). \quad (4)$$

Therefore, with a small-signal step function at the input, we will observe a small-signal step function at the output.

## 11 Bullet Point 11

To determine the ideal output step for the various small-signal step inputs, I first had to simulate the closed loop gain of my circuit. To do this I constructed the circuit shown in Figure 8 and acquired a gain of  $A_{closed-loop} = 0.53V/V = -5.51dB$  (see Figure 9). I then set out to simulate the step response at various input magnitudes and sample at times  $2\tau$  and  $100Ts$ . My transient step responses can be seen in Figure 10 and my voltage transfer characteristic for  $V_{ideal}$ ,  $V_{out1}$ , and  $V_{out2}$  can be seen in Figure 11.

The absolute and percent errors are shown in the Chart 1.

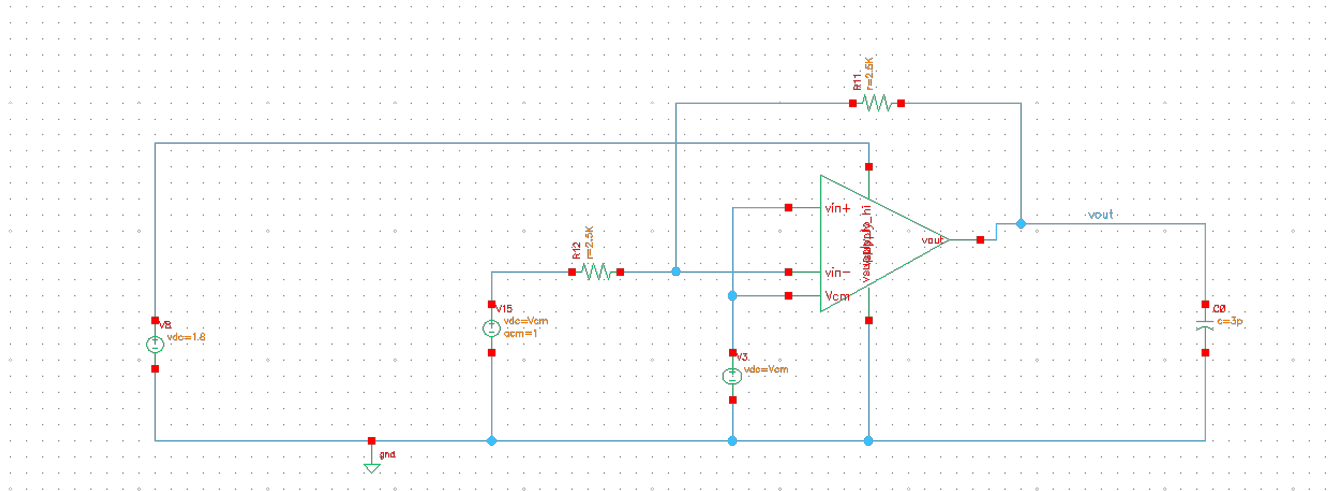


Figure 8: Schematic to Measure Closed Loop Gain

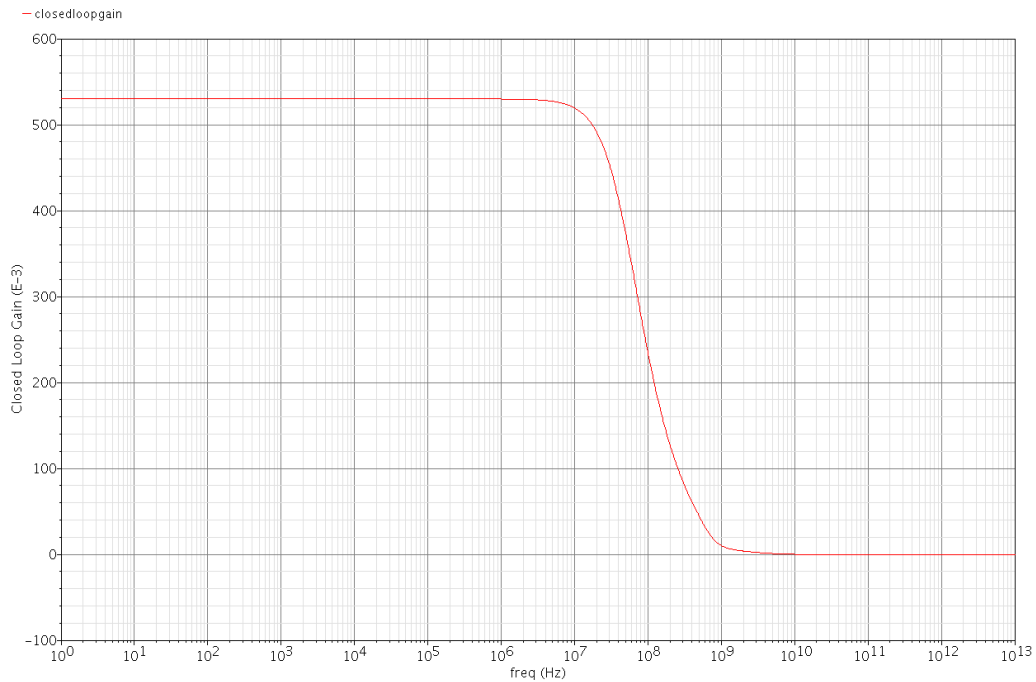


Figure 9: Closed Loop Frequency Response of the OTA in Feedback



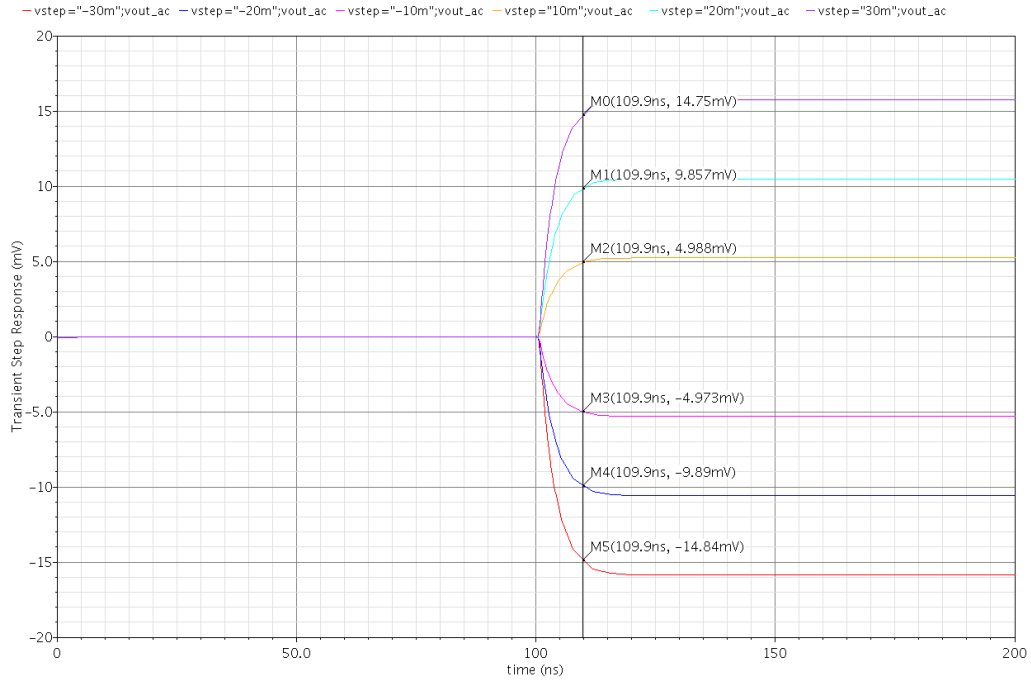


Figure 10: Step Responses for Various Small-Signal Input Step Sizes

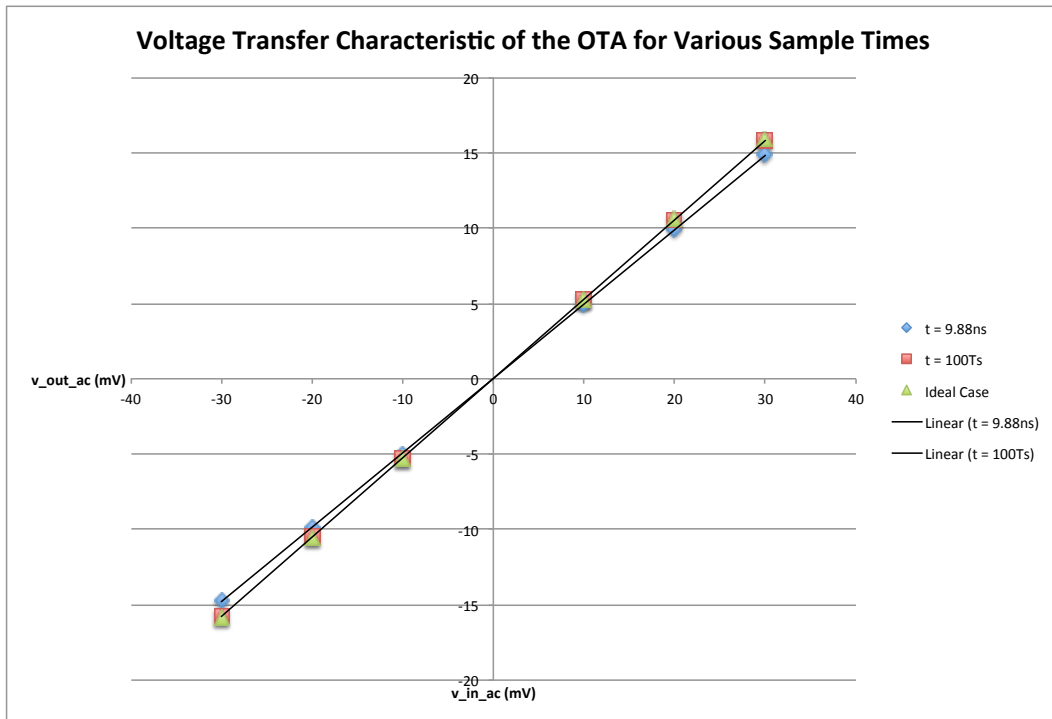


Figure 11: Transfer Function of the OTA Step Response

$v_{in}[\text{mV}]$	$v_{ideal}[\text{mV}]$	Absolute Error at $t = 2\tau[\text{mV}]$	Percent Error at $t = 2\tau[\%]$	Absolute Error at $t = 200Ts[\text{mV}]$	Percent Error at $t = 200Ts[\%]$
10	5.30	0.33	6.17	0.03	0.51
20	10.60	0.71	6.70	0.05	0.47
30	15.90	1.06	6.67	0.07	0.44
-10	5.30	0.31	5.89	0.04	0.79
-20	10.60	0.74	7.00	0.08	0.82
-30	15.90	1.15	7.23	0.14	0.86

Table 1: Error Values for Small Signal Step Response

## 12 Bullet Point 12

## 13 Bullet Point 13

I extended my step response plot for input steps of  $\pm 100\text{mV}$ ,  $\pm 200\text{mV}$ , and  $\pm 500\text{mV}$  to show the effects of slewing. As can be seen in Figure 12, slewing is most obvious in the  $500\text{mV}$  response.

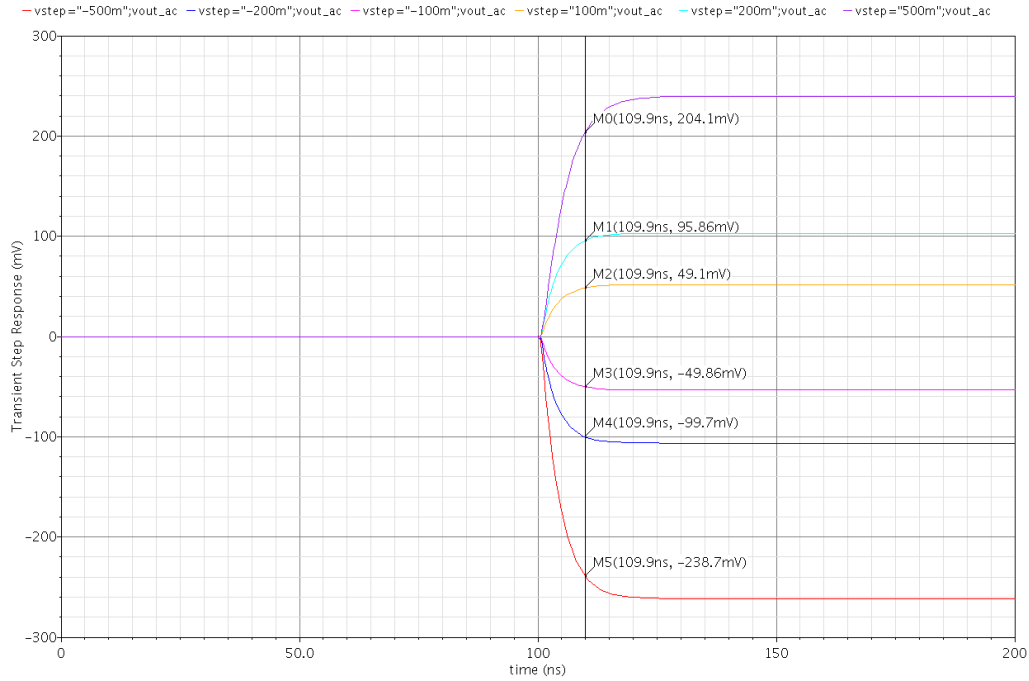


Figure 12: Step Responses for Various Large-Signal Input Step Sizes