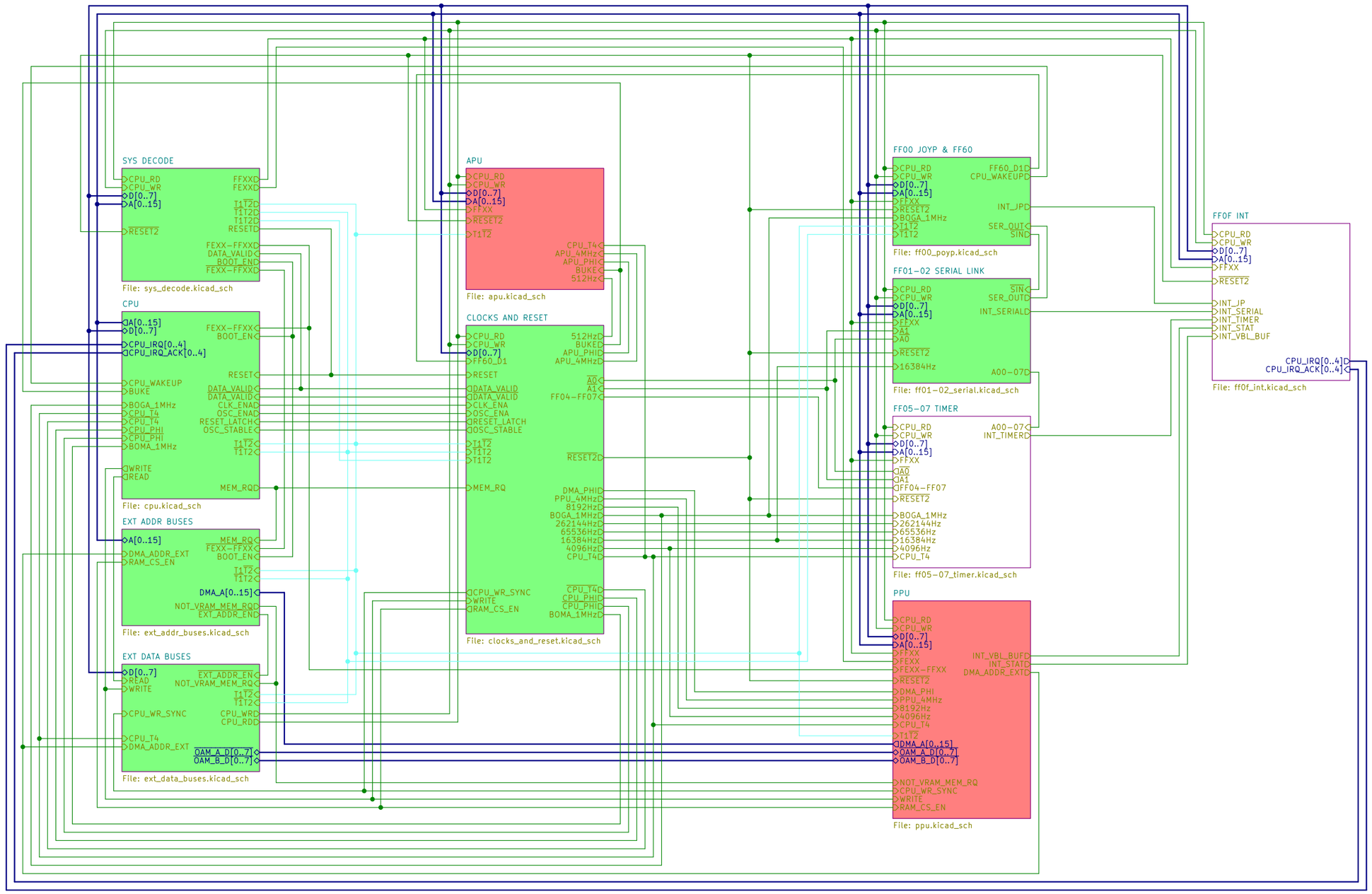

Green boxes contain IO pins
Red boxes contain sub sheets

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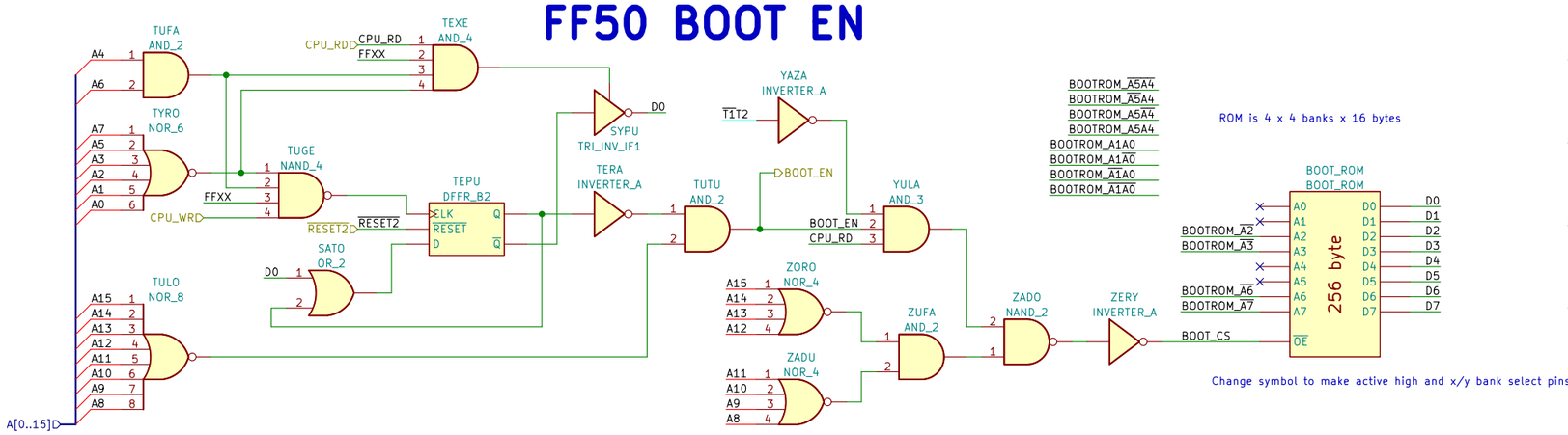
Sheet: /
File: dmg_cpu_b.kicad_sch

Title: DMG CPU B

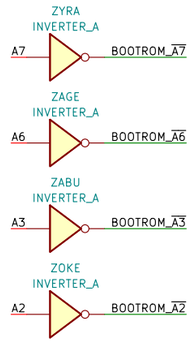
Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 1/45

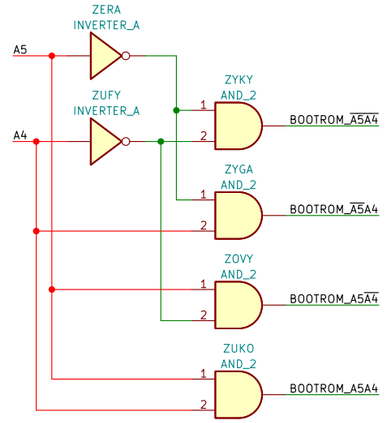
FF50 BOOT EN

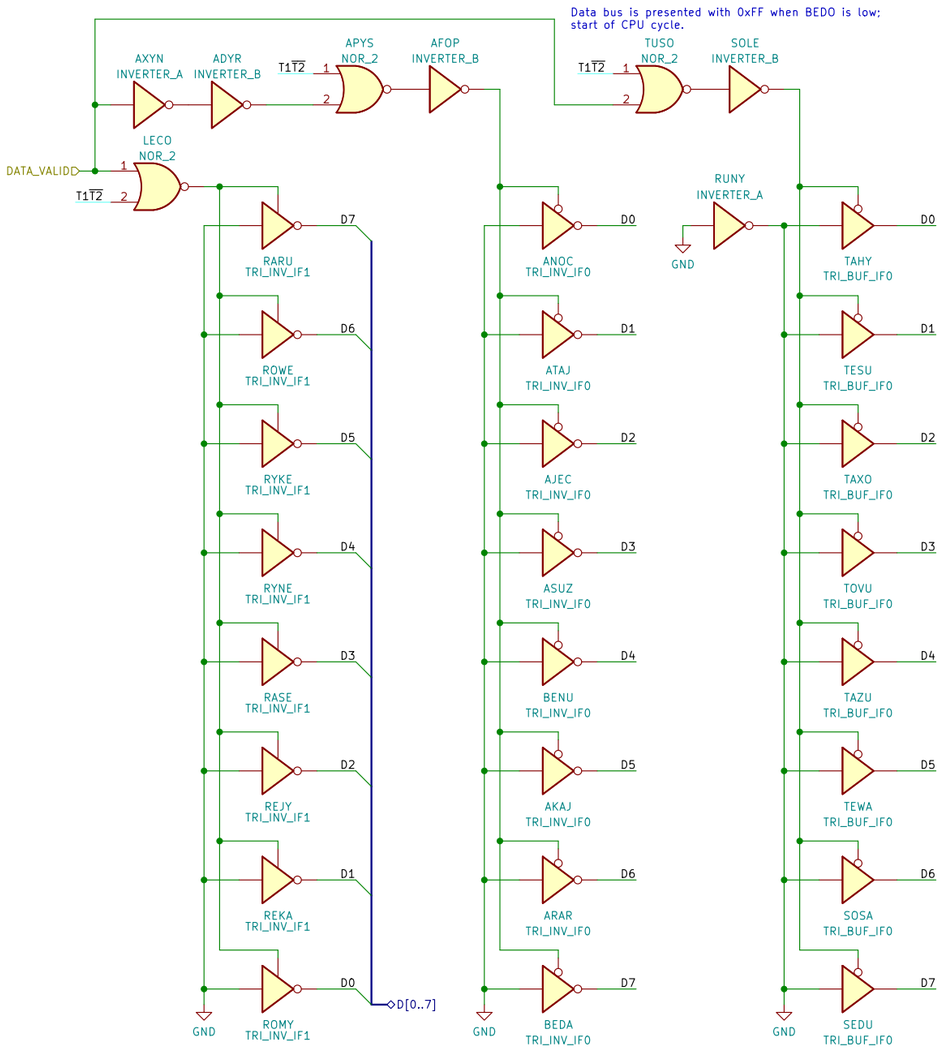


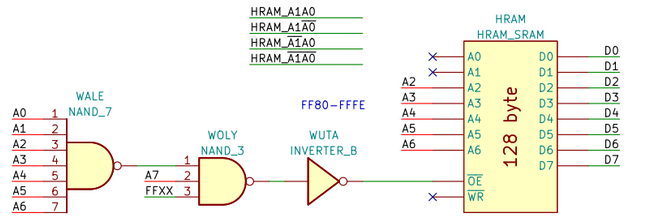
ROM is 4 x 4 banks x 16 bytes

Change symbol to make active high and x/y bank select pins



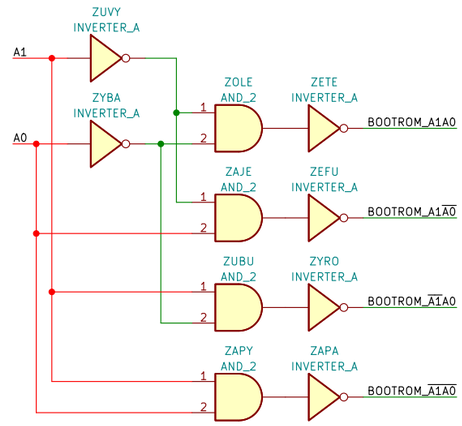


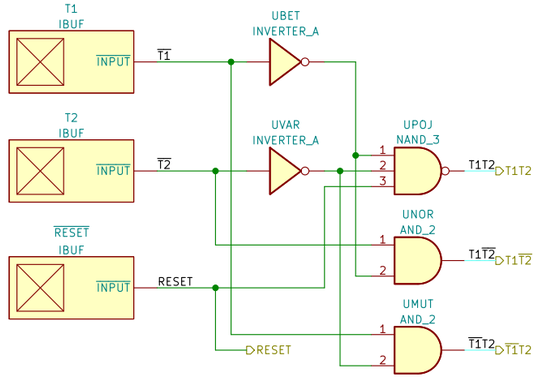




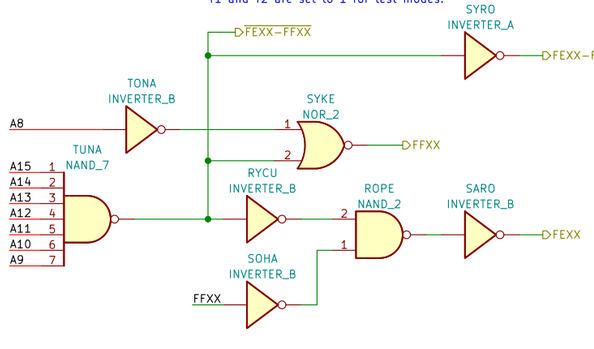
HRAM is 4 banks x 32 bytes

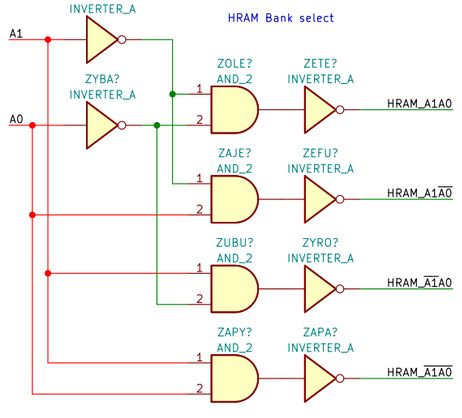
Change symbol to make active high and bank select pins





In normal mode, T1 and T2 pins are gounded on PCB, so T1T2 and T1T2 are always low.
T1T2 only goes low T1=T2=1 and RESET=0.
T1 and T2 are set to 1 for test modes.





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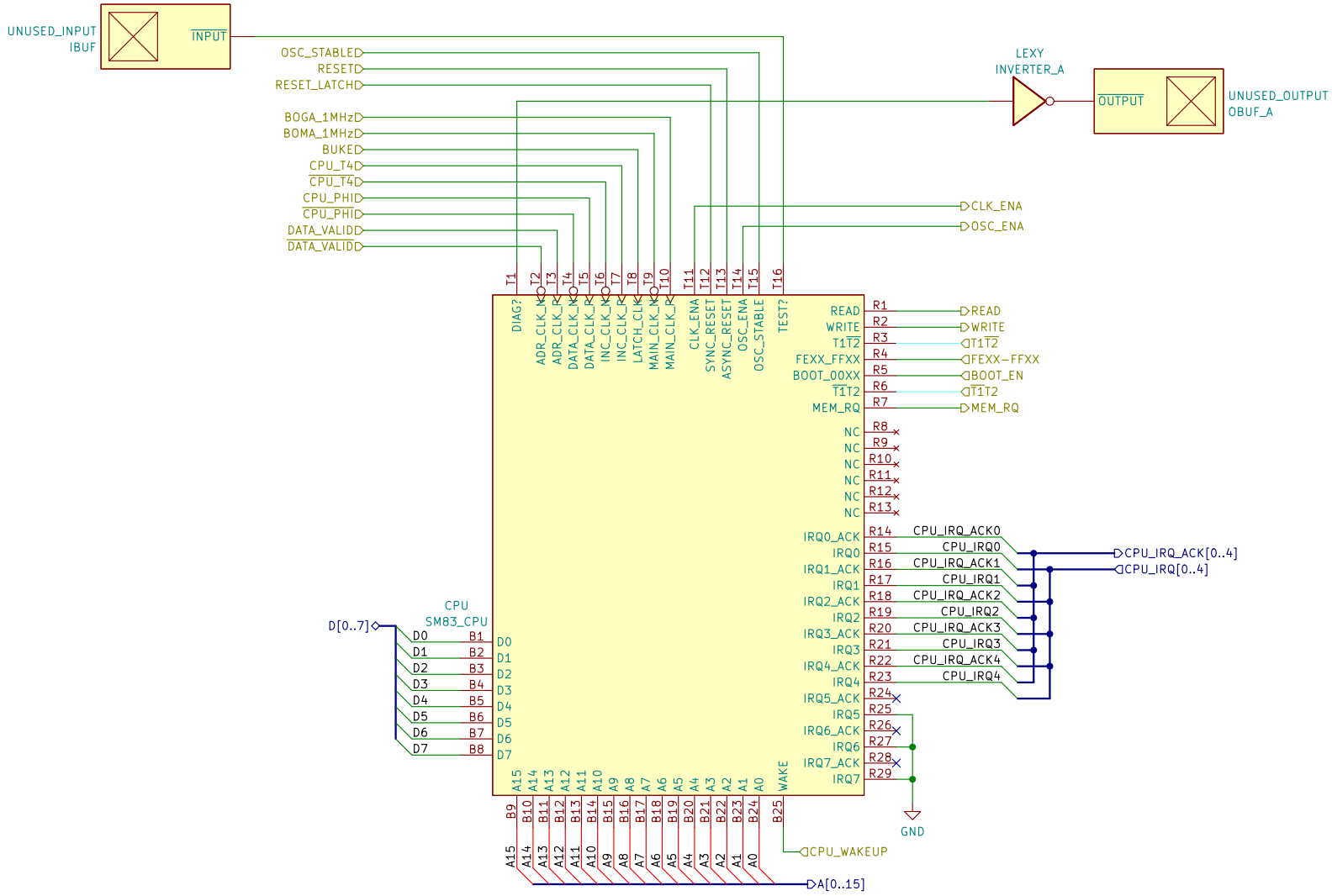
Sheet: /SYS DECODE/
File: sys_decode.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 2/45



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Sheet: /CPU/
File: cpu.kicad_sch

Title: DMG CPU B

Size: A4	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311~116~ubuntu22.04.1		Id: 3/45

TYNU = '1' when A >= 0xA000 else '0'.
TOZA = '1' when A >= 0xA000 and < 0xFE00; RAM space
RAM_CS can only go low in RAM space when driven by CPU

TEXO = '1' during mem req access when A < 0x8000 or A >= 0xA000 else '0'.
It excludes the VRAM address range.
A0–14 are latched and presented to external pins when driven by CPU

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Sheet: /EXT ADDR BUSES/
File: ext_addr_buses.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022–07–08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6–3a73a75311–116–ubuntu22.04.1		Id: 4/45

T1T2 test mode makes RD and WR inputs to bypass the CPU

D[0..7]

OAM_A_D[0..7]

OAM_B_D[0..7]

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Sheet: /EXT DATA BUSES/

File: ext_data_buses.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 5/45

FF04 DIV

CLK_ENA
BAPY NOR_3
BERU INVERTER_B
BUFA INVERTER_D
BYLY INVERTER_E
BOLO INVERTER_D
BYDA INVERTER_E
CPU_T4
CPU_T4
BEJA NAND_4
BANE INVERTER_A
BELO INVERTER_A
BAZE INVERTER_A
BUTO NAND_3
BELE INVERTER_A
BYJU OR_2
BALY INVERTER_A
BOGA INVERTER_E
BOMA INVERTER_E
BOMA_1MHz
BOGA_1MHz
BELU NOR_2
BYRY INVERTER_B
BUDE INVERTER_D
BEVA INVERTER_E
BEKO INVERTER_D
BAVY INVERTER_E
CPU_PHI
CPU_PHI
OUTPUT
PHI OBUF_A
DOVA INVERTER_D
APU_PHI
UVYT INVERTER_B
DMA_PHI
ATEZ INVERTER_A
ABOL INVERTER_A
BUTY INVERTER_A
CLK_ENA
BUVU AND_2
BYXO INVERTER_A
BEDO INVERTER_E
BOWA INVERTER_E
DATA_VALID
DATA_VALID
CLK_ENA
TUBO NOR_LATCH
UPYF OR_2
RESET
UNUT AND_2
T1T2
T1T2
TABA OR_3
ALYP INVERTER_A
AFAR NOR_2
OSC_STABLE
ASOL NOR_LATCH
RESET
RESET
16Hz
BOGA_1MHz
T1T2
AFER DFFR_B
RESET_LATCH
AVOR OR_2
ALUR INVERTER_B
RESET2
UCOB INVERTER_A
OSC_ENA
OSC_ENA
UFOL NOR_3
RESET
RESET_DIV
TAPE AND_4
FF04-FF07
CPU_WR
A1
A0
FF04-FF07
Write to FF04 resets counter
UPOF DFFR_B2
UKET DFFR_B2
TEKA DFFR_B2
SUBU DFFR_B2
SOLA DFFR_B2
TERU DFFR_B2
TOFE DFFR_B2
TUGO DFFR_B2
TULU DFFR_B2
UGOT DFFR_B2
TAGY AND_4
FF04-FF07
CPU_RD
A1
A0
Read to FF04 return counter value
UDOR INVERTER_A
RYSO INVERTER_A
RAVE INVERTER_A
UMER INVERTER_A
SAPY INVERTER_A
UTOK INVERTER_A
UREK INVERTER_A
UMEK INVERTER_A
512Hz
4096Hz
8192Hz
TATU TRI_INV_IF1
SAWA TRI_INV_IF1
SEPU TRI_INV_IF1
UPUG TRI_INV_IF1
TUSE TRI_INV_IF1
TEMU TRI_INV_IF1
TAKU TRI_INV_IF1
TAWU TRI_INV_IF1
D7
D6
D5
D4
D3
D2
D1
D0
D[0..7]
TAMA DFFR_B2
UNYK DFFR_B2
TERO DFFR_B2
UNER DFFR_B2
UFOR DFFR_B2
UKUP DFFR_B2
UVYN INVERTER_A
UVYR INVERTER_A
UBOT INVERTER_A
16384Hz
65536Hz
262144Hz
BOGA_1MHz
FF60_D1
BOGA_1MHz
ULUR MUX
ATAL_INV INVERTER_A
ADYK DR_LATCH
ADAR INVERTER_A
AFAS NOR_2
AREV NAND_2
APOV INVERTER_C
CPU_WR_SYNC
WRITED
AFUR DR_LATCH
ATYP INVERTER_A
AJAX INVERTER_A
AGUT OA
AWOD NOR_2
ABUZ INVERTER_C
RAM_CS_EN
MEM_RQD
T1T2
BUGO INVERTER_A
ALEF DR_LATCH
AFEP INVERTER_A
BATE NOR_3
BASU INVERTER_A
BUKE INVERTER_E
BUKE
CLK_ENA
APUK DR_LATCH
AROV INVERTER_A
T1T2
T1T2
ATAL_4MHz
ATAG INVERTER_A
AMUK INVERTER_E
APU_4MHz
CK1_CK2 OSC
ANOS NAND_2
ARYS INVERTER_A
AVET NAND_2
ATAL INVERTER_B
AZOF INVERTER_E
ZAXY INVERTER_B
ZEME INVERTER_C
PPU_4MHz
CLK
ENA
OSC_ENA

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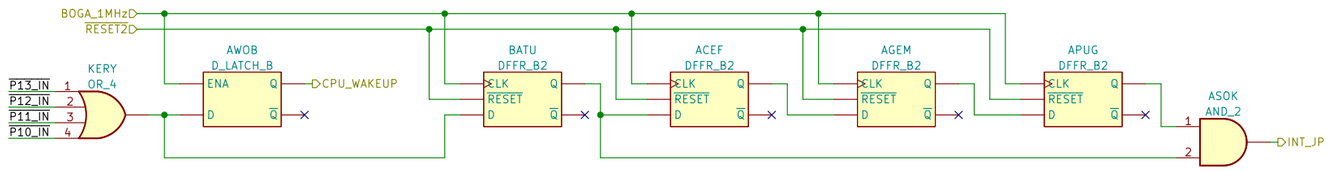
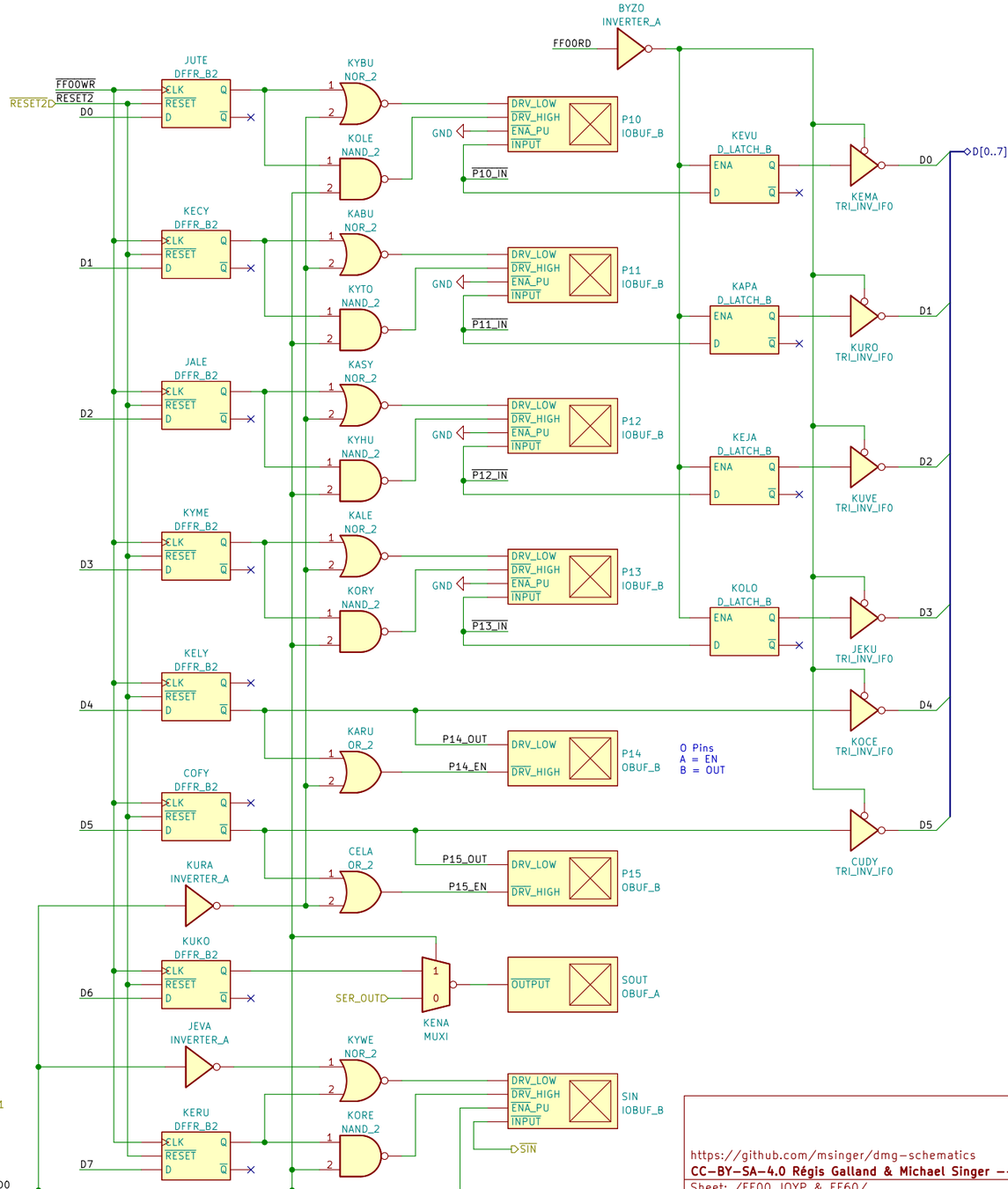
Sheet: /CLOCKS AND RESET/
File: clocks_and_reset.kicad_sch

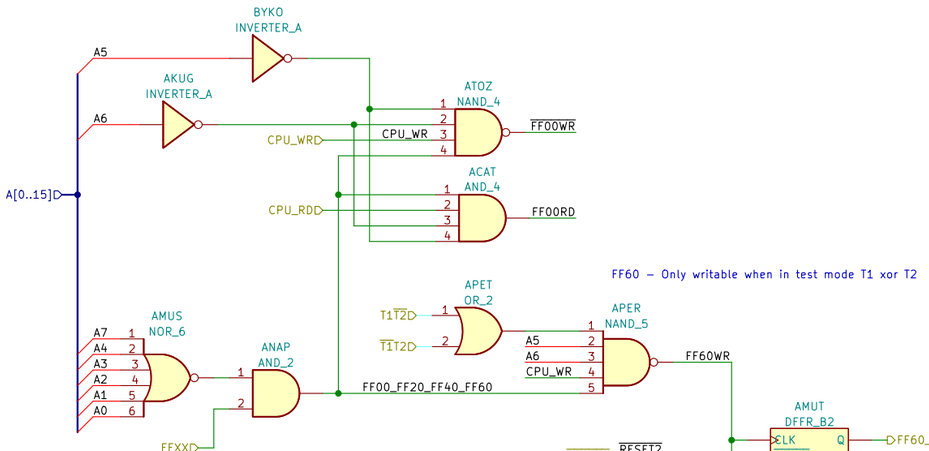
Title: DMG CPU B

Size: A3	Date: 2022-07-08	Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 6/45

FF00 JP







FF60

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Sheet: /FF00 JOYP & FF60/
File: ff00_poyp.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A.	kicad 6.0.6-3a73a75311~116-ubuntu22.04.1	Id: 7/45

FF01 SB

A[0..15]
SARE NOR_5
A7 A6 A5 A4 A3
A00-07
SEFY INVERTER_A
A2
SANO AND_3
FFXXD
A1
A00-03
CPU_WR
CPU_WRD
A1
A0
URYS NAND_4
SERIAL_TICK
EPYT INVERTER_B
DEHO INVERTER_A
DAWE INVERTER_B
CPU_RDD
A00-03
CPU_RD
A1
A0
UFEG AND_4
CAGE INVERTER_A
SIND
DAKU INVERTER_A
D0
CUFU NAND_2
COHY OA
RESET2
CUBA DFFSR
CLK SET RESET D Q
CUGY TRI_INV_IF1
D1
DOCU NAND_2
DUMO OA
DEGU DFFSR
DUDE TRI_INV_IF1
D2
DELA NAND_2
DYBO OA
DYRA DFFSR
DETU TRI_INV_IF1
D3
DYGE NAND_2
DAJU OA
DOJO DFFSR
DASO TRI_INV_IF1
D4
DOLA NAND_2
DYLY OA
DOVU DFFSR
DAME TRI_INV_IF1
D5
ELOK NAND_2
EHUJ OA
EJAB DFFSR
EVOK TRI_INV_IF1
D6
EDEL NAND_2
EFAK OA
EROD DFFSR
EFAB TRI_INV_IF1
D7
EFEF NAND_2
EGUV OA
EDER DFFSR
ETAK TRI_INV_IF1
D[0..7]
ELYS DFFR_B2
SERIAL_TICK
RESET2
SER_OUT

FF02 SC

UCOM AND_4
A00-03
CPU_RD
A1
A0
UWAM NAND_4
CPU_WR
ETAF DFFR_B2
CLK RESET D Q
D7
SCK_EN
ELUV TRI_INV_IF1
CULY DFFR_B2
RESET2D
RESET2
D0
SCK_DIR
CORE TRI_INV_IF1
CARO AND_2
INT_SERIAL
COBA INVERTER_A
CABY AND_2
RESET2
CALY DFFR_B2
CYDE DFFR_B2
CYLO DFFR_B2
CAFA DFFR_B2
EDYL INVERTER_A
SERIAL_TICK
JAGO INVERTER_A
KUJO NOR_2
KEXU NAND_2
DAWA OR_2
16384Hz
COTY DFFR_B2
CAVE MUXI
DRV_LOW
DRV_HIGH
ENA_PU
INPUT
IOBUF_C
SCK

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Sheet: /FF01-02 SERIAL LINK/
File: ff01-02_serial.kicad_sch

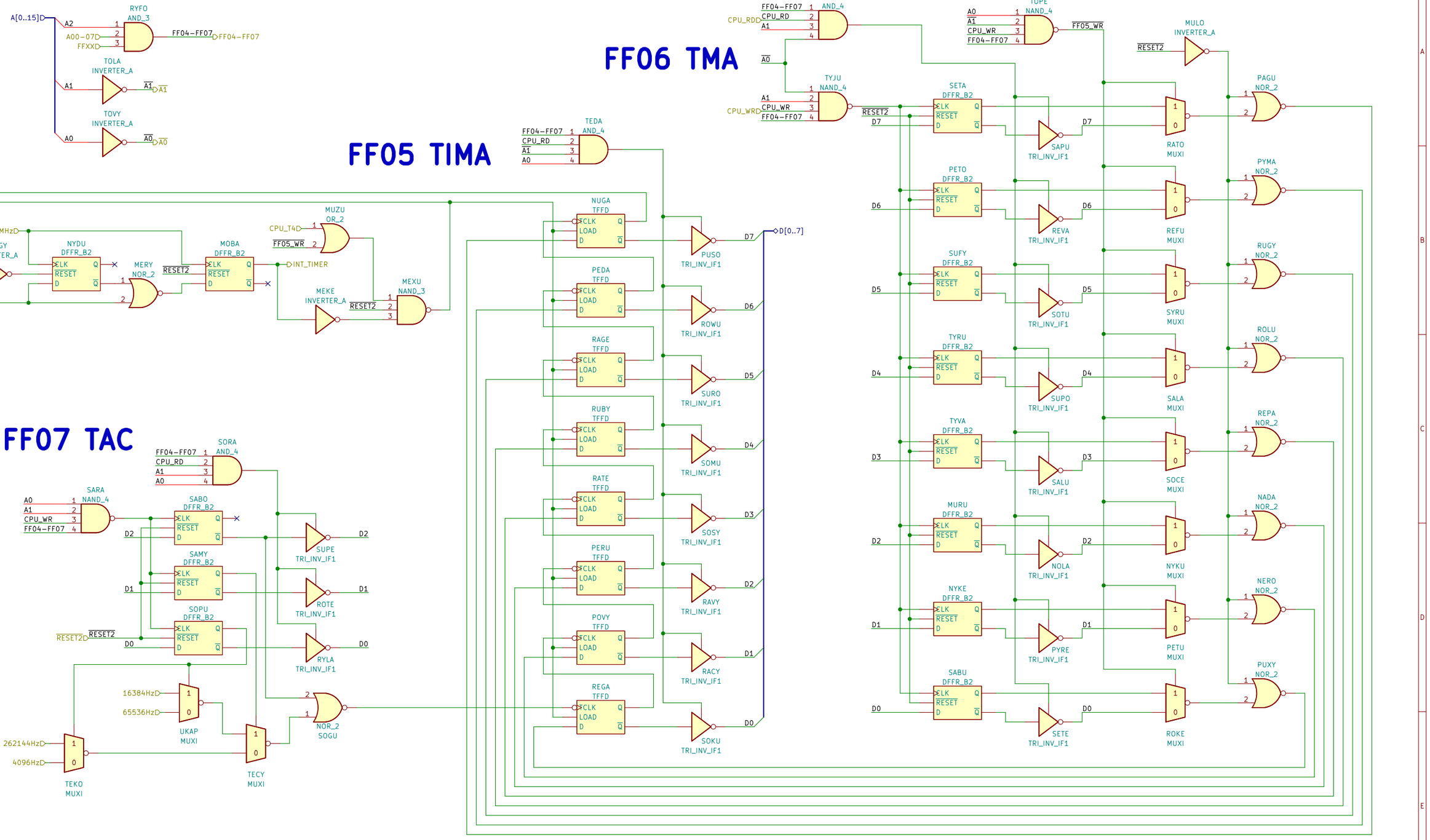
Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 8/45

FF06 TMA

FF05 TIMA

FF07 TAC



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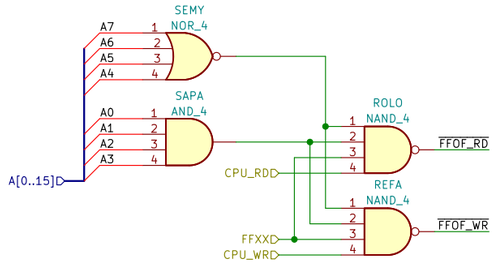
Sheet: /FF05-07 TIMER/
File: ff05-07_timer.kicad_sch

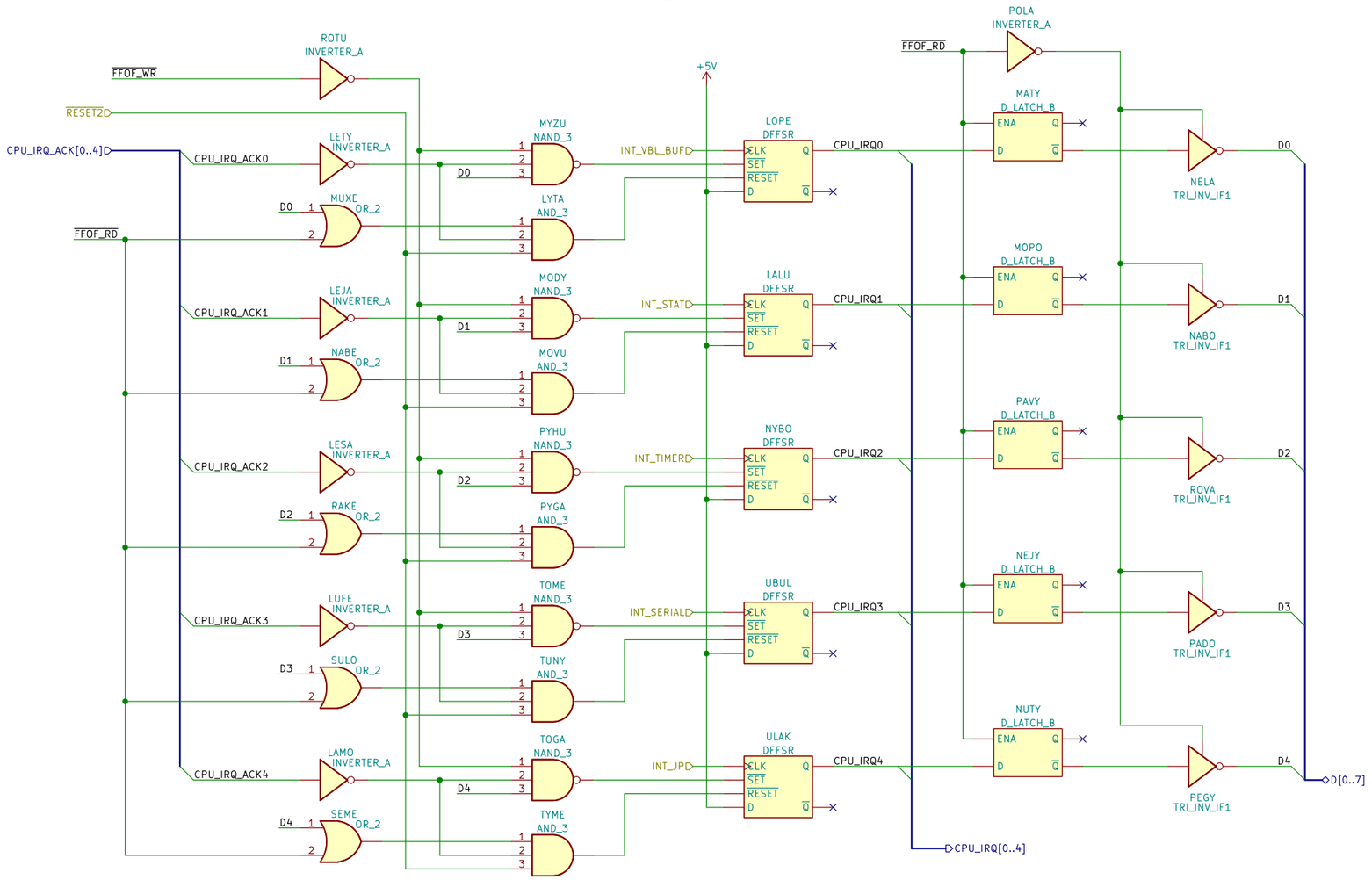
Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 9/45



FFOF IF

Data latching is halted during read as int flags get reset



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Sheet: /FF0F INT/
File: ff0f_int.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 10/45

APU DECODE

CPU_T4
CPU_RD
CPU_WR
FFXX
A[0..15]

CH4_AMP_EN
CH3_AMP_EN
CH2_AMP_EN
CH1_AMP_EN
FF26
FF25
FF24
APU_WR
APU_RD
NRx4_D6_WR
FF14
FF13
FF12
FF11
FF10
FF19
FF18
FF17
FF16
FF23
FF22
FF21
FF20
FF3X
FF1E
FF1D
FF1C
FF1B
FF1A
AMP_EN

File: apu_decode.kicad_sch

D[0..7]

FF24 FF25 CH EN & VOL

APU_RD
APU_WR
D[0..7]
FF24
FF25
FF24-26_RESET

File: ff24_ff25.kicad_sch

FF26 APU CLOCKS & RESETS

APU_RD
APU_WR
D[0..7]
FF26
FF1A_RD
FF24-26_RESET
APU_RESET
APU_RESET
APU_RESET6
APU_RESET2
APU_RESET4
APU_RESET5
NET03
RESET2
512Hz
T1T2
CH1_1MHz
CH2_1MHz
CH3_2MHz
AJER_2MHz
CH4_1MHz
CATE_128Hz
BYFE_128Hz
BUFY_256Hz
HORU_512Hz
CH4_ACTIVE
CH3_ACTIVE
CH2_ACTIVE
CH1_ACTIVE
APU_4MHz
HAMA_512KHz
JESO_512K

File: apu_control.kicad_sch

CH1 REGS

APU_RD
APU_WR
NRx4_D6_WR
D[0..7]
FF10
FF11
FF12
FF13
FF14
APU_RESET
APU_RESET
APU_RESET6
NET03
APU_PHI
CH1_1MHz
FF10_D[0..6]
FF11_D[6..7]
FF11_D[6..7]
FF12_D[0..3]
FF12_D[0..7]
FF14_D6
FF14_D6
CH1_FDIS
CH1_FTICK
CH1_FRST
CH1_FREQ_UPD1
CH1_FREQ_UPD2
CH1_KICKSTART_PULSE
CH1_RESTART
ACC_D[0..10]
SUM[0..10]

File: ch1_regs.kicad_sch

CH1 SWEEP

APU_RESET
SUM[0..10]
ACC_D[0..10]
FF10_D[0..6]
CH1_RESTART
CH1_SUM_OVFL
CH1_LD_SHIFT
CH1_LD_SUM
CH1_SHIFT_CLK

File: ch1_sweep.kicad_sch

CHANNEL 1

APU_WR
D[0..7]
FF11
CH1_SHIFT_CLK
CH1_LD_SUM
CH1_LD_SHIFT
CH1_SUM_OVFL
CH1_RESTART
CH1_KICKSTART_PULSE
CH1_FREQ_UPD2
CH1_FREQ_UPD1
CH1_FRST
APU_RESET
APU_RESET6
CH1_FTICK
CH1_FDIS
FF14_D6
FF14_D6
NET03
FF12_D[0..7]
FF12_D[0..3]
CH1_1MHz
AJER_2MHz
HORU_512Hz
BUFY_256Hz
BYFE_128Hz
CATE_128Hz
FF11_D[6..7]
FF11_D[6..7]
FF10_D[0..6]
CH1_AMP_END
CH1_ACTIVED

File: channel1.kicad_sch

CH2 REGS

APU_RD
APU_WR
NRx4_D6_WR
D[0..7]
FF16
FF17
FF18
FF19
APU_RESET
APU_RESET2
NET03
APU_PHI
CH2_1MHz
FF16_D[6..7]
FF16_D[6..7]
FF17_D[0..3]
FF17_D[0..7]
FF19_D6
FF19_D6
CH2_FDIS
CH2_FTICK
CH2_RESTART
CH2_FRST
CH2_KICKSTART_PULSE

File: ch2_regs.kicad_sch

CHANNEL 2

APU_WR
D[0..7]
FF16
APU_RESET
APU_RESET2
NET03
CH2_1MHz
HORU_512Hz
BUFY_256Hz
BYFE_128Hz
CH2_KICKSTART_PULSE
CH2_FRST
CH2_RESTART
CH2_FTICK
CH2_FDIS
FF19_D6
FF19_D6
FF17_D[0..3]
FF17_D[0..7]
FF16_D[6..7]
FF16_D[6..7]
CH2_AMP_END
CH2_ACTIVED

File: channel2.kicad_sch

CH3 REGS

APU_RD
APU_WR
NRx4_D6_WR
FF1A_RD
D[0..7]
FF1A
FF1B
FF1C
FF1D
FF1E
APU_RESET
NET03
APU_PHI
CH3_2MHz
AJER_2MHz
BUFY_256Hz
CH3_AMP_EN
CH3_ACTIVED
FF1C_D[5..6]
FF1C_D[5..6]
CH3_ACTIVED
CH3_FTICKD
CH3_RESTARTD
CH3_FRSTD

File: ch3_regs.kicad_sch

CH3 WAVE RAM

APU_RD
APU_WR
D[0..7]
FF1C
FF3X
APU_RESET
NET03
BUKE
CH3_2MHz
APU_4MHz
CH3_FRSTD
CH3_RESTARTD
CH3_FTICKD
CH3_ACTIVED
FF1C_D[5..6]
FF1C_D[5..6]
A[0..15]

File: ch3_wave_ram.kicad_sch

CH4 REGS

APU_RD
APU_WR
NRx4_D6_WR
D[0..7]
FF20
FF21
FF22
FF23
APU_RESET
APU_RESET4
APU_RESET5
NET03
APU_PHI
BUFY_256Hz
HAMA_512KHz
CH4_AMP_EN
CH4_ACTIVED
FF21_D[0..3]
FF21_D[0..7]
FF22_D[0..6]
FF22_D[3..7]
CH4_RESTARTD
CH4_FDISD
CH4_ACTIVED
CH4_EG_TESTD
NOISE_COUNTER_CLKD
NOISE_COUNTER_BYPASSD

File: ch4_regs.kicad_sch

CHANNEL 4

NOISE_COUNTER_BYPASS
NOISE_COUNTER_CLK
CH4_EG_TEST
APU_RESET
APU_RESET4
CH4_1MHz
HORU_512Hz
BYFE_128Hz
JESO_512K
CH4_ACTIVE
CH4_FDIS
CH4_RESTART
FF22_D[3..7]
FF22_D[0..6]
FF21_D[0..7]
FF21_D[0..3]

File: channel4.kicad_sch

APU_PHI
APU_4MHz
BUKE

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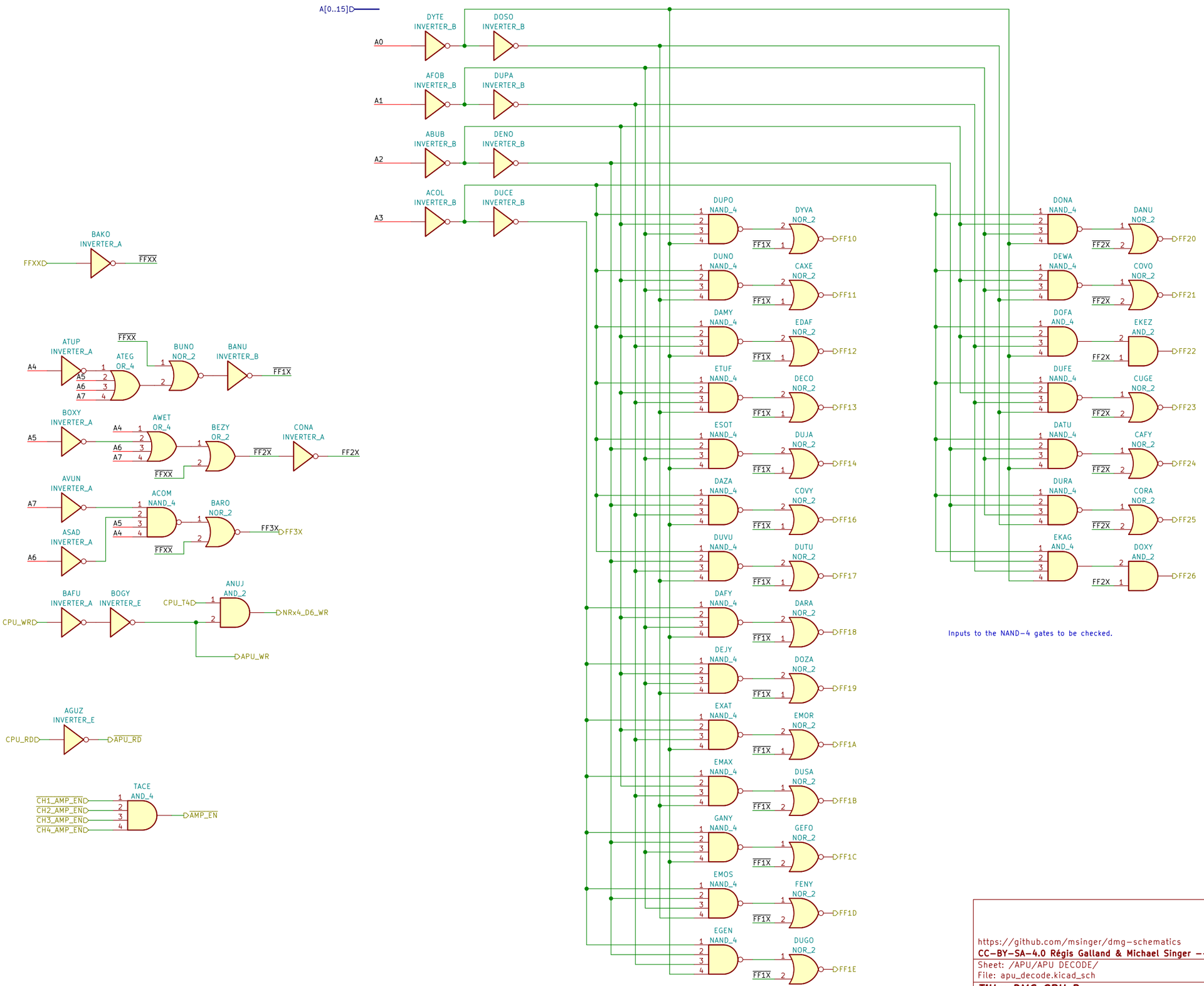
Sheet: /APU/
File: apu.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311~116~ubuntu22.04.1		Id: 11/45



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Sheet: /APU/APU DECODE/

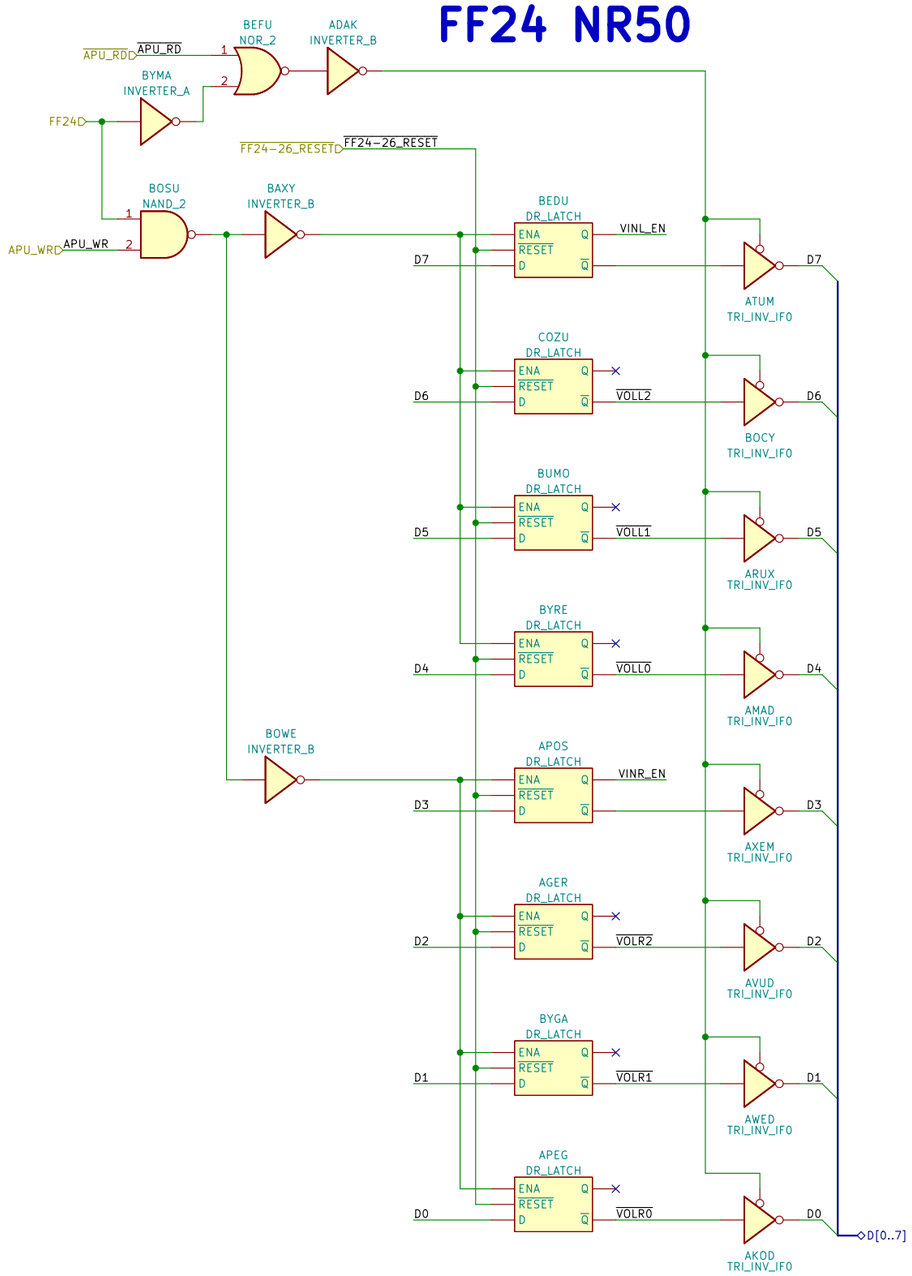
File: apu_decode.kicad_sch

Title: DMG CPU B

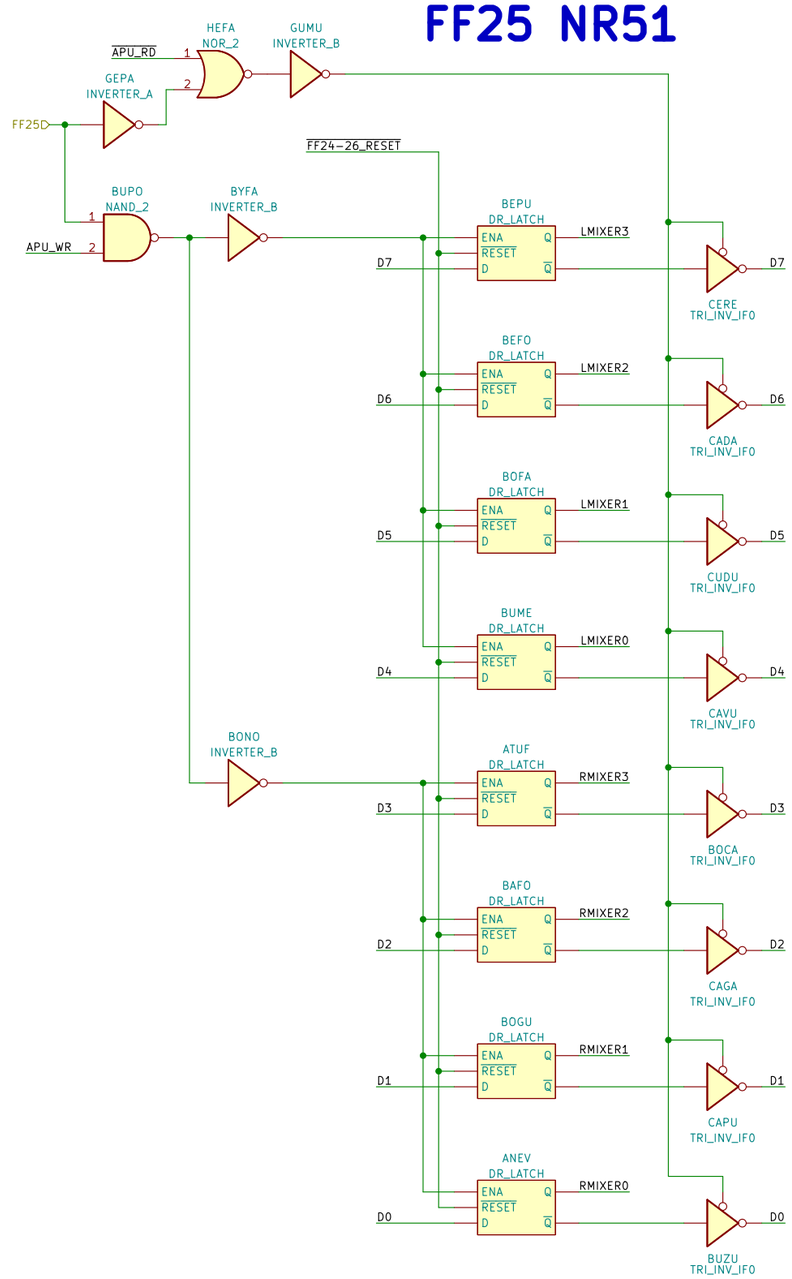
Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 12/45

Mistakes found:
- Reset comes from KEPY and not JYRO
- BUBU, ATAF INV removed since negative clock generators for latches
- L and R mixer wrong way around

FF24 NR50



FF25 NR51



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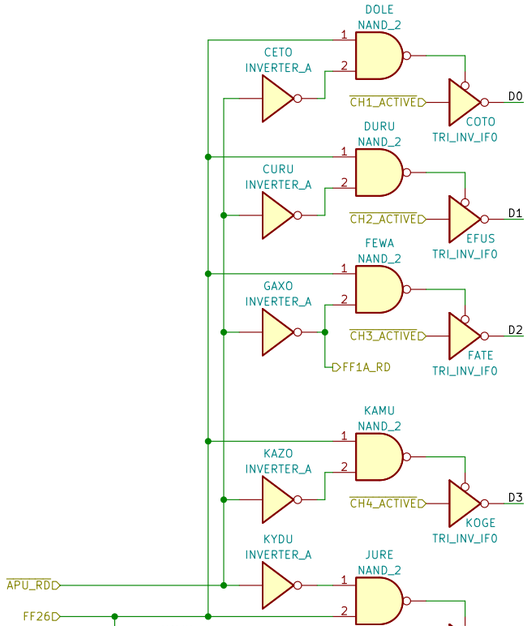
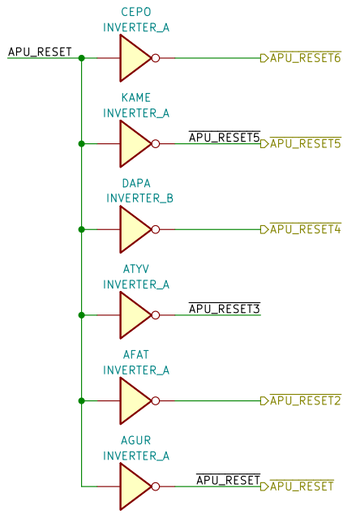
Sheet: /APU/FF24 FF25 CH EN & VOL/
File: ff24_ff25.kicad_sch

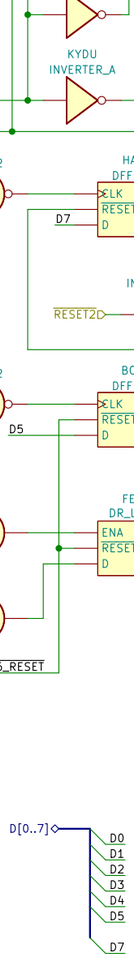
Title: DMG CPU B

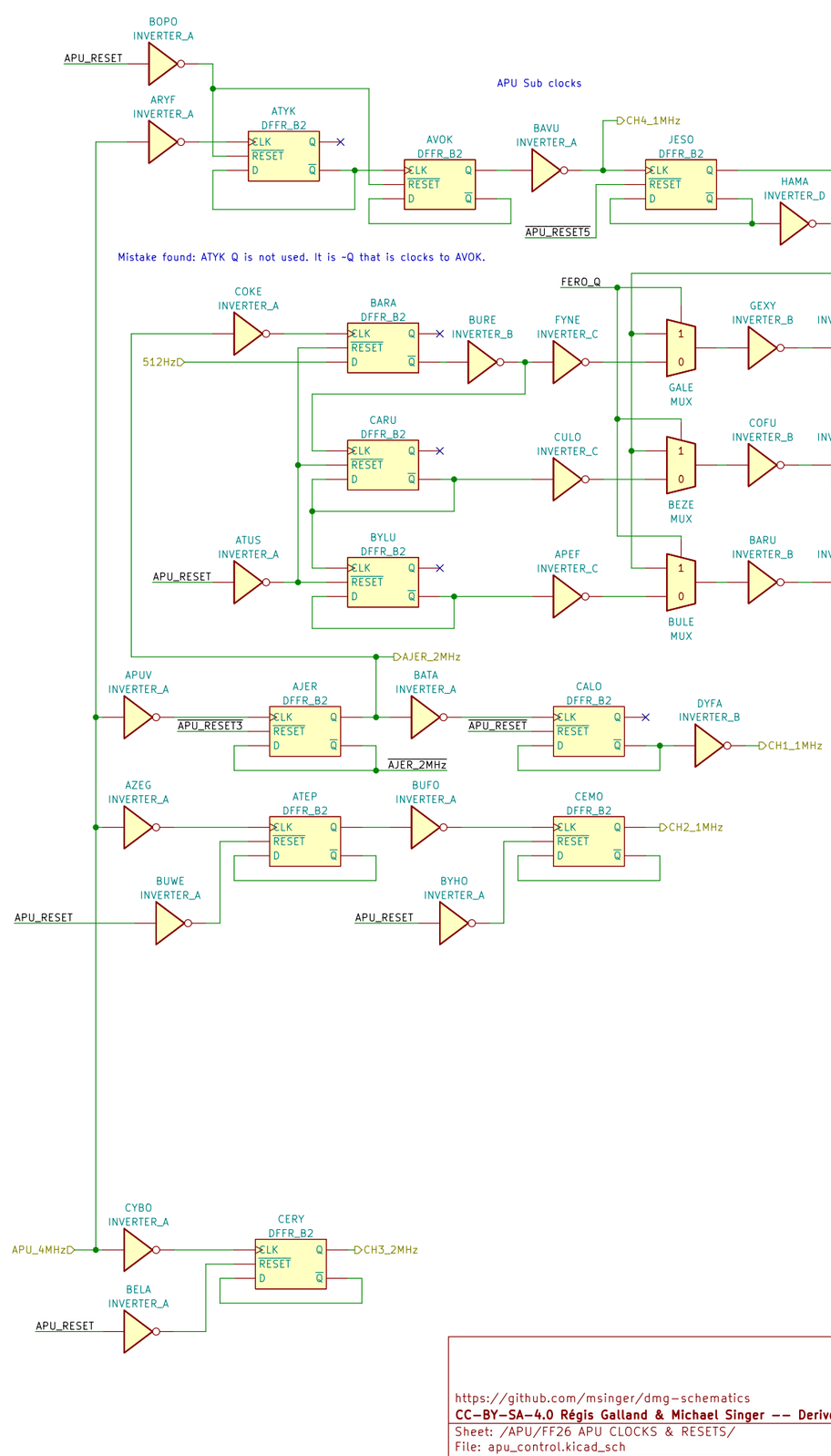
Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311~116-ubuntu22.04.1		Id: 13/45

FF26 NR52









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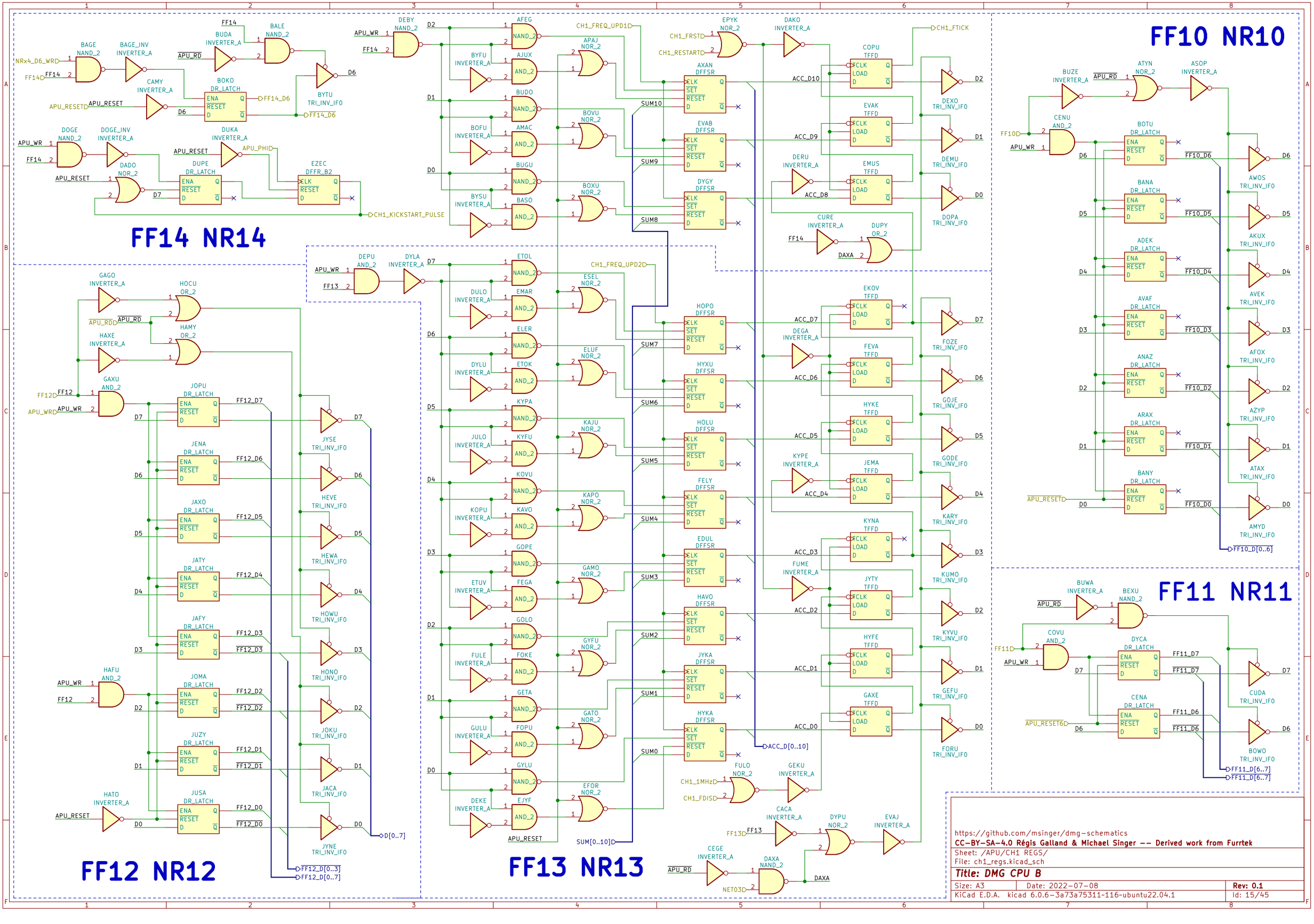
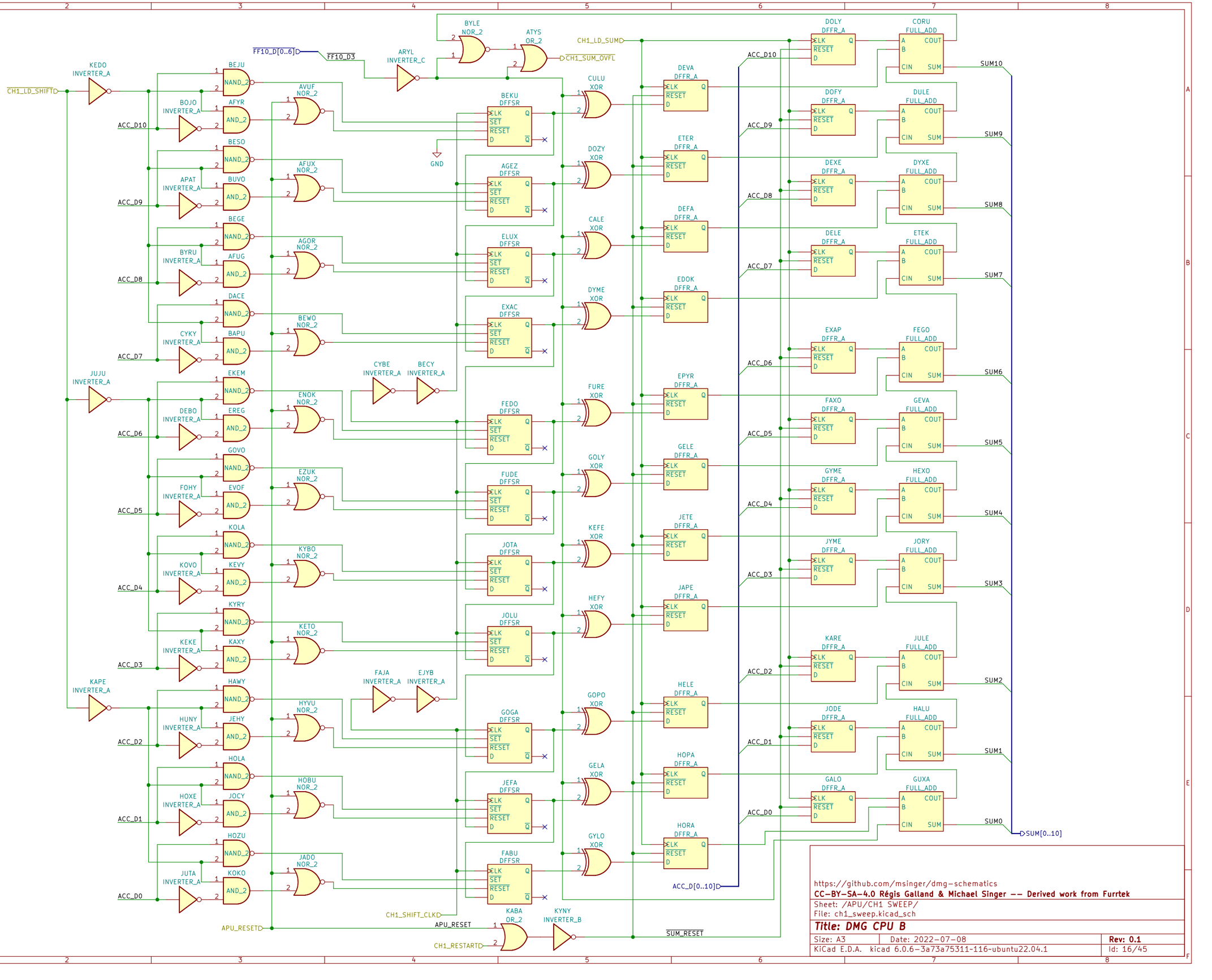
Sheet: /APU/FF26 APU CLOCKS & RESETS/
File: apu_control.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 14/45


FF14 NR14
FF13 NR13
FF12 NR12
FF11 NR11
FF10 NR10
BAGE NAND_2
BAGE_INV INVERTER_A
BUDA INVERTER_A
BALE NAND_2
BOKO DR_LATCH
BYTU TRI_INV_IF0
CAMY INVERTER_A
DOGE NAND_2
DOGE_INV INVERTER_A
DADO NOR_2
DUPE DR_LATCH
DUKA INVERTER_A
EZEC DFFR_B2
DEBY NAND_2
AFEG NAND_2
BYFU INVERTER_A
AJUX NAND_2
BUDO NAND_2
BOFU INVERTER_A
AMAC AND_2
BUGU NAND_2
BYSU INVERTER_A
BASO AND_2
APAJ NOR_2
BOVU NOR_2
BOXU NOR_2
EPYK NOR_2
DAKO INVERTER_A
AXAN DFFSR
EVAB DFFSR
DYGY DFFSR
COPU TFFD
EVAK TFFD
EMUS TFFD
DERU INVERTER_A
CURE INVERTER_A
DUPY OR_2
DEXO TRI_INV_IF0
DEMU TRI_INV_IF0
DOPA TRI_INV_IF0
DEPU AND_2
DYLA INVERTER_A
ETOL NAND_2
DULO INVERTER_A
EMAR AND_2
ELER NAND_2
DYLU INVERTER_A
ETOK AND_2
KYPA NAND_2
JULO INVERTER_A
KYFU AND_2
KOVU NAND_2
KOPU INVERTER_A
KAVO AND_2
GOPE NAND_2
ETUV INVERTER_A
FEGA AND_2
GOLO NAND_2
FULE INVERTER_A
FOKE AND_2
GETA NAND_2
GULU INVERTER_A
FOPU AND_2
GYLU NAND_2
DEKE INVERTER_A
EJYF AND_2
ESEL NOR_2
ELUF NOR_2
KAJU NOR_2
KAPO NOR_2
GAMO NOR_2
GYFU NOR_2
GATO NOR_2
EFOR NOR_2
HOPO DFFSR
HYXU DFFSR
HOLU DFFSR
FELY DFFSR
EDUL DFFSR
HAVO DFFSR
JYKA DFFSR
HYKA DFFSR
EKOV TFFD
FEVA TFFD
HYKE TFFD
JEMA TFFD
KYNA TFFD
JYTY TFFD
HYFE TFFD
GAXE TFFD
FOZE TRI_INV_IF0
GOJE TRI_INV_IF0
GODE TRI_INV_IF0
KARY TRI_INV_IF0
KUMO TRI_INV_IF0
KYVU TRI_INV_IF0
GEFU TRI_INV_IF0
FORU TRI_INV_IF0
DAKE INVERTER_A
DEGA INVERTER_A
KYPE INVERTER_A
FUME INVERTER_A
FULO NOR_2
GEKU INVERTER_A
CACA INVERTER_A
DYPU NOR_2
EVAJ INVERTER_A
CEGE INVERTER_A
DAXA NAND_2
GAGO INVERTER_A
HOCU OR_2
HAMY OR_2
HAXE INVERTER_A
GAXU AND_2
JOPU DR_LATCH
JYSE TRI_INV_IF0
JENA DR_LATCH
HEVE TRI_INV_IF0
JAXO DR_LATCH
HEWA TRI_INV_IF0
JATY DR_LATCH
HOWU TRI_INV_IF0
JAFY DR_LATCH
HONO TRI_INV_IF0
HAFU AND_2
JOMA DR_LATCH
JOKU TRI_INV_IF0
JUZY DR_LATCH
JACA TRI_INV_IF0
HATO INVERTER_A
JUSA DR_LATCH
JYNE TRI_INV_IF0
BUZE INVERTER_A
ATYN NOR_2
ASOP INVERTER_A
CENU AND_2
BOTU DR_LATCH
AWOS TRI_INV_IF0
BANA DR_LATCH
AKUX TRI_INV_IF0
ADEK DR_LATCH
AVEK TRI_INV_IF0
AVAF DR_LATCH
AFOX TRI_INV_IF0
ANAZ DR_LATCH
AZYP TRI_INV_IF0
ARAX DR_LATCH
ATAX TRI_INV_IF0
BANY DR_LATCH
AMYD TRI_INV_IF0
BUWA INVERTER_A
BEXU NAND_2
COVU AND_2
DYCA DR_LATCH
CUDA TRI_INV_IF0
CENA DR_LATCH
BOWO TRI_INV_IF0
APU_WR
APU_RD
APU_RESET
FF14
FF13
FF12
FF11
FF10
D0
D1
D2
D3
D4
D5
D6
D7
CH1_KICKSTART_PULSE
CH1_FREQ_UPD1
CH1_FREQ_UPD2
CH1_FRSTD
CH1_RESTARTD
CH1_FTICK
SUM10
SUM9
SUM8
SUM7
SUM6
SUM5
SUM4
SUM3
SUM2
SUM1
SUM0
SUM[0..10]
ACC_D10
ACC_D9
ACC_D8
ACC_D7
ACC_D6
ACC_D5
ACC_D4
ACC_D3
ACC_D2
ACC_D1
ACC_D0
ACC_D[0..10]
CH1_1MHz
CH1_FDISD
FF13D
NET03D
DAXA
FF10D
FF11D
APU_RESET6D
FF10_D6
FF10_D5
FF10_D4
FF10_D3
FF10_D2
FF10_D1
FF10_D0
FF10_D[0..6]
FF11_D7
FF11_D6
FF11_D[6..7]
FF12_D7
FF12_D6
FF12_D5
FF12_D4
FF12_D3
FF12_D2
FF12_D1
FF12_D0
FF12_D[0..3]
FF12_D[0..7]
D[0..7]
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /APU/CH1 REGS/
File: ch1_regs.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 15/45


CH1_LD_SHIFT
KEDO INVERTER_A
JUJU INVERTER_A
KAPE INVERTER_A
ACC_D10
ACC_D9
ACC_D8
ACC_D7
ACC_D6
ACC_D5
ACC_D4
ACC_D3
ACC_D2
ACC_D1
ACC_D0
BEJU NAND_2
AFYR AND_2
BOJO INVERTER_A
BESO NAND_2
BUVO AND_2
APAT INVERTER_A
BEGE NAND_2
AFUG AND_2
BYRU INVERTER_A
DACE NAND_2
BAPU AND_2
CYKY INVERTER_A
EKEM NAND_2
EREG AND_2
DEBO INVERTER_A
GOVO NAND_2
EVOF AND_2
FOHY INVERTER_A
KOLA NAND_2
KEVY AND_2
KOVO INVERTER_A
KYRY NAND_2
KAXY AND_2
KEKE INVERTER_A
HAWY NAND_2
JEHY AND_2
HUNY INVERTER_A
HOLA NAND_2
JOCY AND_2
HOXE INVERTER_A
HOZU NAND_2
KOKO AND_2
JUTA INVERTER_A
AVUF NOR_2
AFUX NOR_2
AGOR NOR_2
BEWO NOR_2
ENOK NOR_2
EZUK NOR_2
KYBO NOR_2
KETO NOR_2
HYVU NOR_2
HOBU NOR_2
JADO NOR_2
FF10_D[0..6]
FF10_D3
ARYL INVERTER_C
GND
CYBE INVERTER_A
BECY INVERTER_A
FAJA INVERTER_A
EJYB INVERTER_A
BYLE NOR_2
ATYS OR_2
CH1_SUM_OVFL
BEKU DFFSR
AGEZ DFFSR
ELUX DFFSR
EXAC DFFSR
FEDO DFFSR
FUDE DFFSR
JOTA DFFSR
JOLU DFFSR
GOGA DFFSR
JEFA DFFSR
FABU DFFSR
CH1_SHIFT_CLK
APU_RESET
CH1_RESTART
KABA OR_2
KYNY INVERTER_B
CH1_LD_SUM
CULU XOR
DOZY XOR
CALE XOR
DYME XOR
FURE XOR
GOLY XOR
KEFE XOR
HEFY XOR
GOPO XOR
GELA XOR
GYLO XOR
DEVA DFFR_A
ETER DFFR_A
DEFA DFFR_A
EDOK DFFR_A
EPYR DFFR_A
GELE DFFR_A
JETE DFFR_A
JAPE DFFR_A
HELE DFFR_A
HOPA DFFR_A
HORA DFFR_A
ACC_D[0..10]
SUM_RESET
DOLY DFFR_A
DOFY DFFR_A
DEXE DFFR_A
DELE DFFR_A
EXAP DFFR_A
FAXO DFFR_A
GYME DFFR_A
JYME DFFR_A
KARE DFFR_A
JODE DFFR_A
GALO DFFR_A
CORU FULL_ADD
DULE FULL_ADD
DYXE FULL_ADD
ETEK FULL_ADD
FEGO FULL_ADD
GEVA FULL_ADD
HEXO FULL_ADD
JORY FULL_ADD
JULE FULL_ADD
HALU FULL_ADD
GUXA FULL_ADD
SUM10
SUM9
SUM8
SUM7
SUM6
SUM5
SUM4
SUM3
SUM2
SUM1
SUM0
SUM[0..10]
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /APU/CH1 SWEEP/
File: ch1_sweep.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 16/45

Waveform counter

Sweep timer

Duty select

Sweep shift counter

EG timer clocked at 64Hz

Length timer

ERROR: KYLY should be KYNY, KAKE is OR_3, KUKU pin 1 connected to HORU_512Hz
FEMU is NAND LATCH

https://github.com/msinger/dmg-schematics

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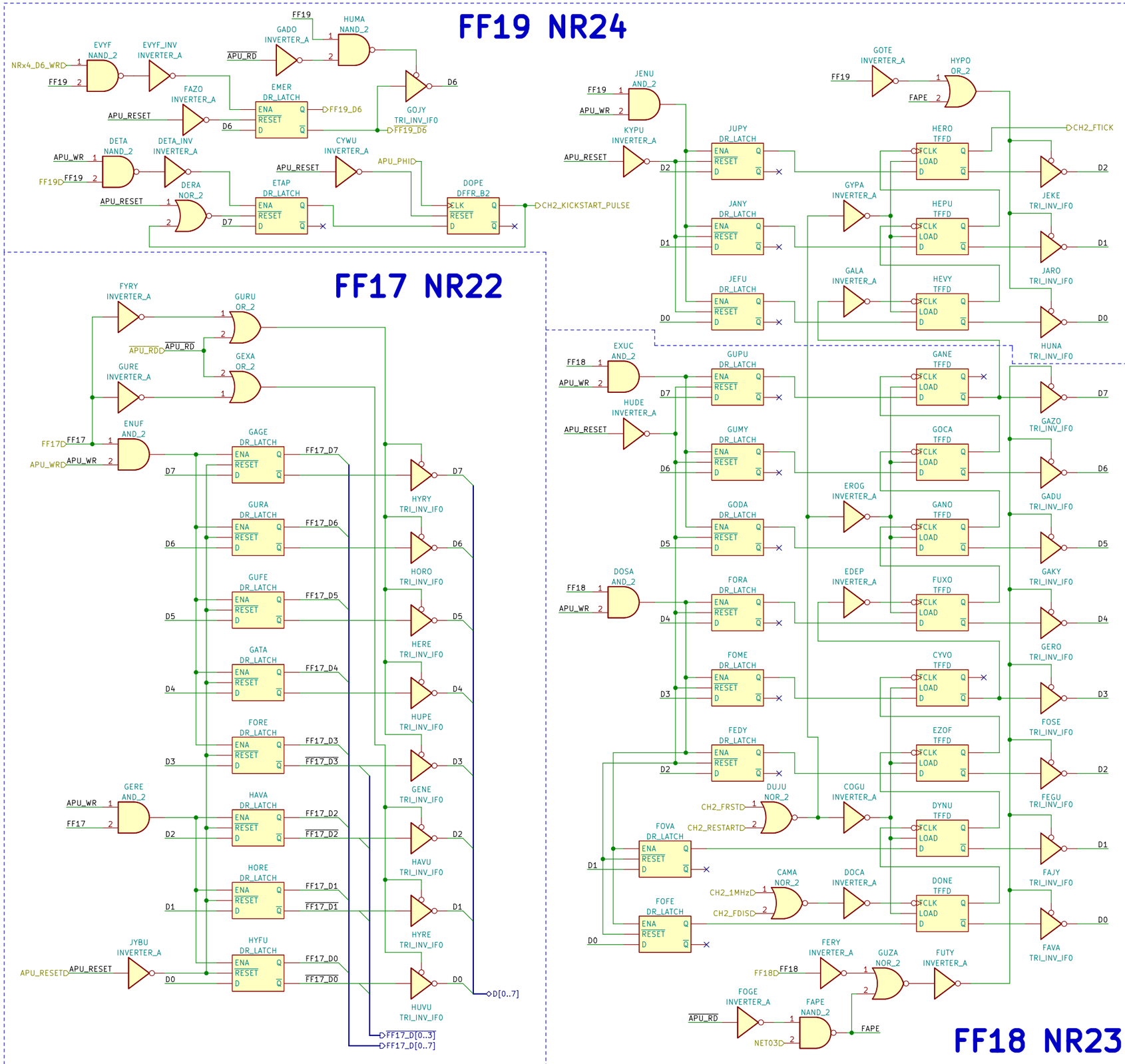
Sheet: /APU/CHANNEL 1/
File: channel1.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 17/45

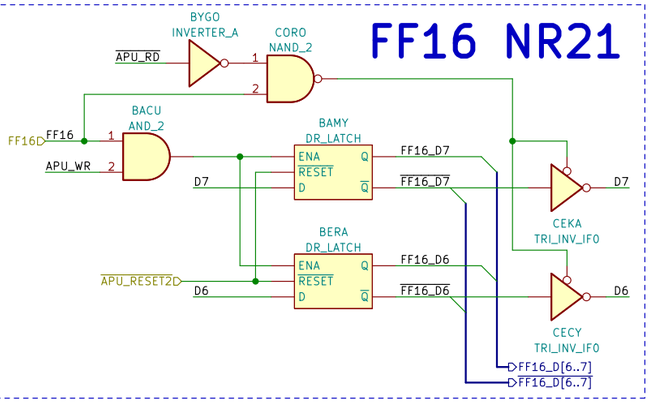
FF19 NR24



FF17 NR22

FF18 NR23

FF16 NR21



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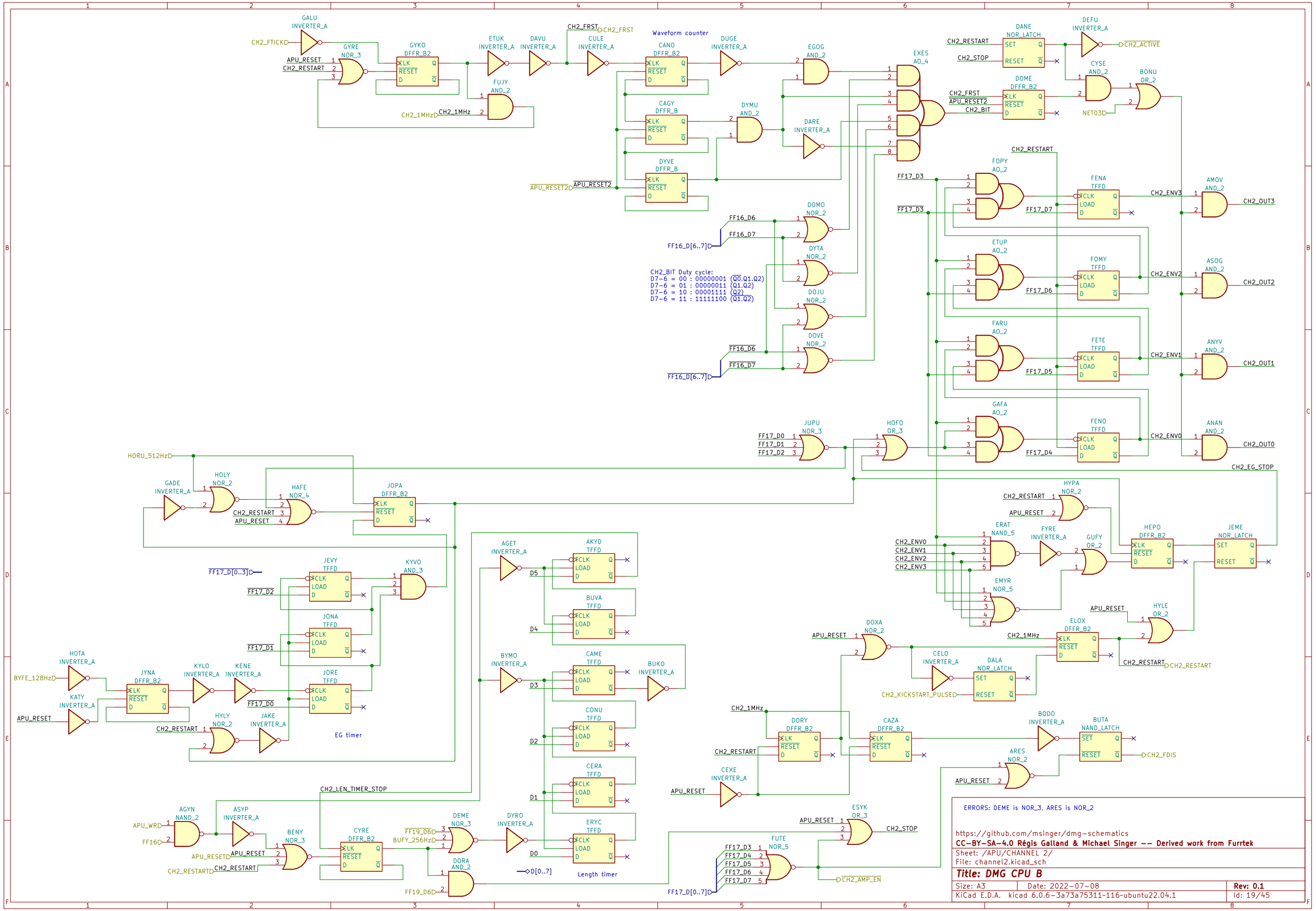
Sheet: /APU/CH2 REGS/		
File: ch2_regs.kicad_sch		
Title: DMG CPU B		
Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 18/45


GALU INVERTER_A
CH2_FTICK
GYRE NOR_3
APU_RESET
CH2_RESTART
GYKO DFFR_B2
ETUK INVERTER_A
DAVU INVERTER_A
CH2_FRST
CULE INVERTER_A
CH2_FRST
Waveform counter
CANO DFFR_B2
DUGE INVERTER_A
EGOG AND_2
FUJY AND_2
CH2_1MHz
CH2_1MHz
CAGY DFFR_B
DYMU AND_2
DARE INVERTER_A
DYVE DFFR_B
APU_RESET2
APU_RESET2
EXES AO_4
DANE NOR_LATCH
CH2_RESTART
CH2_STOP
DEFU INVERTER_A
CH2_ACTIVE
CYSE AND_2
BONU OR_2
DOME DFFR_B2
CH2_FRST
APU_RESET2
CH2_BIT
NET03
CH2_RESTART
FOPY AO_2
FF17_D3
FF17_D3
FENA TFFD
FF17_D7
CH2_ENV3
AMOV AND_2
CH2_OUT3
DOMO NOR_2
FF16_D6
FF16_D7
FF16_D[6..7]
DYTA NOR_2
ETUP AO_2
FOMY TFFD
FF17_D6
CH2_ENV2
ASOG AND_2
CH2_OUT2
CH2_BIT Duty cycle:
D7-6 = 00 : 00000001 (Q0.Q1.Q2)
D7-6 = 01 : 00000011 (Q1.Q2)
D7-6 = 10 : 00001111 (Q2)
D7-6 = 11 : 11111100 (Q1.Q2)
DOJU NOR_2
FARU AO_2
FETE TFFD
FF17_D5
CH2_ENV1
ANYV AND_2
CH2_OUT1
DOVE NOR_2
FF16_D6
FF16_D7
FF16_D[6..7]
JUPU NOR_3
FF17_D0
FF17_D1
FF17_D2
HOFO OR_3
GAFA AO_2
FENO TFFD
FF17_D4
CH2_ENV0
ANAN AND_2
CH2_OUT0
CH2_EG_STOP
HORU_512Hz
GADE INVERTER_A
HOLY NOR_2
HAFE NOR_4
CH2_RESTART
APU_RESET
JOPA DFFR_B2
HYPA NOR_2
CH2_RESTART
APU_RESET
ERAT NAND_5
CH2_ENV0
CH2_ENV1
CH2_ENV2
CH2_ENV3
FYRE INVERTER_A
GUFY OR_2
HEPO DFFR_B2
JEME NOR_LATCH
EMYR NOR_5
FF17_D[0..3]
JEVY TFFD
FF17_D2
KYVO AND_3
JONA TFFD
FF17_D1
JORE TFFD
FF17_D0
HOTA INVERTER_A
BYFE_128Hz
JYNA DFFR_B2
KYLO INVERTER_A
KENE INVERTER_A
KATY INVERTER_A
APU_RESET
HYLY NOR_2
CH2_RESTART
JAKE INVERTER_A
EG timer
AGET INVERTER_A
AKYD TFFD
D5
BUVA TFFD
D4
BYMO INVERTER_A
CAME TFFD
D3
BUKO INVERTER_A
CONU TFFD
D2
CERA TFFD
D1
ERYC TFFD
D0
D[0..7]
Length timer
DOXA NOR_2
APU_RESET
CELO INVERTER_A
CH2_KICKSTART_PULSED
DALA NOR_LATCH
ELOX DFFR_B2
CH2_1MHz
APU_RESET
HYLE OR_2
CH2_RESTART
CH2_RESTART
CH2_1MHz
DORY DFFR_B2
CH2_RESTART
CAZA DFFR_B2
CEXE INVERTER_A
APU_RESET
BODO INVERTER_A
BUTA NAND_LATCH
CH2_FDIS
ARES NOR_2
APU_RESET
CH2_LEN_TIMER_STOP
AGYN NAND_2
APU_WR
FF16
ASYP INVERTER_A
APU_RESET
CH2_RESTART
BENY NOR_3
CYRE DFFR_B2
DEME NOR_3
FF19_D6
BUFY_256Hz
DORA AND_2
FF19_D6
DYRO INVERTER_A
FUTE NOR_5
FF17_D3
FF17_D4
FF17_D5
FF17_D6
FF17_D7
FF17_D[0..7]
ESYK OR_3
APU_RESET
CH2_STOP
CH2_AMP_EN
ERRORS: DEME is NOR_3, ARES is NOR_2
https://github.com/msinger/dmg-schematics
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Sheet: /APU/CHANNEL 2/
File: channel2.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1
Id: 19/45

FF1A NR30

GEJO AND_2 — FF1A, APU_WR → GOVE INVERTER_A → APU_RESET, D7 → GUXE DR_LATCH (ENA, RESET, D, Q, Q̄) → CH3_AMP_EN

FASY NAND_2 — FF1A, FF1A_RDD → GEKO TRI_INV_IF0 → D7

FEVO INVERTER_A — CH3_AMP_EN

FUVO NOR_2 — CH3_AMP_EN, APU_RESET → GUGU NAND_LATCH (RESET, SET, Q, Q̄) → CH3_FDIS

CH3_2MHz → FABO INVERTER_A → GYTA DFFR_B2 (CLK, RESET, D, Q, Q̄) → GYRA DFFR_B2 → FAJU INVERTER_A

CH3_RESTART, GAZE INVERTER_A, APU_RESET

FURY NOR_2 — APU_RESET, GULO INVERTER_A → GOFY NOR_LATCH (SET, RESET, Q, Q̄) → GARA DFFR_B2 → CH3_RESTART

EPYX NAND_2 — APU_WR, FF1E → EPYX_INV INVERTER_A → FAKO NOR_2 — APU_RESET, D7 → GAVU DR_LATCH (ENA, RESET, D, Q, Q̄)

GOMA INVERTER_A — APU_RESET → FOBA DFFR_B2 — APU_PHID

FF1E NR34

FOVO NAND_2 — NRx4_D6_WR, FF1E → FOVO_INV INVERTER_A → HEKY INVERTER_A — APU_RESET, D6 → HOTO DR_LATCH (ENA, RESET, D, Q, Q̄) → FF1E_D6, FF1E_D6 → HACA TRI_INV_IF0 → D6

GORY INVERTER_A — APU_RD, FF1E → GAWA NAND_2

KOPY INVERTER_A — APU_RESET

HUDA AND_2 — FF1E, APU_WR

JACY DR_LATCH (ENA, RESET, D, Q, Q̄) — D2

JETY DR_LATCH — D1

JEMO DR_LATCH — D0

GUNU INVERTER_A — FF1E

FUVA OR_2 — EGAD, CH3_FTICK

JAPU TFFD (CLK, LOAD, D, Q, Q̄) → HUFO TRI_INV_IF0 → D2

JERA INVERTER_A

KEZA TFFD → JURA TRI_INV_IF0 → D1

KESE INVERTER_A

KEJU TFFD → JUVY TRI_INV_IF0 → D0

KOTA AND_2 — FF1D, APU_WR

KOGU DR_LATCH — D7

KANA DR_LATCH — D6

JOVE DR_LATCH — D5

JYPO DR_LATCH — D4

JAFA AND_2 — FF1D, APU_WR

JEFE DR_LATCH — D3

JAXA DR_LATCH — D2

JOVY DR_LATCH — D1

KOGA DR_LATCH — D0

KENO TFFD → KAMY TRI_INV_IF0 → D7

KASO INVERTER_A

KAFO TFFD → KORA TRI_INV_IF0 → D6

KYRU INVERTER_A

KEPA TFFD → JEZA TRI_INV_IF0 → D5

KYKO INVERTER_A

KYGU TFFD → JUKE TRI_INV_IF0 → D4

JUTY INVERTER_A

KEMU TFFD → JUDE TRI_INV_IF0 → D3

KUNU TFFD → KESY TRI_INV_IF0 → D2

KUPE TFFD → KAFU TRI_INV_IF0 → D1

KUTU TFFD → JOFO TRI_INV_IF0 → D0

D[0..7]

HERA NOR_2 — CH3_FRSTD, CH3_RESTART

HEFO NOR_2 — CH3_2MHz, CH3_FDIS

KUHA INVERTER_A — APU_RESETD, APU_RESET

HOXA INVERTER_A — FF1D

GUTE NOR_2 — HOXA, EGAD

HOVO INVERTER_A

EGAD NAND_2 — NET03, EGAD

DOVO INVERTER_A — APU_RDD, APU_RD

FF1C NR32

JOTU INVERTER_A — APU_RD

HENU NAND_2 — JOTU, HAGA AND_2 — APU_WR, FF1C

HUKY DR_LATCH (ENA, RESET, D, Q, Q̄) — FF1C_D6, FF1C_D6 → HUCO TRI_INV_IF0 → D6

GURO INVERTER_A — APU_RESET

HODY DR_LATCH — FF1C_D5, FF1C_D5 → HAMU TRI_INV_IF0 → D5

FF1C_D[5..6], FF1C_D[5..6]

FF1B NR31

DERY NAND_2 — APU_WR, FF1B

GETO INVERTER_A

GUDA NOR_3 — APU_RESET, CH3_RESTART

FEXU DFFR_B2 (CLK, RESET, D, Q) — BUFY_256Hz

CH3_LEN_TIMER_STOP

GEDO AND_2 — FF1E_D6

GEPY NOR_3 — FF1E_D6, BUFY_256Hz

GENU INVERTER_A

GAJY INVERTER_A

EMUT INVERTER_A — D7

FYRU TFFD (CLK, LOAD, D, Q, Q̄)

FAVE TFFD — D6

FORO TFFD — D5

GEMO TFFD — D4

GAPO TFFD — D3

FALU INVERTER_A

GATU TFFD — D2

FORY TFFD — D1

GEVO TFFD — D0

Length timer

FYGO OR_3 — APU_RESET, CH3_AMP_EN

CH3_RESTART

FOZU NOR_LATCH (SET, RESET, Q, Q̄)

EZAS INVERTER_A

DORU INVERTER_A

AJER_2MHz

CALU INVERTER_A — APU_RESET

DAVO DFFR_B2 (CLK, RESET, D, Q)

COKA INVERTER_B

ERED INVERTER_A — CH3_ACTIVE, CH3_ACTIVE

https://github.com/msinger/dmg-schematics
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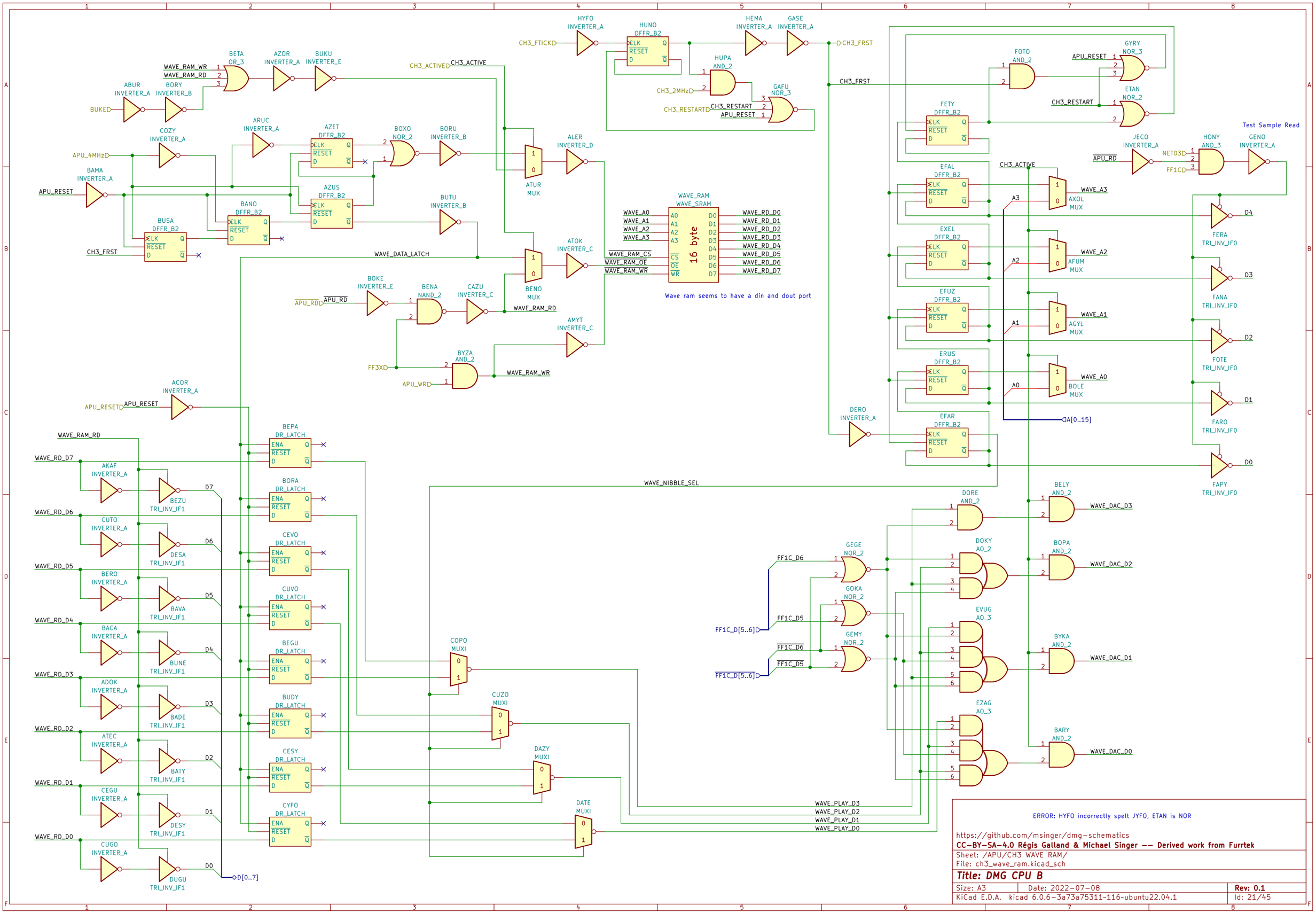
Sheet: /APU/CH3 REGS/
File: ch3_regs.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 20/45


HYFO INVERTER_A
CH3_FTICKD
HUNO DFFR_B2
HEMA INVERTER_A
GASE INVERTER_A
CH3_FRST
HUPA AND_2
CH3_2MHz
CH3_RESTARTD
GAFU NOR_3
CH3_RESTART
APU_RESET
BETA OR_3
WAVE_RAM_WR
WAVE_RAM_RD
AZOR INVERTER_A
BUKU INVERTER_E
CH3_ACTIVED
CH3_ACTIVE
ABUR INVERTER_A
BORY INVERTER_B
BUKED
COZY INVERTER_A
APU_4MHz
ARUC INVERTER_A
AZET DFFR_B2
BOXO NOR_2
BORU INVERTER_B
ALER INVERTER_D
ATUR MUX
BAMA INVERTER_A
APU_RESET
AZUS DFFR_B2
BANO DFFR_B2
BUTU INVERTER_B
BUSA DFFR_B2
CH3_FRST
WAVE_DATA_LATCH
ATOK INVERTER_C
BENO MUX
WAVE_RAM
WAVE_SRAM
16 byte
WAVE_A0
WAVE_A1
WAVE_A2
WAVE_A3
WAVE_RAM_CS
WAVE_RAM_OE
WAVE_RAM_WR
WAVE_RD_D0
WAVE_RD_D1
WAVE_RD_D2
WAVE_RD_D3
WAVE_RD_D4
WAVE_RD_D5
WAVE_RD_D6
WAVE_RD_D7
Wave ram seems to have a din and dout port
BOKE INVERTER_E
APU_RDD
APU_RD
BENA NAND_2
CAZU INVERTER_C
WAVE_RAM_RD
AMYT INVERTER_C
FF3XD
BYZA AND_2
APU_WRD
WAVE_RAM_WR
ACOR INVERTER_A
APU_RESETD
APU_RESET
WAVE_RAM_RD
WAVE_RD_D7
AKAF INVERTER_A
BEZU TRI_INV_IF1
D7
BEPA DR_LATCH
BORA DR_LATCH
WAVE_RD_D6
CUTO INVERTER_A
DESA TRI_INV_IF1
D6
CEVO DR_LATCH
WAVE_RD_D5
BERO INVERTER_A
BAVA TRI_INV_IF1
D5
CUVO DR_LATCH
WAVE_RD_D4
BACA INVERTER_A
BUNE TRI_INV_IF1
D4
BEGU DR_LATCH
WAVE_RD_D3
ADOK INVERTER_A
BADE TRI_INV_IF1
D3
BUDY DR_LATCH
WAVE_RD_D2
ATEC INVERTER_A
BATY TRI_INV_IF1
D2
CESY DR_LATCH
WAVE_RD_D1
CEGU INVERTER_A
DESY TRI_INV_IF1
D1
CYFO DR_LATCH
WAVE_RD_D0
CUGO INVERTER_A
DUGU TRI_INV_IF1
D0
D[0..7]
WAVE_NIBBLE_SEL
COPO MUXI
CUZO MUXI
DAZY MUXI
DATE MUXI
FF1C_D[5..6]
FF1C_D6
FF1C_D5
GEGE NOR_2
GOKA NOR_2
GEMY NOR_2
DERO INVERTER_A
FOTO AND_2
GYRY NOR_3
APU_RESET
ETAN NOR_2
CH3_RESTART
FETY DFFR_B2
JECO INVERTER_A
APU_RD
HONY AND_3
NET03
FF1CD
GENO INVERTER_A
Test Sample Read
EFAL DFFR_B2
CH3_ACTIVE
WAVE_A3
AXOL MUX
A3
EXEL DFFR_B2
WAVE_A2
AFUM MUX
A2
EFUZ DFFR_B2
WAVE_A1
AGYL MUX
A1
ERUS DFFR_B2
WAVE_A0
BOLE MUX
A0
EFAR DFFR_B2
A[0..15]
FERA TRI_INV_IF0
D4
FANA TRI_INV_IF0
D3
FOTE TRI_INV_IF0
D2
FARO TRI_INV_IF0
D1
FAPY TRI_INV_IF0
D0
DORE AND_2
BELY AND_2
WAVE_DAC_D3
DOKY AO_2
BOPA AND_2
WAVE_DAC_D2
EVUG AO_3
BYKA AND_2
WAVE_DAC_D1
EZAG AO_3
BARY AND_2
WAVE_DAC_D0
WAVE_PLAY_D3
WAVE_PLAY_D2
WAVE_PLAY_D1
WAVE_PLAY_D0
ERROR: HYFO incorrectly spelt JYFO, ETAN is NOR
https://github.com/msinger/dmg-schematics
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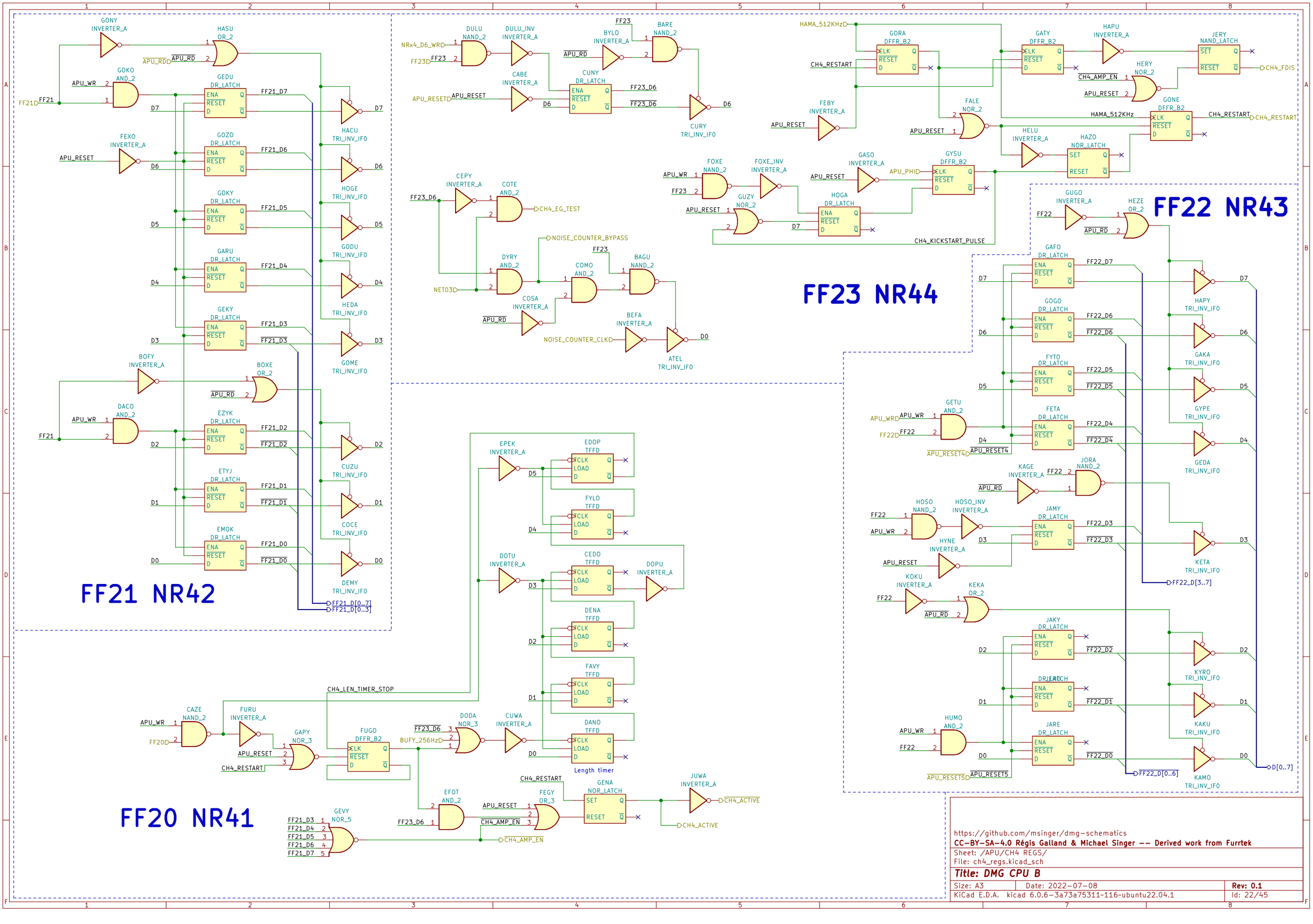
Sheet: /APU/CH3 WAVE RAM/
File: ch3_wave_ram.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 21/45


FF21 NR42
FF23 NR44
FF22 NR43
FF20 NR41
GONY INVERTER_A
HASU OR_2
APU_RD
APU_WR
GOKO AND_2
FF21
GEDU DR_LATCH
FF21_D7
D7
HACU TRI_INV_IF0
FEXO INVERTER_A
APU_RESET
GOZO DR_LATCH
FF21_D6
D6
HOGE TRI_INV_IF0
GOKY DR_LATCH
FF21_D5
D5
GODU TRI_INV_IF0
GARU DR_LATCH
FF21_D4
D4
HEDA TRI_INV_IF0
GEKY DR_LATCH
FF21_D3
D3
GOME TRI_INV_IF0
BOFY INVERTER_A
BOXE OR_2
DACO AND_2
EZYK DR_LATCH
FF21_D2
D2
CUZU TRI_INV_IF0
ETYJ DR_LATCH
FF21_D1
D1
COCE TRI_INV_IF0
EMOK DR_LATCH
FF21_D0
D0
DEMY TRI_INV_IF0
FF21_D[0..7]
FF21_D[0..3]
DULU NAND_2
DULU_INV INVERTER_A
NRx4_D6_WR
FF23
BYLO INVERTER_A
BARE NAND_2
CABE INVERTER_A
CUNY DR_LATCH
FF23_D6
CURY TRI_INV_IF0
CEPY INVERTER_A
COTE AND_2
CH4_EG_TEST
NOISE_COUNTER_BYPASS
DYRY AND_2
NET03
COMO AND_2
BAGU NAND_2
COSA INVERTER_A
BEFA INVERTER_A
NOISE_COUNTER_CLK
ATEL TRI_INV_IF0
HAMA_512KHz
GORA DFFR_B2
CH4_RESTART
GATY DFFR_B2
HAPU INVERTER_A
JERY NAND_LATCH
CH4_FDIS
CH4_AMP_EN
HERY NOR_2
FEBY INVERTER_A
FALE NOR_2
GONE DFFR_B2
CH4_RESTART
HELU INVERTER_A
HAZO NOR_LATCH
FOXE NAND_2
FOXE_INV INVERTER_A
GASO INVERTER_A
GYSU DFFR_B2
APU_PHI
GUZY NOR_2
HOGA DR_LATCH
CH4_KICKSTART_PULSE
GUGO INVERTER_A
HEZE OR_2
GAFO DR_LATCH
FF22_D7
HAPY TRI_INV_IF0
GOGO DR_LATCH
FF22_D6
GAKA TRI_INV_IF0
FYTO DR_LATCH
FF22_D5
GYPE TRI_INV_IF0
GETU AND_2
FETA DR_LATCH
FF22_D4
GEDA TRI_INV_IF0
APU_RESET4
KAGE INVERTER_A
JORA NAND_2
HOSO NAND_2
HOSO_INV INVERTER_A
JAMY DR_LATCH
FF22_D3
KETA TRI_INV_IF0
HYNE INVERTER_A
KOKU INVERTER_A
KEKA OR_2
FF22_D[3..7]
JAKY DR_LATCH
FF22_D2
KYRO TRI_INV_IF0
JARE DR_LATCH
FF22_D1
KAKU TRI_INV_IF0
HUMO AND_2
FF22_D0
KAMO TRI_INV_IF0
APU_RESET5
FF22_D[0..6]
D[0..7]
EPEK INVERTER_A
EDOP TFFD
FYLO TFFD
CEDO TFFD
DOPU INVERTER_A
DENA TFFD
FAVY TFFD
DANO TFFD
DOTU INVERTER_A
Length timer
CH4_LEN_TIMER_STOP
CAZE NAND_2
FURU INVERTER_A
GAPY NOR_3
FUGO DFFR_B2
BUFY_256Hz
DODA NOR_3
CUWA INVERTER_A
EFOT AND_2
FEGY OR_3
GENA NOR_LATCH
JUWA INVERTER_A
CH4_ACTIVE
GEVY NOR_5
FF21_D3
FF21_D4
FF21_D5
FF21_D6
FF21_D7
CH4_AMP_EN
https://github.com/msinger/dmg-schematics
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Sheet: /APU/CH4 REGS/
File: ch4_regs.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1
Id: 22/45

APU_RESET4
ESEP DFFR_B2
DERE DFFR_B2
DOTA DFFR_B2
ERUT DFFR_B2
DETE DFFR_B2
DOSE DFFR_B2
DEMO DFFR_B2
DOKE DFFR_B2
DALE DFFR_B2
DURE DFFR_B2
EPOR DFFR_B2
EZEF DFFR_B2
DEKO DFFR_B2
CEXO DFFR_B2

FF22_D7-4 = "1101", Noise Counter CLK/16384
FF22_D7-4 = "1100", Noise Counter CLK/8192
FF22_D7-4 = "1011", Noise Counter CLK/4096
FF22_D7-4 = "1010", Noise Counter CLK/2048
FF22_D7-4 = "1001", Noise Counter CLK/1024
FF22_D7-4 = "1000", Noise Counter CLK/512
FF22_D7-4 = "0111", Noise Counter CLK/256
FF22_D7-4 = "0110", Noise Counter CLK/128
FF22_D7-4 = "0101", Noise Counter CLK/64
FF22_D7-4 = "0100", Noise Counter CLK/32
FF22_D7-4 = "0011", Noise Counter CLK/16
FF22_D7-4 = "0010", Noise Counter CLK/8
FF22_D7-4 = "0001", Noise Counter CLK/4
FF22_D7-4 = "0000", Noise Counter CLK/2

ETYR AO_6
ELYX AO_4
DARY AO_4
FF21_D[0..7]

FF22_D[0..6]
FF22_D[3..7]
EMOF NOR_3
ELAR NOR_3
DUDU NOR_3
ETAT NOR_3
FURA NOR_3
ETAR NOR_3
EVER NOR_3
ETOV NOR_3

NOISE_COUNTER_CLK
JYFU TFFD
JYRE TFFD
JYCO TFFD
CH4_1MHz
GYBA INVERTER_A
HYNO AND_3
GUNY NOR_2
GARY DFFR_B2
CARY AND_2
FF22_D2
FF22_D1
FF22_D0
APU_RESET
CH4_RESTART

Frequency divider:
Noise Counter CLK = 1MHz/ 1, 2, 4, 6, 8, 10, 12 or 14

CH4_FDISC
JESO_512K
KYKU OR_2
KONY INVERTER_A
KANU INVERTER_A
GOFU NOR_2
HUCE INVERTER_A

FF22_D7
ERYF OR_2
FEME MUX
NOISE_COUNTER_BYPASSD
CH4_LFSR_CLK1
LFSR_OUT
EZUL MUX
GUFA INVERTER_A
GYVE INVERTER_A
KARA INVERTER_A
KOPA INVERTER_A
CH4_LFSR_CLK2
CH4_LFSR_CLK3
DATO OR_2
CH4_RESTART
CH4_EG_TEST
ELAF AO_2
FF21_D3
FF21_D7
FYRO TFFD
CH4_ENV3
BOZA AND_2
CH4_OUT3
EDYF AO_2
FF21_D6
FERU TFFD
CH4_ENV2
APYR AND_2
CH4_OUT2
ETEF AO_2
FF21_D5
FATY TFFD
CH4_ENV1
BYZY AND_2
CH4_OUT1
FOLE AO_2
FF21_D4
FEKO TFFD
CH4_ENV0
AKOF AND_2
CH4_OUT0
CH4_EG_STOP
CH4_EG_TICK
FELO OR_3
FOWA NOR_3
FF21_D0
FF21_D1
FF21_D2
EMET NOR_2
CH4_RESTARTD
APU_RESET
CUTY NAND_5
DUBO INVERTER_A
EVUR OR_2
DARO NOR_5
FYNO DFFR_B2
EROX NOR_LATCH
ENUR OR_2
CH4_ENV0
CH4_ENV1
CH4_ENV2
CH4_ENV3
CH4_EG_DISABLE
GOPA NOR_4
FOSY DFFR_B2
HORU_512Hz
HURY NOR_2
GEXE INVERTER_A
ALOP INVERTER_A
BOKY INVERTER_A
ABEL DFFR_B2
BAWA INVERTER_A
BUXO INVERTER_A
BYFE_128Hz
64Hz
DOGO TFFD
COFE TFFD
CUNA TFFD
EJEX AND_3
FF21_D[0..3]
EG timer
GAME NAND_2
LFSR_OUT
ENEC NOR_2
DAPY INVERTER_A
HURA XNOR

GEPO OR_2
GOGE INVERTER_B
JYJA INVERTER_A
KAVU AO_2
JEPE DFFR_B2
JAVO DFFR_B2
HEPA DFFR_B2
HORY DFFR_B2
HENO DFFR_B2
HYRO DFFR_B2
HEZU DFFR_B2
JOTO DFFR_B2
KOMU DFFR_B2
KETU DFFR_B2
KUTA DFFR_B2
KUZY DFFR_B2
KYWY DFFR_B2
JAJU DFFR_B2
HAPE DFFR_B2
JUXE DFFR_B2
bit13_xnor_bit14

https://github.com/msinger/dmg-schematics
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Sheet: /APU/CHANNEL 4/
File: channel4.kicad_sch
Title: DMG CPU B
Size: A3 | Date: 2022-07-08 | **Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1 | Id: 23/45

PPU DECODE & VIDEO CONTROL

File: ppu_decode.kicad_sch

CPU_RD
CPU_WR
FFXX
RESET2
PPU_4MHz
A[0..15]
D[0..7]
PPU_HARD_RESET
PPU_RESET
FF46
FF45
FF44
FF41
FF4B
FF4A
FF43
FF42
PPU_WR
PPU_RD
PPU_4MHz
DMA_PHI2
FF40_D[0..7]
FF49
FF48
FF47

FF47–FF49 PALETTES

PPU_RD
PPU_WR
D[0..7]
FF47
FF48
FF49
SP0_D[0..7]
SP1_D[0..7]
BGP_D[0..7]

File: palettes.kicad_sch

PIXEL MUX

FF40_D[0..7]
BG_PX_A
BG_PX_B
BGP_D[0..7]
SP1_D[0..7]
SP0_D[0..7]
SPRITE_PX_A7
SPRITE_PX_B7
SPRITE_PX_PRIORITY
SPRITE_PX_PALETTE

File: pixel_mux.kicad_sch

FF42–FF43 BACKGROUND SCROLLING

PPU_RD
PPU_WR
D[0..7]
FF42
FF43
PPU_HARD_RESET
FF40_D[0..7]
FF43_D[0..7]
MA[0..12]
H[0..7]
V[0..7]
BP_SEL
BP_CY
TM_CY
IN_WINDOW

File: background.kicad_sch

BG PIXEL SHIFTER

FF40_D[0..7]
MA[0..12]
BP_CY
MD[0..7]
BG_PX_AD
BG_PX_BD
CLKPIPE
LATCH_BG_BP_A
CLK_BG_BP_B
BG_CY_RST

File: bg_px_shifter.kicad_sch

VRAM INTERFACE

D[0..7]
A[0..15]
PPU_HARD_RESET
MD[0..7]
FEXX–FFXX
WRITE
CPU_WR_SYNC
T1T2
RAM_CS_EN
NOT_VRAM_MEM_RQ
TM_BP_CYS
VRAM_TO_OAM
OAM_RD
TACU
MODE3
SP_BP_CYS
MA[0..12]

File: vram_interface.kicad_sch

FF4A–FF4B WINDOW DETECTION

PPU_RD
PPU_WR
D[0..7]
FF4A
FF4B
PPU_HARD_RESET
PPU_RESET
FF40_D[0..7]
PPU_RESET2
BP_SEL
BP_CY
TM_CY
IN_WINDOW
WX_RST
WX_CLK
WXY_MATCH
MA[0..12]
V[0..7]
H[0..7]
HCLK
INT_VBL

File: win_detect.kicad_sch

BG & WIN CYCLES

PPU_RESET
PPU_4MHz
PPU_RESET2
BP_SEL
BP_CY
TM_CY
IN_WINDOW
WX_RST
WX_CLK
WXY_MATCH
FF40_D[0..7]
FF43_D[0..7]
H[0..7]
PX9
STOP_MODE3
H_RESET
SPRITE_X_MATCH
MODE3
ATEJ
STOP_OAM_PARSING
BG_CY_RST
CLK_BG_BP_BD
LATCH_BG_BP_AD
CLKPIPE
TM_BP_CYSD
LYRY
TAVE
TOMU

File: bg_win_cycles.kicad_sch

FF41 STAT, FF44 LY & FF45 LYC

PPU_RD
PPU_WR
D[0..7]
FF41
FF44
FF45
PPU_HARD_RESET
PPU_4MHz
INT_VBL_BUF
INT_STAT
PX9
STOP_MODE3
H_RESET
STOP_OAM_PARSING
ATEJ
MODE3
SPRITE_X_MATCH
CLKPIPE
MODE1
H[0..7]
V[0..7]
VCLK2
V_RESET
VCLK
HCLK
INT_VBL

File: ff41_stat.kicad_sch

SPRITE CONTROL

SAVE_SPRITE_Y[0..9]
SAVE_SPRITE_NUM[0..9]
PPU_RESET
PPU_4MHz
ATEJ
SAVE_SPRITE_X[0..9]
SPRITE_SAVE_EN

File: sprite_control.kicad_sch

SPRITE STORE 0–4

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]
SAVE_SPRITE_NUM[0..9]
SAVE_SPRITE_Y[0..9]
SPRITE_SEL[0..9]

File: sprite_store_part1.kicad_sch

SPRITE STORE 5–9

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]
SAVE_SPRITE_NUM[0..9]
SAVE_SPRITE_Y[0..9]
SPRITE_SEL[0..9]

File: sprite_store_part2.kicad_sch

SPRITE X PRIORITY

PPU_RESET
FF40_D[0..7]
SPRITE_SEL[0..9]
SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
OAM_RENDERING2
ATEJ
SPRITE_X_MATCH
WUTY

File: sprite_x.kicad_sch

SPRITE X MATCHERS 0–4

SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
H[0..7]
SPRITE_X[0..7]
SAVE_SPRITE_X[0..9]

File: sprite_x_matchers_part1.kicad_sch

SPRITE X MATCHERS 5–9

SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
H[0..7]
SPRITE_X[0..7]
SAVE_SPRITE_X[0..9]

File: sprite_x_matchers_part2.kicad_sch

SPRITE Y COMPARATOR

PPU_RESET
PPU_4MHz
FF40_D[0..7]
SPRITE_Y_STORE[0..3]
V[0..7]
LYRY
TAVE
TOMU
MODE3
TACU
XUJA
TUVO
COTA
OAM_DATA_LATCH
D[0..7]
OAM_B_D[0..7]
OAM_B_RD
SPRITE_Y_MATCHD
MA[0..12]
ATEJ
SPRITE_X_MATCH
WUTYD
SPRITE_Y_FLIP
SP_BP_CYSD
LATCH_SP_BP_AD
LATCH_SP_BP_BD

File: sprite_y_comparator.kicad_sch

SPRITE X MATCH TOP

WUTY
SPRITE_Y_FLIP
CLKPIPE
COTA
OAM_DATA_LATCH
D[0..7]
OAM_A_D[0..7]
OAM_A_RD
SPRITE_X[0..7]
SPRITE_PX_PALETTE
SPRITE_PX_PRIORITY
SPRITE_X_FLIP
SPRITE_ON[0..7]
SPRITE_PX_A[0..7]
SPRITE_PX_B[0..7]

File: sprite_x_match.kicad_sch

SP PIXEL SHIFTER

SPRITE_PX_B[0..7]
SPRITE_PX_A[0..7]
MD[0..7]
SPRITE_ON[0..7]
SPRITE_X_FLIP
SPRITE_PX_B7
SPRITE_PX_A7
CLKPIPE
SP_BP_CYS
LATCH_SP_BP_A
LATCH_SP_BP_B

File: sp_px_shifter.kicad_sch

OAM

MD[0..7]
OAM_RENDER_A[2..7]
PPU_HARD_RESET
PPU_4MHz
MODE1
MODE3
OAM_RD
TACU
XUJA
TUVO
COTA
OAM_DATA_LATCH
D[0..7]
OAM_B_D[0..7]
OAM_B_RD
XOCE
XUPY
XYSO
OAM_RENDERING
OAM_PARSING
OAM_PARSE_A[2..7]
OAM_A_D[0..7]
OAM_A_RD
DMA_PHI2
VRAM_TO_OAM
DMA_RUN
DMA_PHI
OAM_ADDR_DMA
DMA_A[0..15]
PPU_RD
PPU_WR
A[0..15]
CPU_T4
FEXX

File: oam.kicad_sch

LCD

PPU_RESET
PPU_4MHz
8192Hz
4096Hz
FF40_D[0..7]
STOP_OAM_PARSING
SPRITE_SAVE_EN
OAM_RENDERING2
SPRITE_Y_MATCH
INT_VBLD
HCLKD
VCLKD
V_RESETD
VCLK2D
V[0..7]
MODE3D
ATEJD
XOCED
XUPYD
XYSOD
OAM_RENDERINGD
OAM_PARSINGD
OAM_PARSE_A[2..7]D

File: lcd.kicad_sch

FF46 DMA

PPU_RD
PPU_WR
D[0..8]
FF46
PPU_HARD_RESET
DMA_PHI
MA[0..12]
DMA_PHI2D
VRAM_TO_OAM
DMA_RUN
DMA_PHI
OAM_ADDR_DMA
DMA_A[0..15]
DMA_ADDR_EXT

File: ff46_dma.kicad_sch

INT_VBL_BUF
INT_STAT
8192Hz
4096Hz
DMA_PHI
CPU_T4
FEXX
DMA_ADDR_EXT

https://github.com/msinger/dmg-schematics

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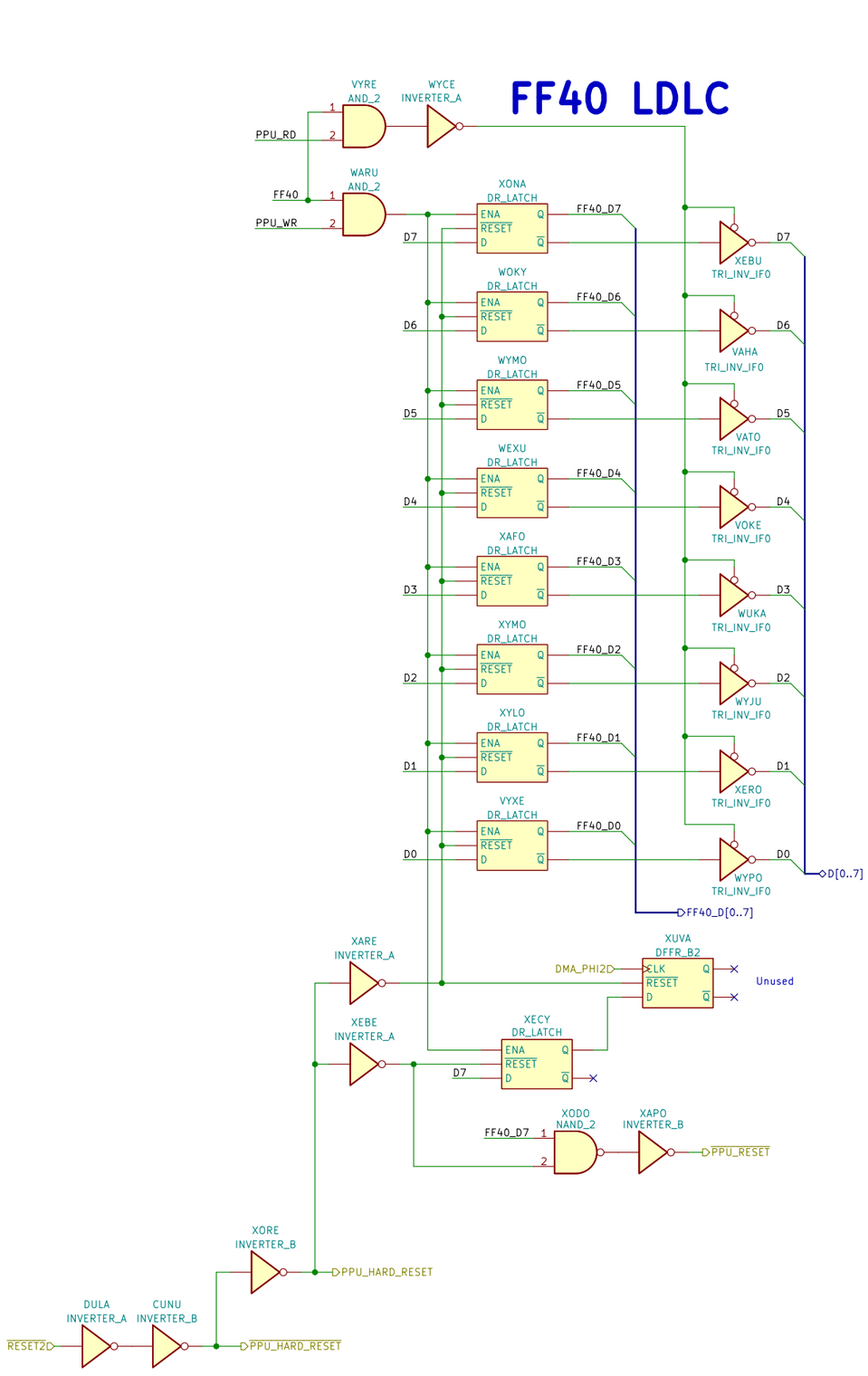
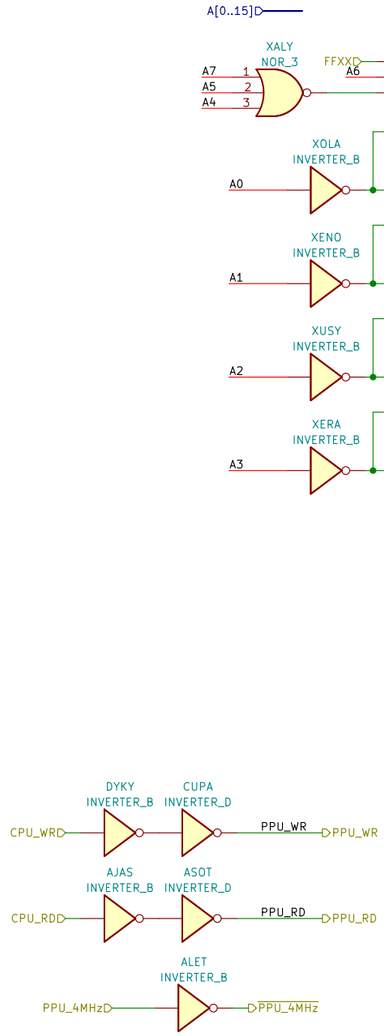
Sheet: /PPU/
File: ppu.kicad_sch

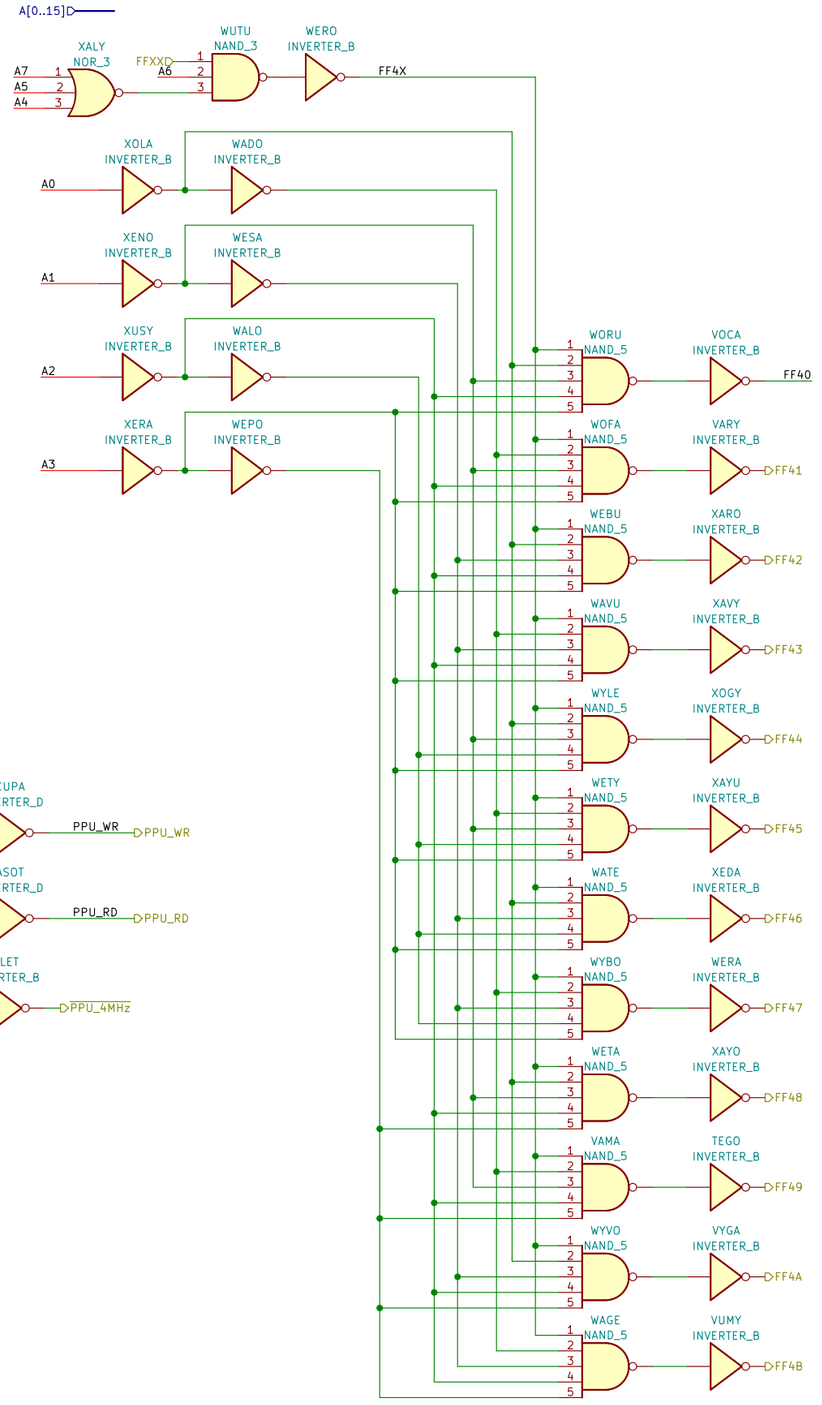
Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A.	kicad 6.0.6-3a73a75311~116~ubuntu22.04.1	Id: 24/45

FF40 LDLC







https://github.com/msinger/dmg-schematics

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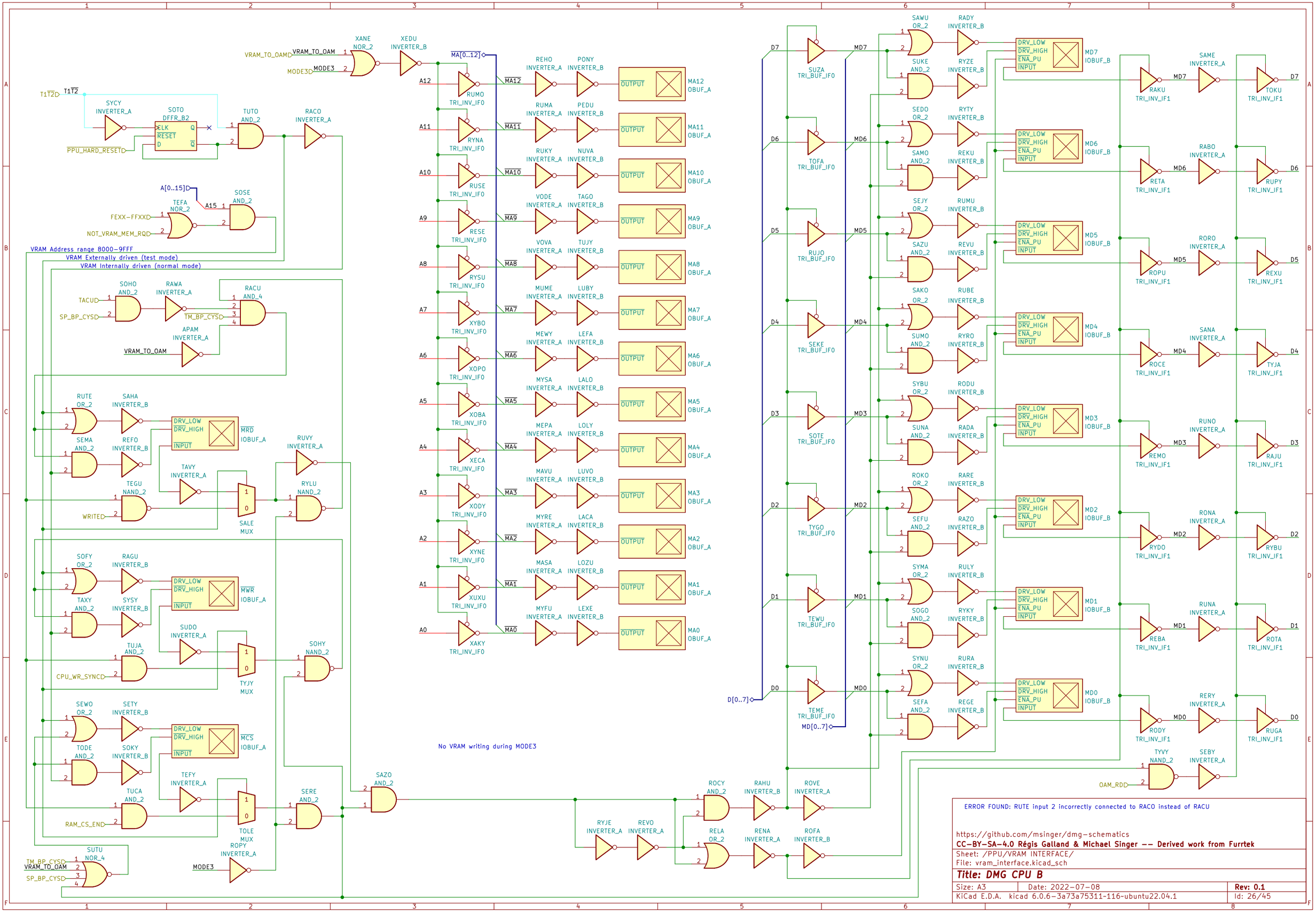
Sheet: /PPU/PPU DECODE & VIDEO CONTROL/
File: ppu_decode.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311~116~ubuntu22.04.1		Id: 25/45


T1T2
SYCY INVERTER_A
SOTO DFFR_B2
TUTO AND_2
RACO INVERTER_A
PPU_HARD_RESET
A[0..15]
TEFA NOR_2
A15
SOSE AND_2
FEXX-FFXX
NOT_VRAM_MEM_RQD
VRAM Address range 8000-9FFF
VRAM Externally driven (test mode)
VRAM Internally driven (normal mode)
SOHO AND_2
RAWA INVERTER_A
RACU AND_4
TACUD
SP_BP_CYSD
TM_BP_CYSD
APAM INVERTER_A
VRAM_TO_OAM
RUTE OR_2
SAHA INVERTER_B
SEMA AND_2
REFO INVERTER_B
DRV_LOW
DRV_HIGH
INPUT
MRD IOBUF_A
TAVY INVERTER_A
TEGU NAND_2
WRITED
SALE MUX
RUVY INVERTER_A
RYLU NAND_2
SOFY OR_2
RAGU INVERTER_B
TAXY AND_2
SYSY INVERTER_B
MWR IOBUF_A
SUDO INVERTER_A
TUJA AND_2
CPU_WR_SYNCD
TYJY MUX
SOHY NAND_2
SEWO OR_2
SETY INVERTER_B
TODE AND_2
SOKY INVERTER_B
MCS IOBUF_A
TEFY INVERTER_A
TUCA AND_2
RAM_CS_END
TOLE MUX
SERE AND_2
SUTU NOR_4
VRAM_TO_OAM
SP_BP_CYSD
TM_BP_CYSD
ROPY INVERTER_A
MODE3
XANE NOR_2
XEDU INVERTER_B
VRAM_TO_OAM
MODE3
MA[0..12]
A12
RUMO TRI_INV_IF0
A11
RYNA TRI_INV_IF0
A10
RUSE TRI_INV_IF0
A9
RESE TRI_INV_IF0
A8
RYSU TRI_INV_IF0
A7
XYBO TRI_INV_IF0
A6
XOPO TRI_INV_IF0
A5
XOBA TRI_INV_IF0
A4
XECA TRI_INV_IF0
A3
XODY TRI_INV_IF0
A2
XYNE TRI_INV_IF0
A1
XUXU TRI_INV_IF0
A0
XAKY TRI_INV_IF0
REHO INVERTER_A
PONY INVERTER_B
RUMA INVERTER_A
PEDU INVERTER_B
RUKY INVERTER_A
NUVA INVERTER_B
VODE INVERTER_A
TAGO INVERTER_B
VOVA INVERTER_A
TUJY INVERTER_B
MUME INVERTER_A
LUBY INVERTER_B
MEWY INVERTER_A
LEFA INVERTER_B
MYSA INVERTER_A
LALO INVERTER_B
MEPA INVERTER_A
LOLY INVERTER_B
MAVU INVERTER_A
LUVO INVERTER_B
MYRE INVERTER_A
LACA INVERTER_B
MASA INVERTER_A
LOZU INVERTER_B
MYFU INVERTER_A
LEXE INVERTER_B
OUTPUT
MA12 OBUF_A
MA11 OBUF_A
MA10 OBUF_A
MA9 OBUF_A
MA8 OBUF_A
MA7 OBUF_A
MA6 OBUF_A
MA5 OBUF_A
MA4 OBUF_A
MA3 OBUF_A
MA2 OBUF_A
MA1 OBUF_A
MA0 OBUF_A
No VRAM writing during MODE3
SAZO AND_2
RYJE INVERTER_A
REVO INVERTER_A
ROCY AND_2
RAHU INVERTER_B
ROVE INVERTER_A
RELA OR_2
RENA INVERTER_A
ROFA INVERTER_B
D7
SUZA TRI_BUF_IF0
D6
TOFA TRI_BUF_IF0
D5
RUJO TRI_BUF_IF0
D4
SEKE TRI_BUF_IF0
D3
SOTE TRI_BUF_IF0
D2
TYGO TRI_BUF_IF0
D1
TEWU TRI_BUF_IF0
D0
TEME TRI_BUF_IF0
D[0..7]
MD[0..7]
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
SAWU OR_2
RADY INVERTER_B
SUKE AND_2
RYZE INVERTER_B
SEDO OR_2
RYTY INVERTER_B
SAMO AND_2
REKU INVERTER_B
SEJY OR_2
RUMU INVERTER_B
SAZU AND_2
REVU INVERTER_B
SAKO OR_2
RUBE INVERTER_B
SUMO AND_2
RYRO INVERTER_B
SYBU OR_2
RODU INVERTER_B
SUNA AND_2
RADA INVERTER_B
ROKO OR_2
RARE INVERTER_B
SEFU AND_2
RAZO INVERTER_B
SYMA OR_2
RULY INVERTER_B
SOGO AND_2
RYKY INVERTER_B
SYNU OR_2
RURA INVERTER_B
SEFA AND_2
REGE INVERTER_B
MD7 IOBUF_B
MD6 IOBUF_B
MD5 IOBUF_B
MD4 IOBUF_B
MD3 IOBUF_B
MD2 IOBUF_B
MD1 IOBUF_B
MD0 IOBUF_B
RAKU TRI_INV_IF1
RETA TRI_INV_IF1
ROPU TRI_INV_IF1
ROCE TRI_INV_IF1
REMO TRI_INV_IF1
RYDO TRI_INV_IF1
REBA TRI_INV_IF1
RODY TRI_INV_IF1
SAME INVERTER_A
RABO INVERTER_A
RORO INVERTER_A
SANA INVERTER_A
RUNO INVERTER_A
RONA INVERTER_A
RUNA INVERTER_A
RERY INVERTER_A
TOKU TRI_INV_IF1
RUPY TRI_INV_IF1
REXU TRI_INV_IF1
TYJA TRI_INV_IF1
RAJU TRI_INV_IF1
RYBU TRI_INV_IF1
ROTA TRI_INV_IF1
RUGA TRI_INV_IF1
TYVY NAND_2
SEBY INVERTER_A
OAM_RDD
ERROR FOUND: RUTE input 2 incorrectly connected to RACO instead of RACU
https://github.com/msinger/dmg-schematics
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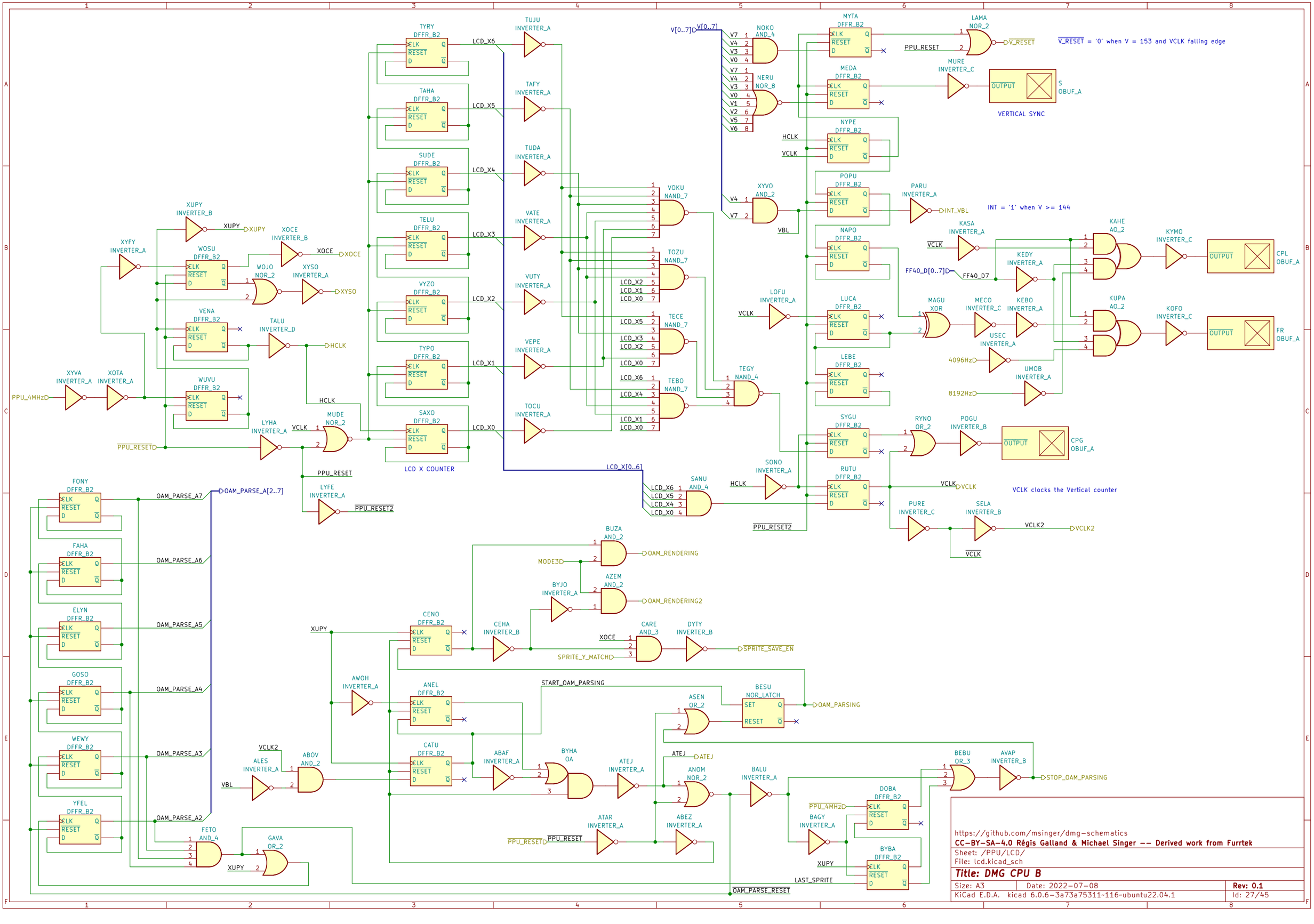
Sheet: /PPU/VRAM INTERFACE/
File: vram_interface.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 26/45


TYRY DFFR_B2
TUJU INVERTER_A
LCD_X6
TAHA DFFR_B2
TAFY INVERTER_A
LCD_X5
SUDE DFFR_B2
TUDA INVERTER_A
LCD_X4
TELU DFFR_B2
VATE INVERTER_A
LCD_X3
VYZO DFFR_B2
VUTY INVERTER_A
LCD_X2
TYPO DFFR_B2
VEPE INVERTER_A
LCD_X1
SAXO DFFR_B2
TOCU INVERTER_A
LCD_X0
LCD X COUNTER
LCD_X[0..6]
V[0..7]
NOKO AND_4
NERU NOR_8
MYTA DFFR_B2
MEDA DFFR_B2
NYPE DFFR_B2
POPU DFFR_B2
NAPO DFFR_B2
LUCA DFFR_B2
LEBE DFFR_B2
SYGU DFFR_B2
RUTU DFFR_B2
LAMA NOR_2
PPU_RESET
V_RESET
V_RESET = '0' when V = 153 and VCLK falling edge
MURE INVERTER_C
OUTPUT
S OBUF_A
VERTICAL SYNC
HCLK
VCLK
XYVO AND_2
VBL
PARU INVERTER_A
INT_VBL
INT = '1' when V >= 144
KASA INVERTER_A
KAHE AO_2
KYMO INVERTER_C
CPL OBUF_A
FF40_D[0..7]
FF40_D7
KEDY INVERTER_A
LOFU INVERTER_A
MAGU XOR
MECO INVERTER_C
KEBO INVERTER_A
KUPA AO_2
KOFO INVERTER_C
FR OBUF_A
USEC INVERTER_A
4096Hz
8192Hz
UMOB INVERTER_A
TEGY NAND_4
VOKU NAND_7
TOZU NAND_7
TECE NAND_7
TEBO NAND_7
SONO INVERTER_A
SANU AND_4
RYNO OR_2
POGU INVERTER_B
CPG OBUF_A
PURE INVERTER_C
SELA INVERTER_B
VCLK2
VCLK clocks the Vertical counter
XUPY INVERTER_B
XUPY
XOCE INVERTER_B
XOCE
XYFY INVERTER_A
WOSU DFFR_B2
WOJO NOR_2
XYSO INVERTER_A
XYSO
VENA DFFR_B2
TALU INVERTER_D
HCLK
XYVA INVERTER_A
XOTA INVERTER_A
PPU_4MHz
WUVU DFFR_B2
LYHA INVERTER_A
MUDE NOR_2
PPU_RESET
LYFE INVERTER_A
PPU_RESET2
FONY DFFR_B2
FAHA DFFR_B2
ELYN DFFR_B2
GOSO DFFR_B2
WEWY DFFR_B2
YFEL DFFR_B2
OAM_PARSE_A7
OAM_PARSE_A6
OAM_PARSE_A5
OAM_PARSE_A4
OAM_PARSE_A3
OAM_PARSE_A2
OAM_PARSE_A[2..7]
FETO AND_4
GAVA OR_2
BUZA AND_2
MODE3
OAM_RENDERING
AZEM AND_2
BYJO INVERTER_A
OAM_RENDERING2
CENO DFFR_B2
CEHA INVERTER_B
CARE AND_3
DYTY INVERTER_B
SPRITE_Y_MATCH
SPRITE_SAVE_EN
AWOH INVERTER_A
ANEL DFFR_B2
CATU DFFR_B2
START_OAM_PARSING
BESU NOR_LATCH
SET
RESET
OAM_PARSING
ASEN OR_2
ALES INVERTER_A
ABOV AND_2
ABAF INVERTER_A
BYHA OA
ATEJ INVERTER_A
ANOM NOR_2
BALU INVERTER_A
BEBU OR_3
AVAP INVERTER_B
STOP_OAM_PARSING
ATAR INVERTER_A
ABEZ INVERTER_A
BAGY INVERTER_A
DOBA DFFR_B2
BYBA DFFR_B2
LAST_SPRITE
OAM_PARSE_RESET
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /PPU/LCD/
File: lcd.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 27/45

FF44 LY

FF41 STAT

FF41: WR = PPU INT ENABLE, RD = PPU INT ENABLE + PPU INT
Glitch when writing to this register — All interrupts are enabled before data settles.

FF45 LYC

When all interrupts are enabled,
INT_STAT = '1' when LY = LYC (whole line), VBLANK (MODE1), HBLANK (MODE0),
and Only for a few cycles at the start of OAM parsing when VCLK is high.

STOP MODE3 when H = 167 and no more sprites to fetch

BG/WIN X COUNTER

Y COUNTER

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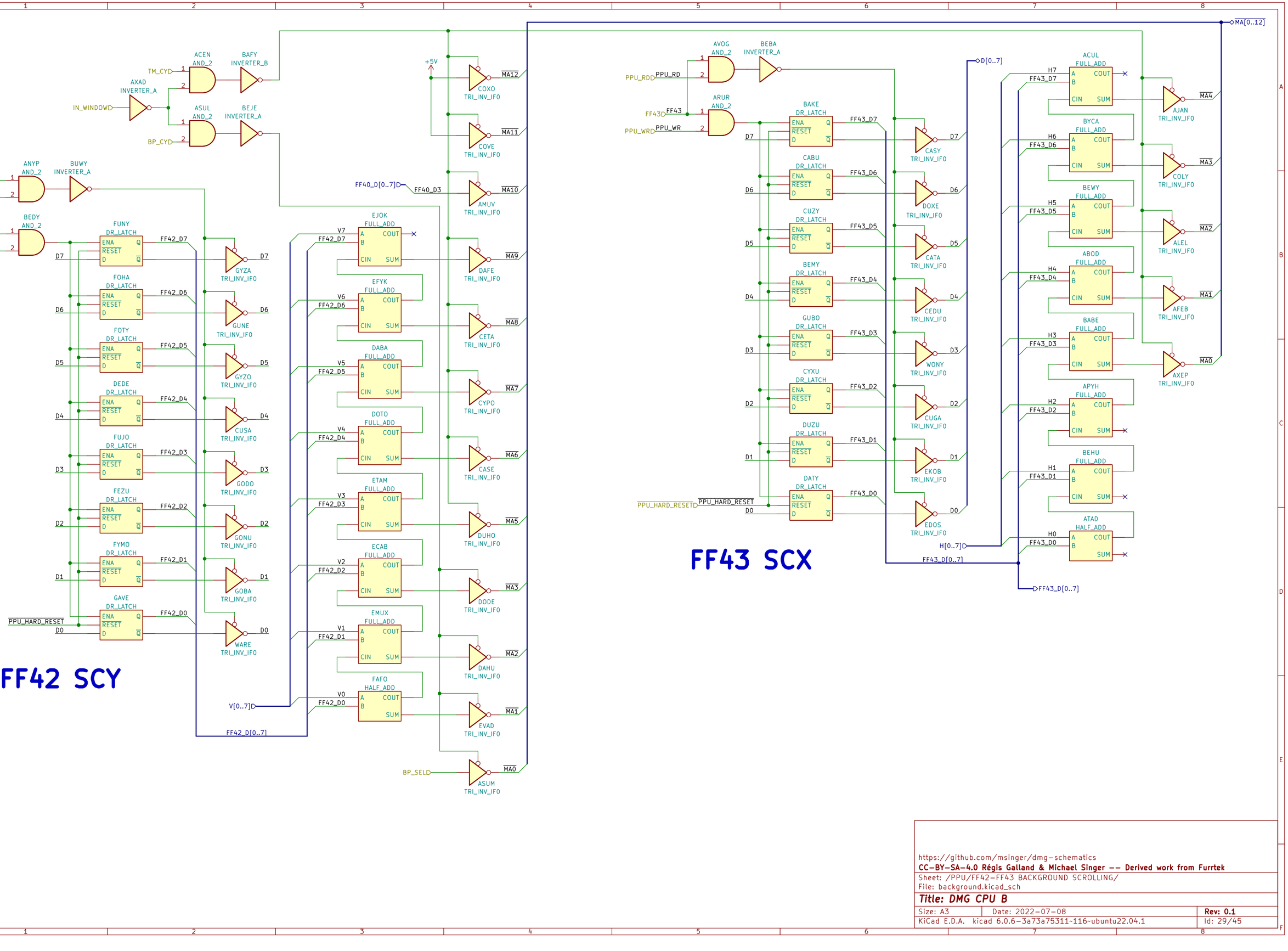
Sheet: /PPU/FF41 STAT, FF44 LY & FF45 LYC/
File: ff41_stat.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 28/45


MA[0..12]
D[0..7]
ACEN
AND_2
BAFY
INVERTER_B
TM_CYD
AXAD
INVERTER_A
IN_WINDOWD
ASUL
AND_2
BEJE
INVERTER_A
BP_CYD
+5V
COXO
TRI_INV_IF0
MA12
COVE
TRI_INV_IF0
MA11
AMUV
TRI_INV_IF0
MA10
FF40_D[0..7]
FF40_D3
ANYP
AND_2
BUWY
INVERTER_A
PPU_RD
BEDY
AND_2
PPU_WR
FF42D
FF42
FUNY
DR_LATCH
FOHA
DR_LATCH
FOTY
DR_LATCH
DEDE
DR_LATCH
FUJO
DR_LATCH
FEZU
DR_LATCH
FYMO
DR_LATCH
GAVE
DR_LATCH
FF42_D7
FF42_D6
FF42_D5
FF42_D4
FF42_D3
FF42_D2
FF42_D1
FF42_D0
D7
D6
D5
D4
D3
D2
D1
D0
GYZA
TRI_INV_IF0
GUNE
TRI_INV_IF0
GYZO
TRI_INV_IF0
CUSA
TRI_INV_IF0
GODO
TRI_INV_IF0
GONU
TRI_INV_IF0
GOBA
TRI_INV_IF0
WARE
TRI_INV_IF0
PPU_HARD_RESET
V[0..7]
FF42_D[0..7]
EJOK
FULL_ADD
EFYK
FULL_ADD
DABA
FULL_ADD
DOTO
FULL_ADD
ETAM
FULL_ADD
ECAB
FULL_ADD
EMUX
FULL_ADD
FAFO
HALF_ADD
V7
V6
V5
V4
V3
V2
V1
V0
DAFE
TRI_INV_IF0
MA9
CETA
TRI_INV_IF0
MA8
CYPO
TRI_INV_IF0
MA7
CASE
TRI_INV_IF0
MA6
DUHO
TRI_INV_IF0
MA5
DODE
TRI_INV_IF0
MA3
DAHU
TRI_INV_IF0
MA2
EVAD
TRI_INV_IF0
MA1
ASUM
TRI_INV_IF0
MA0
BP_SELD
FF42 SCY
AVOG
AND_2
BEBA
INVERTER_A
PPU_RDD
ARUR
AND_2
FF43D
PPU_WRD
BAKE
DR_LATCH
CABU
DR_LATCH
CUZY
DR_LATCH
BEMY
DR_LATCH
GUBO
DR_LATCH
CYXU
DR_LATCH
DUZU
DR_LATCH
DATY
DR_LATCH
FF43_D7
FF43_D6
FF43_D5
FF43_D4
FF43_D3
FF43_D2
FF43_D1
FF43_D0
CASY
TRI_INV_IF0
DOXE
TRI_INV_IF0
CATA
TRI_INV_IF0
CEDU
TRI_INV_IF0
WONY
TRI_INV_IF0
CUGA
TRI_INV_IF0
EKOB
TRI_INV_IF0
EDOS
TRI_INV_IF0
H[0..7]
FF43_D[0..7]
ACUL
FULL_ADD
BYCA
FULL_ADD
BEWY
FULL_ADD
ABOD
FULL_ADD
BABE
FULL_ADD
APYH
FULL_ADD
BEHU
FULL_ADD
ATAD
HALF_ADD
H7
H6
H5
H4
H3
H2
H1
H0
AJAN
TRI_INV_IF0
COLY
TRI_INV_IF0
ALEL
TRI_INV_IF0
AFEB
TRI_INV_IF0
AXEP
TRI_INV_IF0
MA4
MA3
MA2
MA1
MA0
FF43 SCX
https://github.com/msinger/dmg-schematics
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Sheet: /PPU/FF42-FF43 BACKGROUND SCROLLING/
File: background.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 29/45

FF4A WY

FF4B WX

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Sheet: /PPU/FF4A-FF4B WINDOW DETECTION/

File: win_detect.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 30/45

BG/WIN Cycle counter

TAVE resets the cycle counter at cycle 5 only once at the start of a new rendering line.
PORY will reset the counter when Window has started at cycle 5 too.
ROZE will reset the counter at cycle 7 in other cases.

HORIZONTAL SYNC

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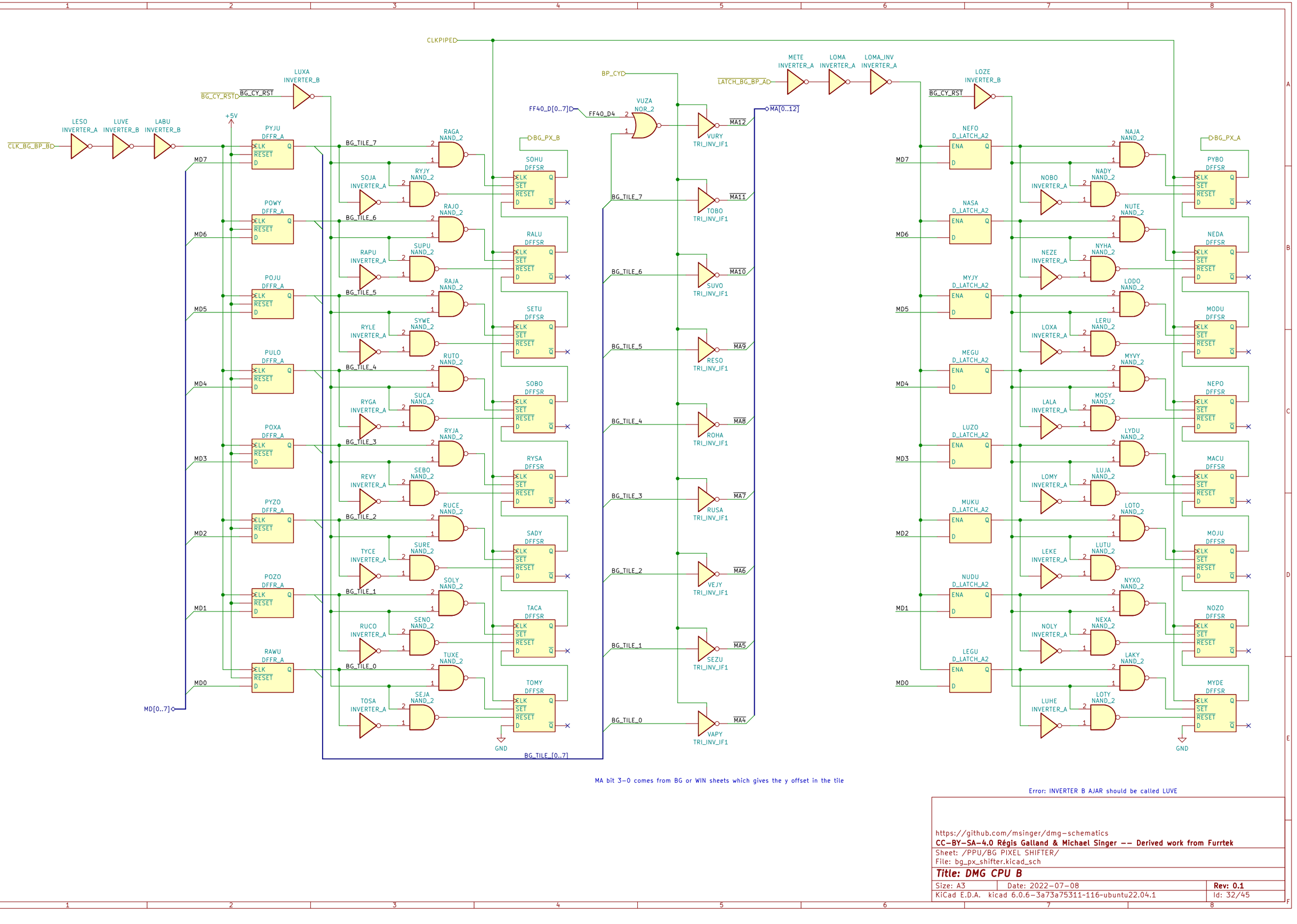
Sheet: /PPU/BG & WIN CYCLES/
File: bg_win_cycles.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 31/45



MA bit 3-0 comes from BG or WIN sheets which gives the y offset in the tile

Error: INVERTER B AJAR should be called LUVE

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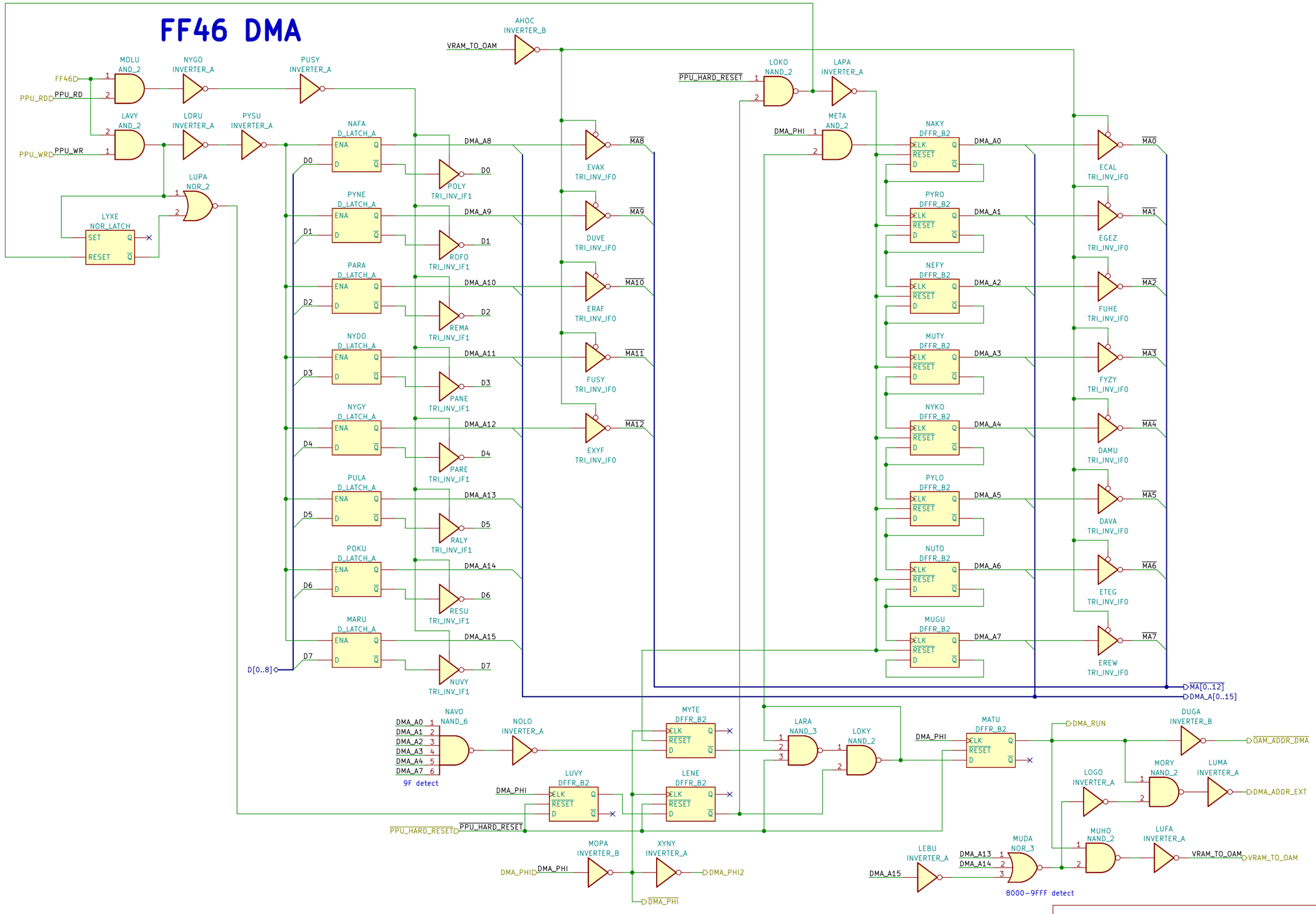
Sheet: /PPU/BG PIXEL SHIFTER/
File: bg_px_shifter.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 32/45

FF46 DMA



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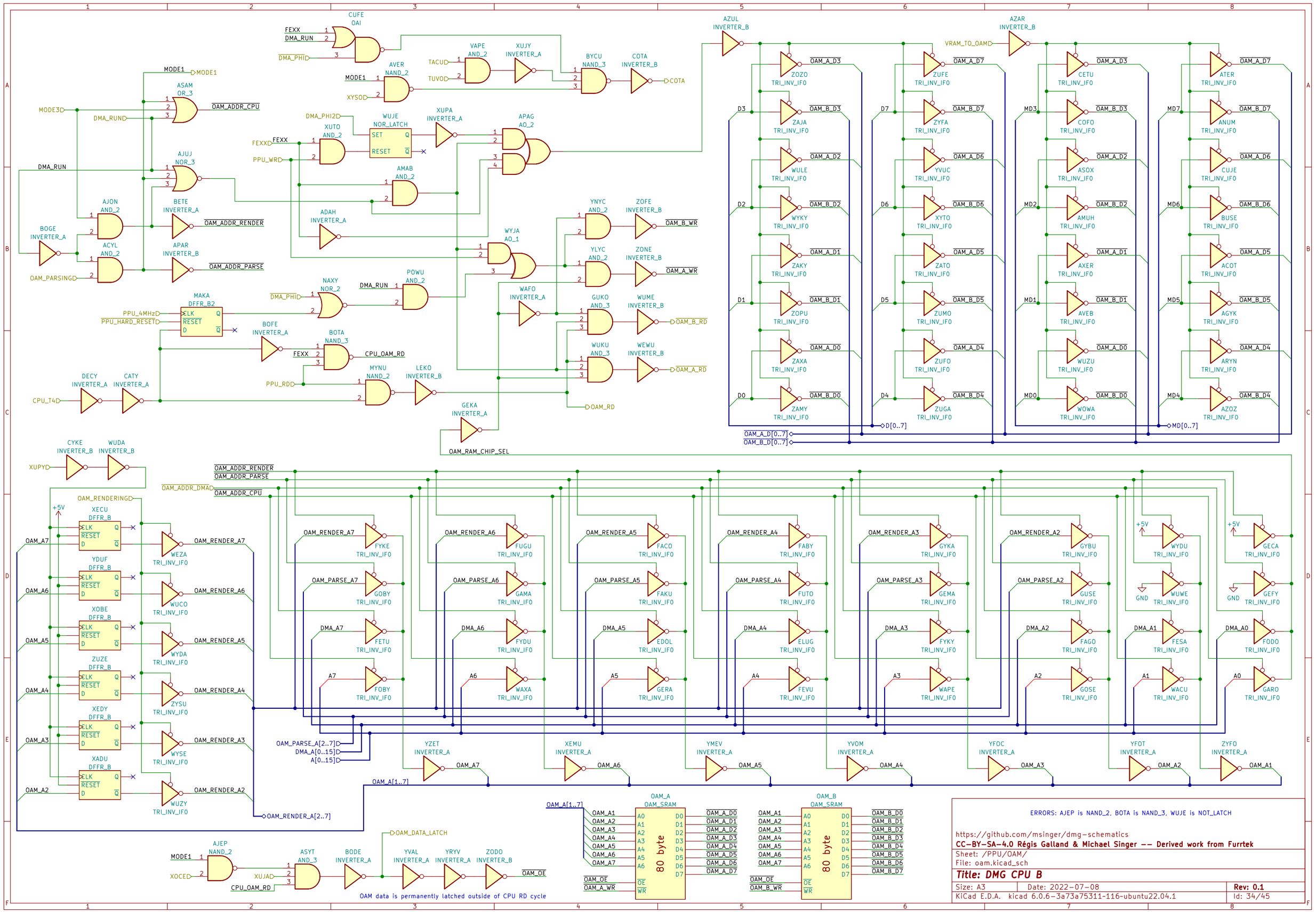
Sheet: /PPU/FF46 DMA/		
File: ff46_dma.kicad_sch		
Title: DMG CPU B		
Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 33/45


CUFE OAI
FEXX
DMA_RUN
DMA_PHI
VAPE AND_2
TACU
TUVO
XUJY INVERTER_A
BYCU NAND_3
COTA INVERTER_B
COTA
AVER NAND_2
MODE1
XYSO
AZUL INVERTER_B
AZAR INVERTER_B
VRAM_TO_OAM
MODE1
ASAM OR_3
MODE3
DMA_RUN
OAM_ADDR_CPU
DMA_PHI2
WUJE NOR_LATCH
SET
RESET
XUPA INVERTER_A
APAG AO_2
XUTO AND_2
FEXXD
PPU_WR
AMAB AND_2
AJUJ NOR_3
ADAH INVERTER_A
AJON AND_2
BETE INVERTER_A
OAM_ADDR_RENDER
BOGE INVERTER_A
ACYL AND_2
APAR INVERTER_B
OAM_ADDR_PARSE
OAM_PARSING
WYJA AO_1
YNYC AND_2
ZOFE INVERTER_B
OAM_B_WR
YLYC AND_2
ZONE INVERTER_B
OAM_A_WR
NAXY NOR_2
POWU AND_2
MAKA DFFR_B2
CLK
RESET
D
PPU_4MHz
PPU_HARD_RESET
WAFO INVERTER_A
GUKO AND_3
WUME INVERTER_B
OAM_B_RD
BOFE INVERTER_A
BOTA NAND_3
CPU_OAM_RD
WUKU AND_3
WEWU INVERTER_B
OAM_A_RD
DECY INVERTER_A
CATY INVERTER_A
CPU_T4
MYNU NAND_2
LEKO INVERTER_B
OAM_RD
GEKA INVERTER_A
OAM_RAM_CHIP_SEL
ZOZO TRI_INV_IF0
ZAJA TRI_INV_IF0
WULE TRI_INV_IF0
WYKY TRI_INV_IF0
ZAKY TRI_INV_IF0
ZOPU TRI_INV_IF0
ZAXA TRI_INV_IF0
ZAMY TRI_INV_IF0
ZUFE TRI_INV_IF0
ZYFA TRI_INV_IF0
YVUC TRI_INV_IF0
XYTO TRI_INV_IF0
ZATO TRI_INV_IF0
ZUMO TRI_INV_IF0
ZUFO TRI_INV_IF0
ZUGA TRI_INV_IF0
CETU TRI_INV_IF0
COFO TRI_INV_IF0
ASOX TRI_INV_IF0
AMUH TRI_INV_IF0
AXER TRI_INV_IF0
AVEB TRI_INV_IF0
WUZU TRI_INV_IF0
WOWA TRI_INV_IF0
ATER TRI_INV_IF0
ANUM TRI_INV_IF0
CUJE TRI_INV_IF0
BUSE TRI_INV_IF0
ACOT TRI_INV_IF0
AGYK TRI_INV_IF0
ARYN TRI_INV_IF0
AZOZ TRI_INV_IF0
D[0..7]
MD[0..7]
OAM_A_D[0..7]
OAM_B_D[0..7]
CYKE INVERTER_B
WUDA INVERTER_B
XUPY
OAM_RENDERING
OAM_ADDR_RENDER
OAM_ADDR_PARSE
OAM_ADDR_DMA
OAM_ADDR_CPU
+5V
XECU DFFR_B
YDUF DFFR_B
XOBE DFFR_B
ZUZE DFFR_B
XEDY DFFR_B
XADU DFFR_B
OAM_A7
OAM_A6
OAM_A5
OAM_A4
OAM_A3
OAM_A2
WEZA TRI_INV_IF0
WUCO TRI_INV_IF0
WYDA TRI_INV_IF0
ZYSU TRI_INV_IF0
WYSE TRI_INV_IF0
WUZY TRI_INV_IF0
OAM_RENDER_A7
OAM_RENDER_A6
OAM_RENDER_A5
OAM_RENDER_A4
OAM_RENDER_A3
OAM_RENDER_A2
OAM_RENDER_A[2..7]
OAM_RENDER_A7 FYKE TRI_INV_IF0
OAM_PARSE_A7 GOBY TRI_INV_IF0
DMA_A7 FETU TRI_INV_IF0
A7 FOBY TRI_INV_IF0
OAM_RENDER_A6 FUGU TRI_INV_IF0
OAM_PARSE_A6 GAMA TRI_INV_IF0
DMA_A6 FYDU TRI_INV_IF0
A6 WAXA TRI_INV_IF0
OAM_RENDER_A5 FACO TRI_INV_IF0
OAM_PARSE_A5 FAKU TRI_INV_IF0
DMA_A5 EDOL TRI_INV_IF0
A5 GERA TRI_INV_IF0
OAM_RENDER_A4 FABY TRI_INV_IF0
OAM_PARSE_A4 FUTO TRI_INV_IF0
DMA_A4 ELUG TRI_INV_IF0
A4 FEVU TRI_INV_IF0
OAM_RENDER_A3 GYKA TRI_INV_IF0
OAM_PARSE_A3 GEMA TRI_INV_IF0
DMA_A3 FYKY TRI_INV_IF0
A3 WAPE TRI_INV_IF0
OAM_RENDER_A2 GYBU TRI_INV_IF0
OAM_PARSE_A2 GUSE TRI_INV_IF0
DMA_A2 FAGO TRI_INV_IF0
A2 GOSE TRI_INV_IF0
WYDU TRI_INV_IF0
WUWE TRI_INV_IF0
DMA_A1 FESA TRI_INV_IF0
A1 WACU TRI_INV_IF0
GECA TRI_INV_IF0
GEFY TRI_INV_IF0
DMA_A0 FODO TRI_INV_IF0
A0 GARO TRI_INV_IF0
GND
OAM_PARSE_A[2..7]
DMA_A[0..15]
A[0..15]
YZET INVERTER_A
XEMU INVERTER_A
YMEV INVERTER_A
YVOM INVERTER_A
YFOC INVERTER_A
YFOT INVERTER_A
ZYFO INVERTER_A
OAM_A7
OAM_A6
OAM_A5
OAM_A4
OAM_A3
OAM_A2
OAM_A1
OAM_A[1..7]
OAM_A
OAM_SRAM
80 byte
A0
A1
A2
A3
A4
A5
A6
A7
OE
WR
D0
D1
D2
D3
D4
D5
D6
D7
OAM_A_D0
OAM_A_D1
OAM_A_D2
OAM_A_D3
OAM_A_D4
OAM_A_D5
OAM_A_D6
OAM_A_D7
OAM_OE
OAM_A_WR
OAM_B
OAM_B_WR
OAM_B_D0
OAM_B_D1
OAM_B_D2
OAM_B_D3
OAM_B_D4
OAM_B_D5
OAM_B_D6
OAM_B_D7
AJEP NAND_2
MODE1
XOCE
ASYT AND_3
XUJA
CPU_OAM_RD
BODE INVERTER_A
OAM_DATA_LATCH
YVAL INVERTER_A
YRYV INVERTER_A
ZODO INVERTER_B
OAM_OE
OAM data is permanently latched outside of CPU RD cycle
ERRORS: AJEP is NAND_2, BOTA is NAND_3, WUJE is NOT_LATCH
https://github.com/msinger/dmg-schematics
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Sheet: /PPU/OAM/
File: oam.kicad_sch
Title: DMG CPU B
Size: A3
Date: 2022-07-08
Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1
Id: 34/45

OAM B D[0..7] gives the sprite Y position during parsing and will determine if the sprite appears on the current line.
If it does, D[0..3] gets stored to define the offset in the sprite char.
During rendering, it will contain the Tile address which be used to fecth sprite char data in VRAM.

VONU is 2 CLK5 cycles behind TULY. Sprite bit plane fetching takes 8 cycles during which
TULY = '1' during cycle 2 and 3 and VONU = '1' during cycle 4 and 5.

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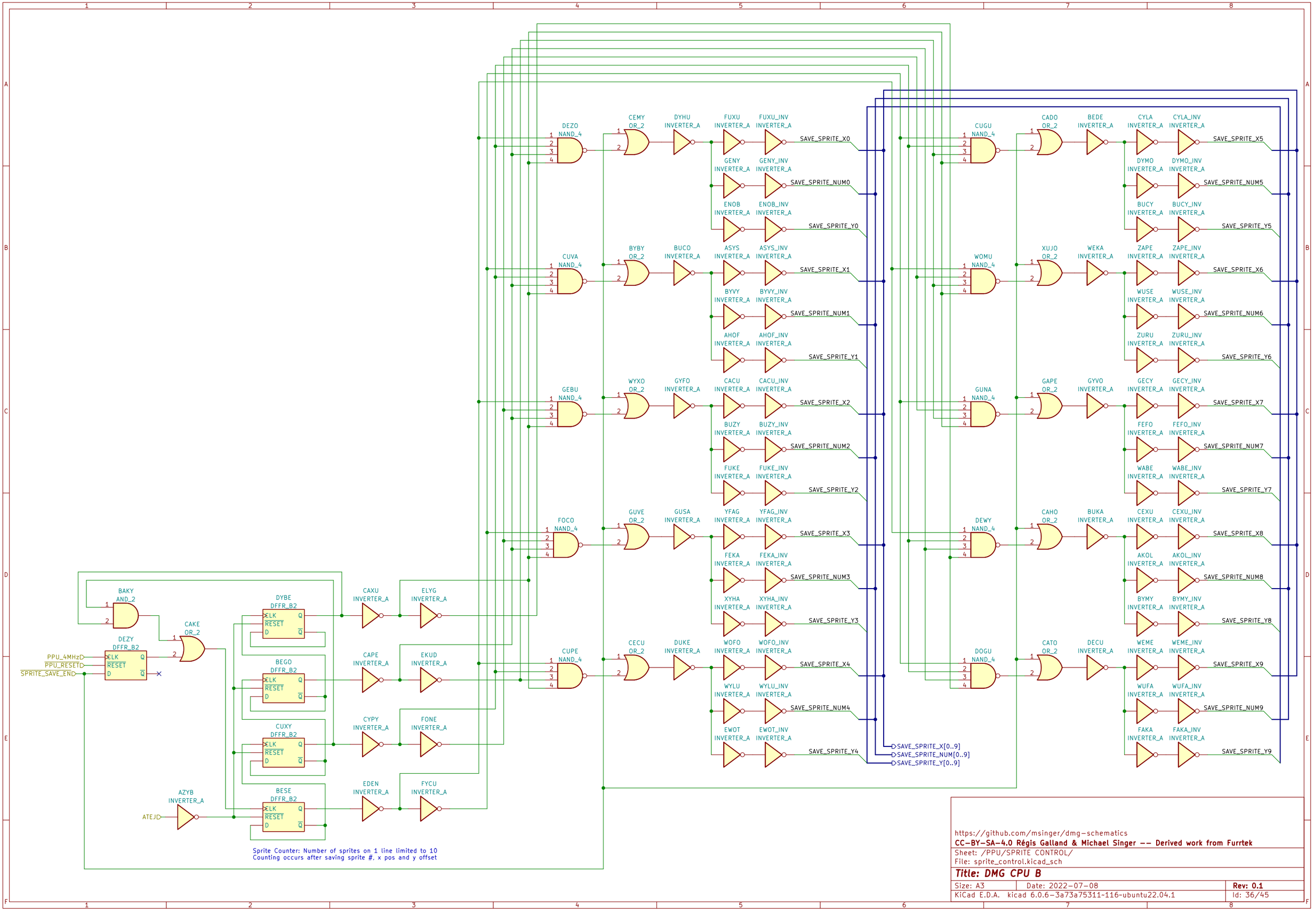
Sheet: /PPU/SPRITE Y COMPARATOR/
File: sprite_y_comparator.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 35/45



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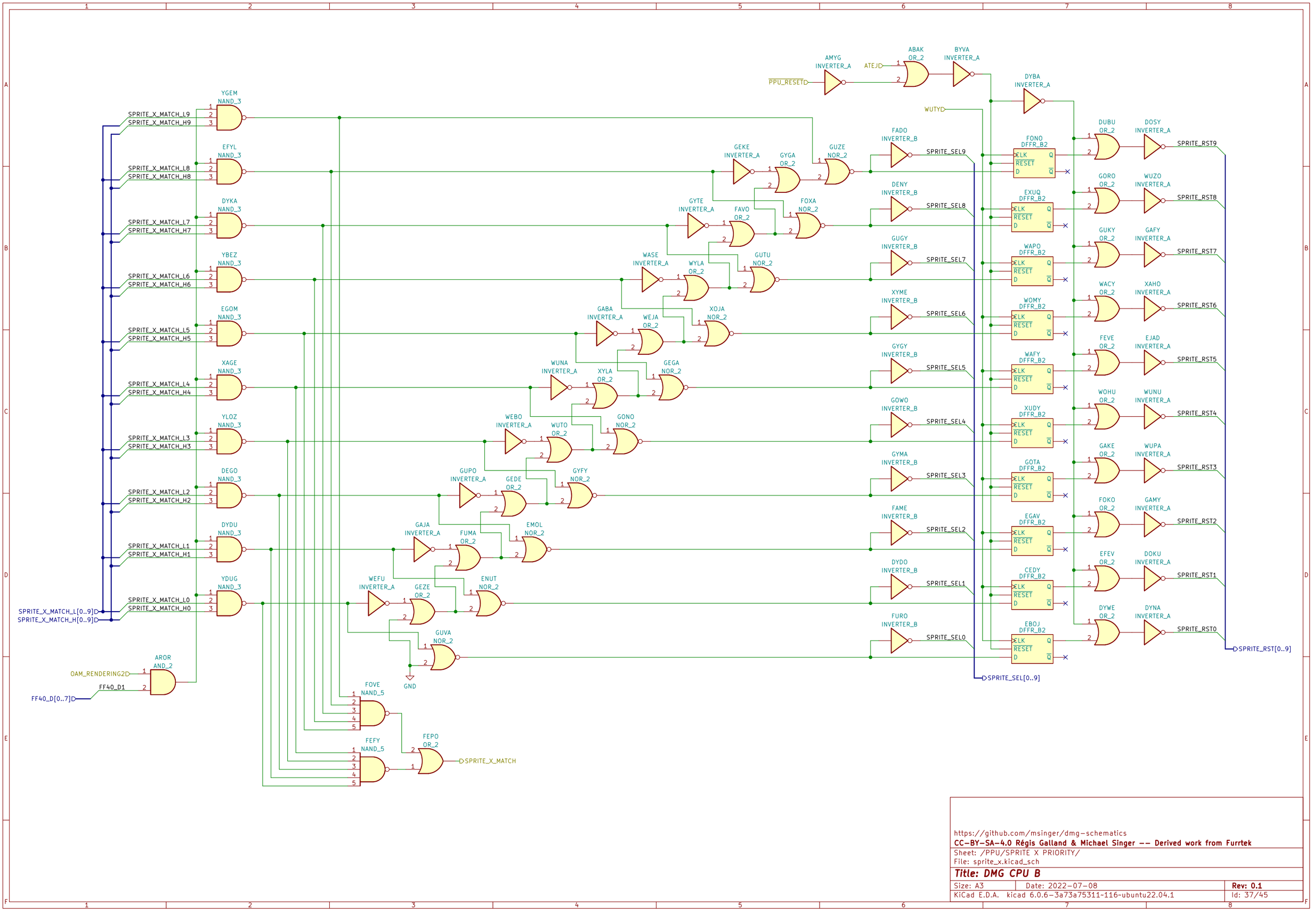
Sheet: /PPU/SPRITE CONTROL/

File: sprite_control.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 36/45



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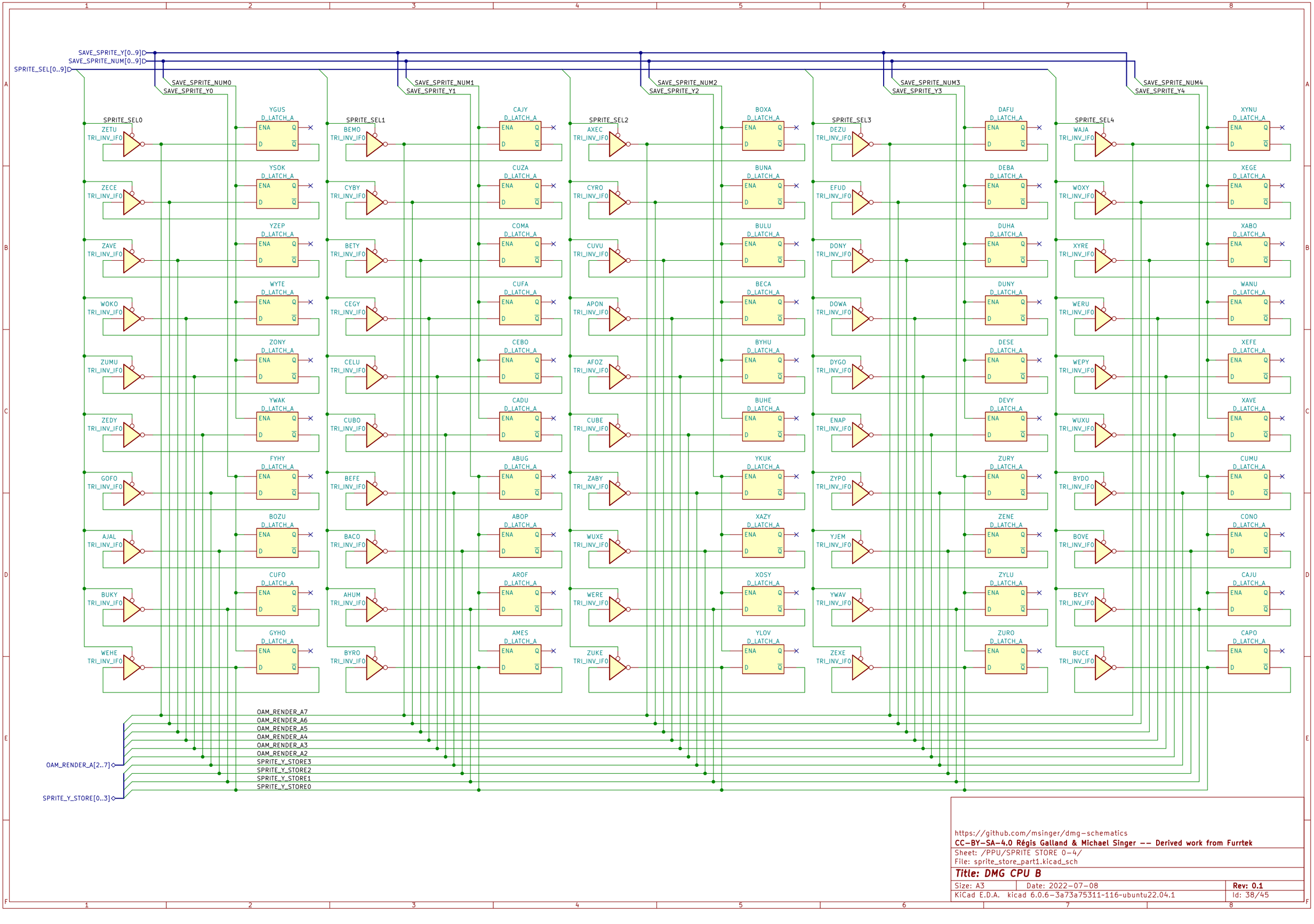
Sheet: /PPU/SPRITE X PRIORITY/
File: sprite_x.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1		Id: 37/45



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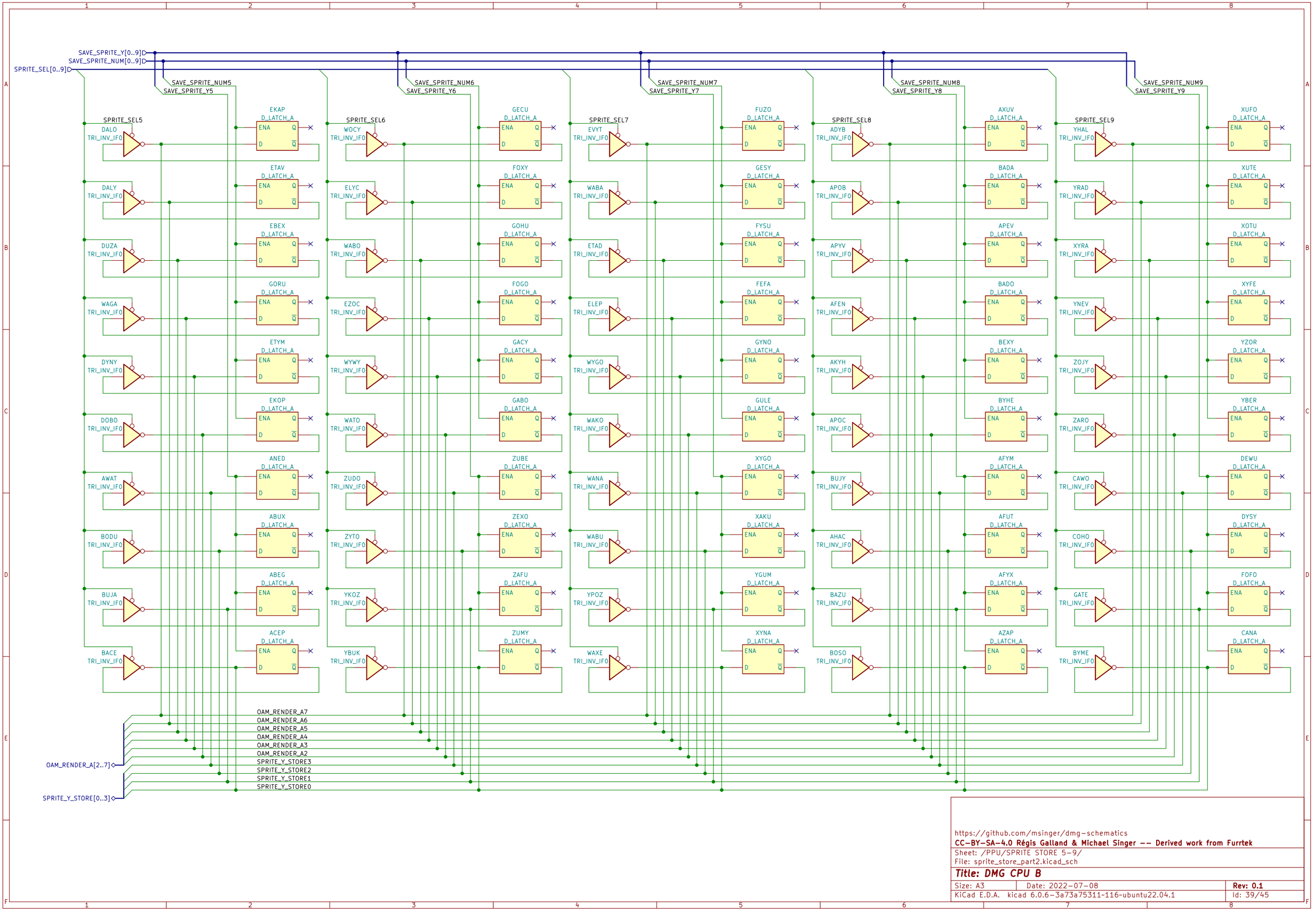
Sheet: /PPU/SPRITE STORE 0-4/
File: sprite_store_part1.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 38/45



https://github.com/msinger/dmg-schematics

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Sheet: /PPU/SPRITE STORE 5-9/
File: sprite_store_part2.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 39/45

SAVE_SPRITE_X0
SPRITE_RST0
WELO DR_LATCH
XUNY DR_LATCH
WOTE DR_LATCH
XAKO DR_LATCH
XEPE DR_LATCH
YLAH DR_LATCH
ZOLA DR_LATCH
ZULU DR_LATCH
WOJU XOR
YFUN XOR
WYZA XOR
YPUK XOR
ZOGY XOR
ZEBA XOR
ZAHA XOR
ZOKY XOR
XEBA NOR_4
ZAKO NOR_4
SPRITE_X_MATCH_H0
SPRITE_X_MATCH_L0
SAVE_SPRITE_X1
SPRITE_RST1
DAKE DR_LATCH
CESO DR_LATCH
DYFU DR_LATCH
CUSY DR_LATCH
DANY DR_LATCH
DUKO DR_LATCH
DESU DR_LATCH
DAZO DR_LATCH
COLA XOR
BOBA XOR
COLU XOR
BAHU XOR
EDYM XOR
EMYB XOR
EBEF XOR
EWOK XOR
CYVY NOR_4
EWAM NOR_4
SPRITE_X_MATCH_H1
SPRITE_X_MATCH_L1
SAVE_SPRITE_X2
SPRITE_RST2
DUHY DR_LATCH
EJUF DR_LATCH
ENOR DR_LATCH
DEPY DR_LATCH
FOKA DR_LATCH
FYTY DR_LATCH
FUBY DR_LATCH
GOXU DR_LATCH
CEKO XOR
DETY XOR
DOZO XOR
CONY XOR
FUZU XOR
FESO XOR
FOKY XOR
FYVA XOR
CEHU NOR_4
EKES NOR_4
SPRITE_X_MATCH_H2
SPRITE_X_MATCH_L2
SPRITE_X[0..7]
H[0..7]
SAVE_SPRITE_X[0..9]
SPRITE_RST[0..9]
SAVE_SPRITE_X3
SPRITE_RST3
XOMY DR_LATCH
WUHA DR_LATCH
WYNA DR_LATCH
WECO DR_LATCH
XOLY DR_LATCH
XYBA DR_LATCH
XABE DR_LATCH
XEKA DR_LATCH
YVAP XOR
XENY XOR
XAVU XOR
XEVA XOR
YHOK XOR
YCAH XOR
YDAJ XOR
YVUZ XOR
YWOS NOR_4
ZURE NOR_4
SPRITE_X_MATCH_H3
SPRITE_X_MATCH_L3
SAVE_SPRITE_X4
SPRITE_RST4
YBED DR_LATCH
ZALA DR_LATCH
WYDE DR_LATCH
XEPA DR_LATCH
WEDU DR_LATCH
YGAJ DR_LATCH
ZYJO DR_LATCH
XURY DR_LATCH
ZYKU XOR
ZYPU XOR
XAHA XOR
ZEFE XOR
XEJU XOR
ZATE XOR
ZAKU XOR
YBOX XOR
YKOK NOR_4
YNAZ NOR_4
SPRITE_X_MATCH_H4
SPRITE_X_MATCH_L4
SPRITE_X_MATCH_H[0..9]
SPRITE_X_MATCH_L[0..9]

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Sheet: /PPU/SPRITE X MATCHERS 0-4/
File: sprite_x_matchers_part1.kicad_sch

Title: DMG CPU B

Size: A3 | Date: 2022-07-08 | **Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116-ubuntu22.04.1 | Id: 40/45

SAVE_SPRITE_X5
SPRITE_RST5
SAVE_SPRITE_X6
SPRITE_RST6
SAVE_SPRITE_X7
SPRITE_RST7
SAVE_SPRITE_X8
SPRITE_RST8
SAVE_SPRITE_X9
SPRITE_RST9
SAVE_SPRITE_X[0..9]
SPRITE_RST[0..9]
SPRITE_X[0..7]
H[0..7]
SPRITE_X_MATCH_H[0..9]
SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H5
SPRITE_X_MATCH_H6
SPRITE_X_MATCH_H7
SPRITE_X_MATCH_H8
SPRITE_X_MATCH_H9
SPRITE_X_MATCH_L5
SPRITE_X_MATCH_L6
SPRITE_X_MATCH_L7
SPRITE_X_MATCH_L8
SPRITE_X_MATCH_L9

CYWE DR_LATCH
DYBY DR_LATCH
DURY DR_LATCH
CUVY DR_LATCH
FUSA DR_LATCH
FAXA DR_LATCH
FOZY DR_LATCH
FESY DR_LATCH
BAZY XOR
CYLE XOR
CEVA XOR
BUMY XOR
GUZO XOR
GOLA XOR
GEVE XOR
GUDE XOR
COGY NOR_4
FYMA NOR_4

ZOLY DR_LATCH
ZOGO DR_LATCH
ZECU DR_LATCH
ZESA DR_LATCH
YCOL DR_LATCH
YRAC DR_LATCH
YMEM DR_LATCH
YVAG DR_LATCH
ZARE XOR
ZEMU XOR
ZYGO XOR
ZUZY XOR
XOSU XOR
ZUVU XOR
XUCO XOR
ZULO XOR
YWAP NOR_4
YDOT NOR_4

FAZU DR_LATCH
FAXE DR_LATCH
EXUK DR_LATCH
FEDE DR_LATCH
ERAZ DR_LATCH
EPUM DR_LATCH
EROL DR_LATCH
EHYN DR_LATCH
EJOT XOR
ESAJ XOR
DUCU XOR
EWUD XOR
DUSE XOR
DAGU XOR
DYZE XOR
DESO XOR
DAJE NOR_4
CYCO NOR_4

EZUF DR_LATCH
ENAD DR_LATCH
EBOW DR_LATCH
FYCA DR_LATCH
GAVY DR_LATCH
GYPU DR_LATCH
GADY DR_LATCH
GAZA DR_LATCH
DUZE XOR
DAGA XOR
DAWU XOR
EJAW XOR
GOHO XOR
GASU XOR
GABU XOR
GAFE XOR
DAMA NOR_4
FEHA NOR_4

YPOD DR_LATCH
YROP DR_LATCH
YNEP DR_LATCH
YZOF DR_LATCH
XUVY DR_LATCH
XERE DR_LATCH
XUZO DR_LATCH
XEXA DR_LATCH
ZYWU XOR
ZUZA XOR
ZEJO XOR
ZEDA XOR
YMAM XOR
YTYP XOR
YFOP XOR
YVAC XOR
YTUB NOR_4
YLEV NOR_4

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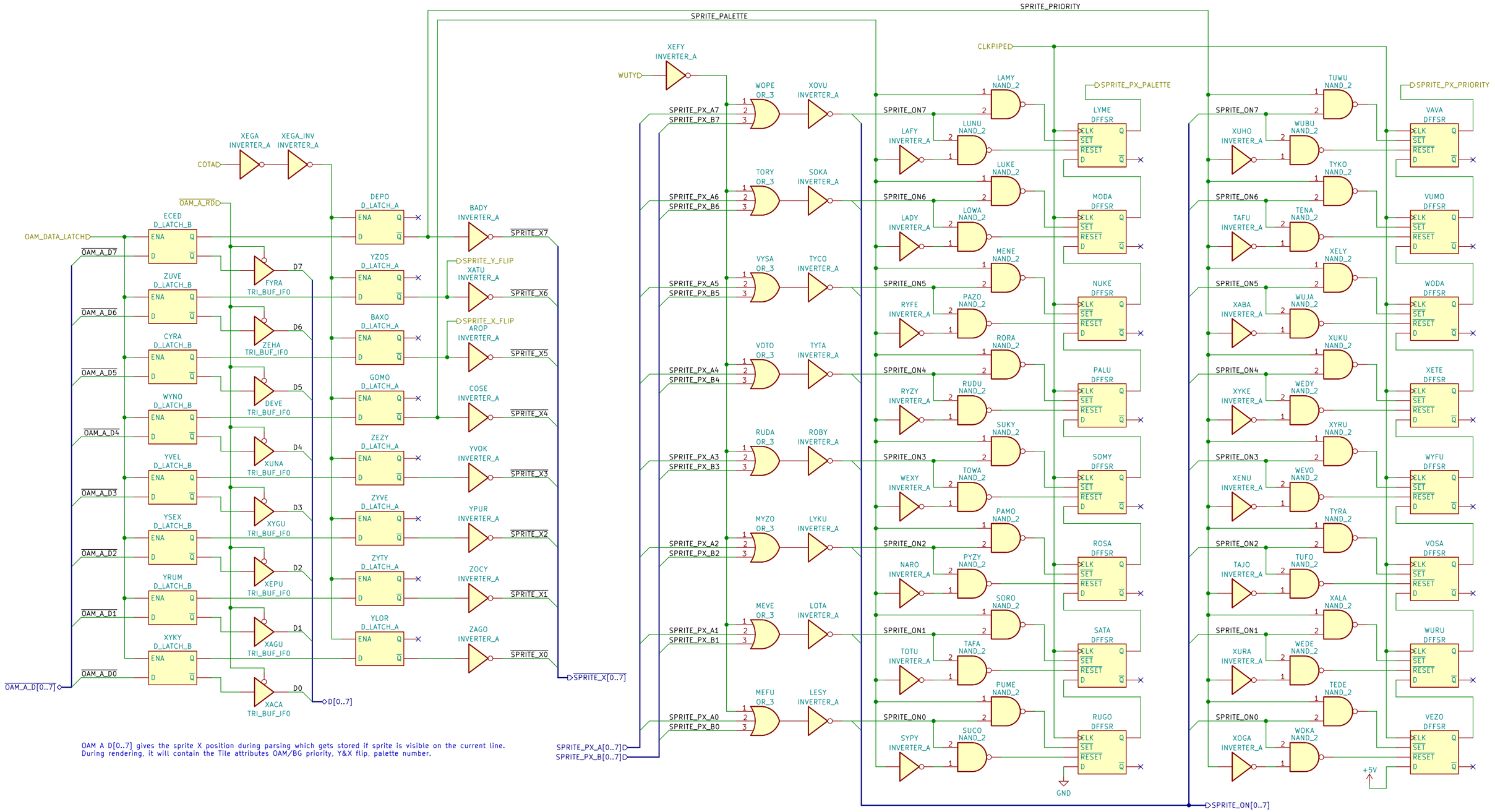
Sheet: /PPU/SPRITE X MATCHERS 5-9/
File: sprite_x_matchers_part2.kicad_sch
Title: DMG CPU B
Size: A3 | Date: 2022-07-08 | Rev: 0.1
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1 | Id: 41/45



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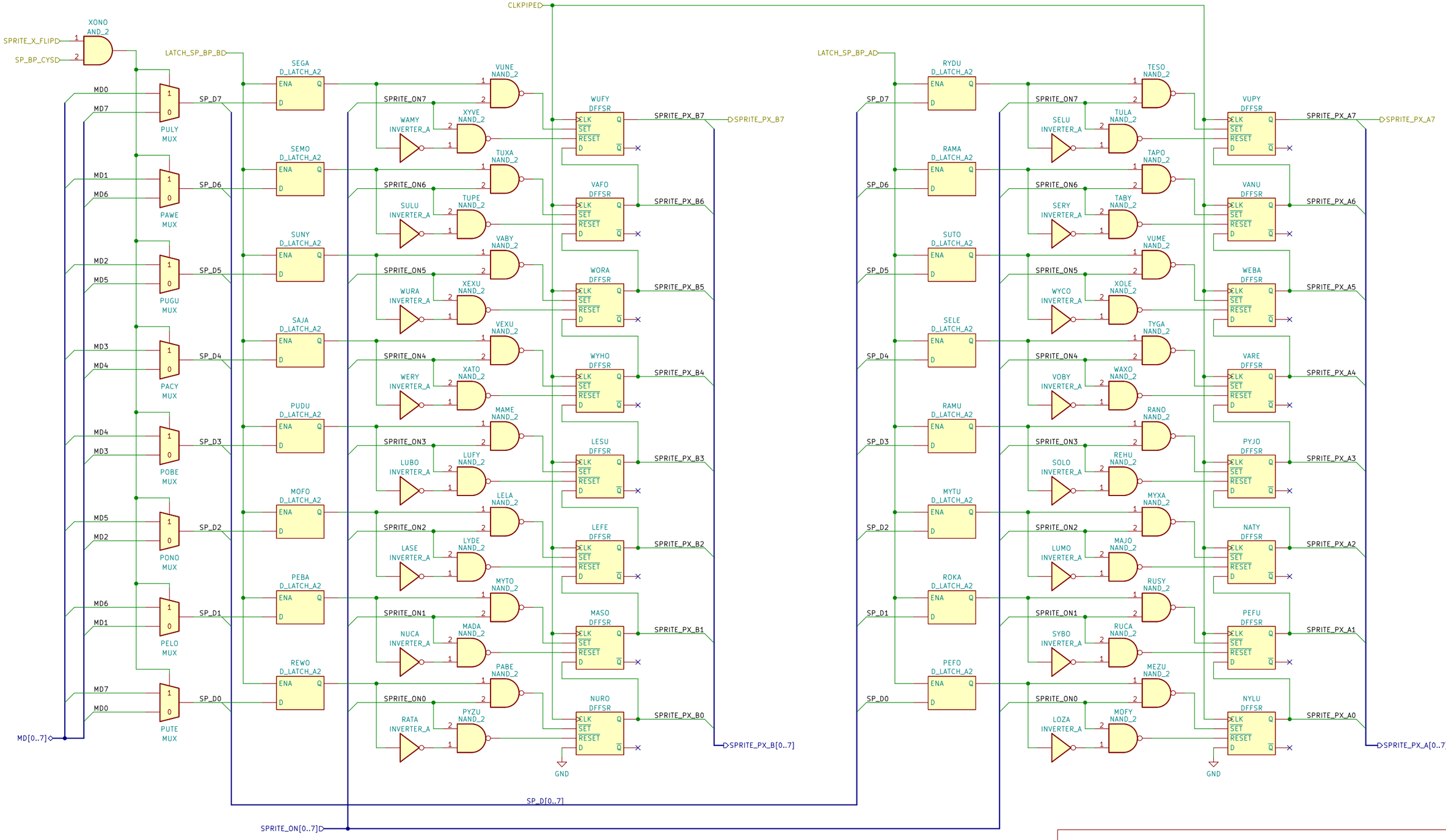
Sheet: /PPU/SPRITE X MATCH TOP/
File: sprite_x_match.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 42/45



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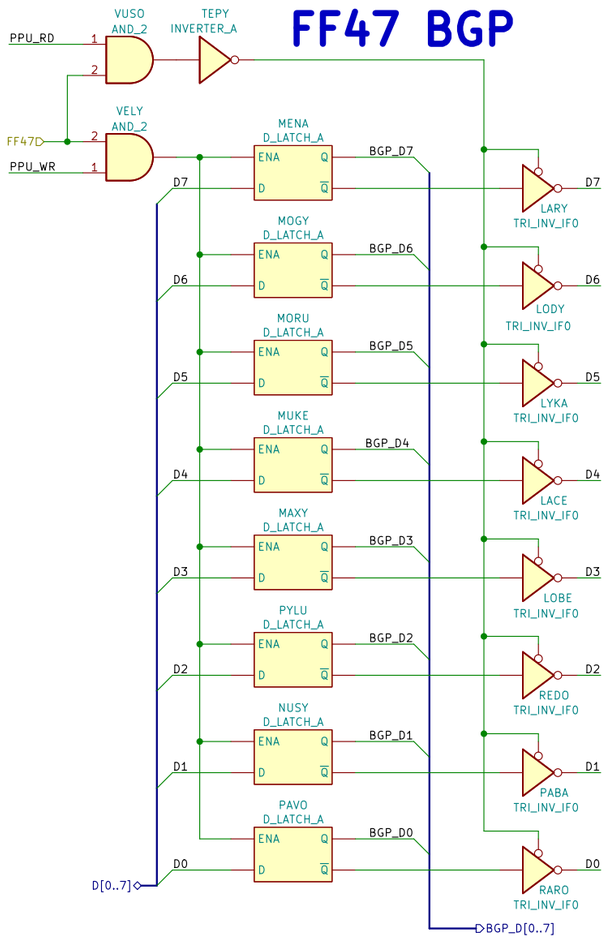
Sheet: /PPU/SP PIXEL SHIFTER/
File: sp_px_shifter.kicad_sch

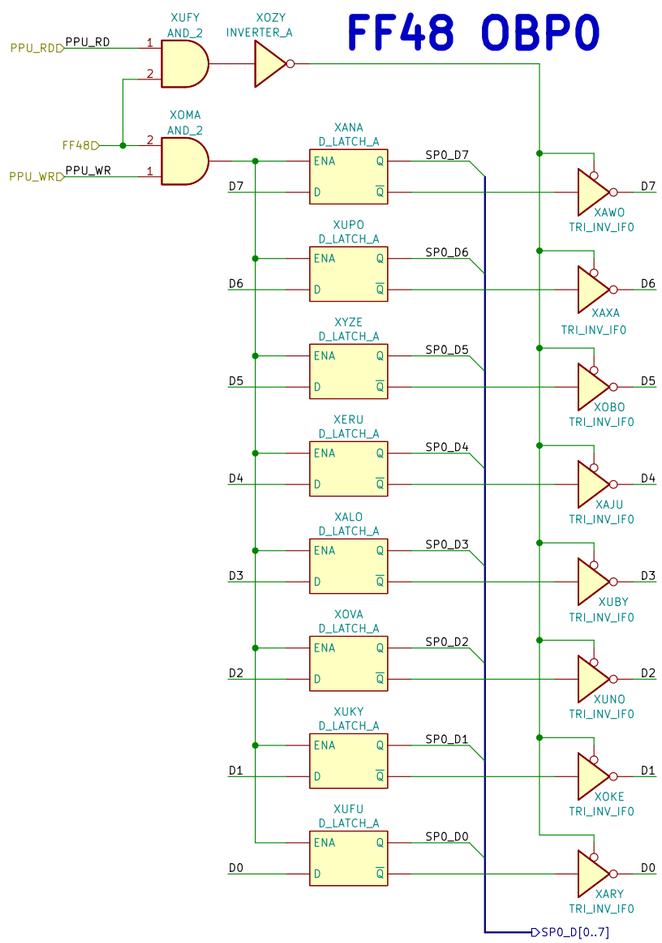
Title: *DMG CPU B*

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 43/45

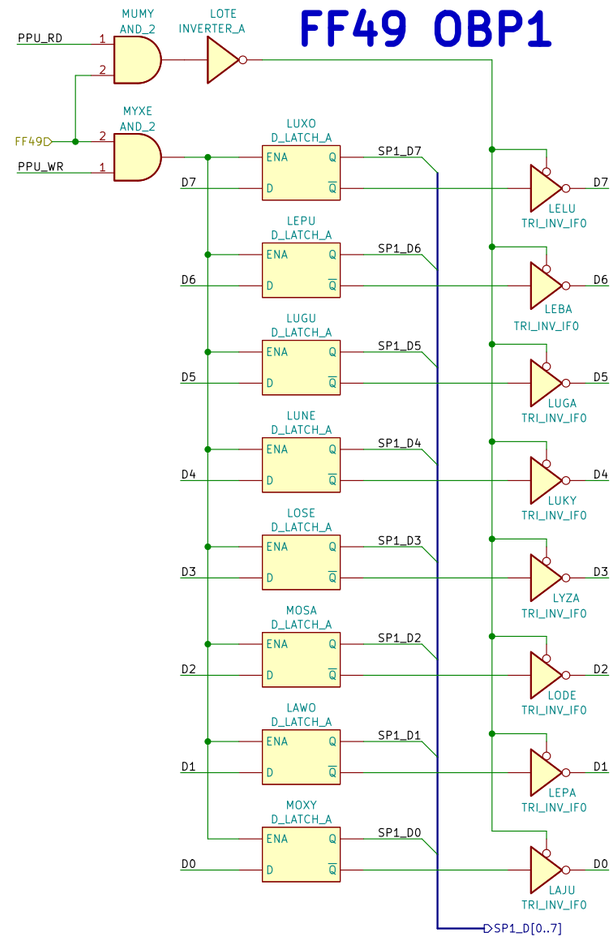
FF47 BGP



FF48 OBP0



FF49 OBP1



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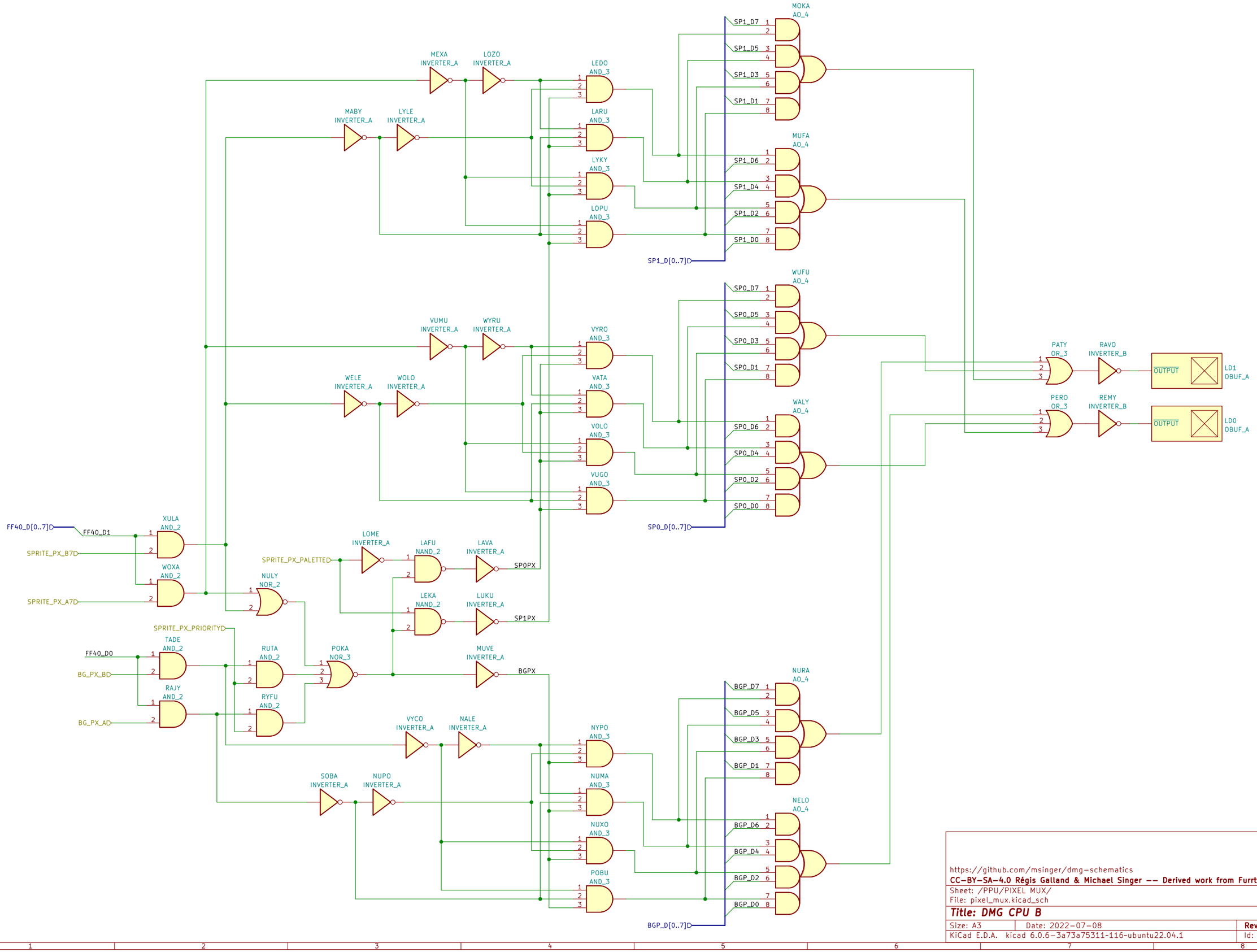
File: palettes.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
KiCad E.D.A. kicad 6.0.6-3a73a75311-116~ubuntu22.04.1		Id: 44/45



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File: pixel_mux.kicad_sch

Title: DMG CPU B

Size: A3	Date: 2022-07-08	**Rev: 0.1**
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