Sprawozdanie Laboratorium PTC

Realizacja układów sekwencyjnych w FPGA

Stanisław Fiedler 160250, L1

LAB 6, 16 grudnia 2024

1 Tresc zadania

Zrealizuj 8-bitowy licznik asynchroniczny zbudowany z przerzutników typu T i zasymuluj jego działanie.

2 Moduł główny

```
-- fourbit_counter.vhd
-- This is a simple 4-bit (Ripple) binary counter made up
-- of four T flip-flops. It also includes a clock divider
-- to bring down the input CK signal from 100 MHz to about 1 Hz.
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity fourbit_counter is
    Port ( CK : in  STD_LOGIC;
           Q : out  STD_LOGIC_VECTOR (7 downto 0));
end fourbit_counter;

architecture Structural of fourbit_counter is

component tff
    Port ( T    : in  STD_LOGIC;
            CK  : in  STD_LOGIC;
            Q, QN : out STD_LOGIC);
end component;

component ck_divider
    Port ( CK_IN : in  STD_LOGIC;
           CK_OUT : out  STD_LOGIC);
end component;

signal all_T, S0, S1, S2, S3, S4, S5, S6, S7, internal_ck : STD_LOGIC;
begin

-- We use signal all_T set to logic '1' to drive
-- input T of all T flip-flops to logic '1'.
all_T <= '1';

CLOCK: ck_divider port map (CK, internal_ck);
TFF0: tff port map (all_T, internal_ck, Q(0), S0);
TFF1: tff port map (all_T, S0, Q(1), S1);
TFF2: tff port map (all_T, S1, Q(2), S2);
TFF3: tff port map (all_T, S2, Q(3), S3);
TFF4: tff port map (all_T, S3, Q(4), S4);
TFF5: tff port map (all_T, S4, Q(5), S5);
TFF6: tff port map (all_T, S5, Q(6), S6);
```

```
41 TFF7: tff port map (all_T, S6, Q(7), S7);
42
43
44 end Structural;
```

3 Plik UCF

```
1
2 # PlanAhead Generated physical constraints
3
4 NET "Q[0]" LOC = U18;
5 NET "Q[1]" LOC = M14;
6 NET "Q[2]" LOC = N14;
7 NET "Q[3]" LOC = L14;
8
9 NET "Q[4]" LOC = M13;
10 NET "Q[5]" LOC = D4;
11 NET "Q[6]" LOC = P16;
12 NET "Q[7]" LOC = N12;
13
14 NET "CK" LOC = L15;
```

4 Wyniki symulacji