

# Realizacja układów cyfrowych z wykorzystaniem FPGA

Stanisław Fiedler 160250, L1

LAB 5, 2 grudnia 2024

## 1 Treść zadania

Korzystając z Xilinx ISE dokonaj implementacji transkodera 4x4.

- Z tabeli 1 wybierz wariant odpowiadający ostatniej cyfrze Twojego numeru indexu.
- Opisz układ w języku VHDL.
- Zaimplementuj układ korzystając z Xilinx ISE
- Wykonaj symulację układu korzystając z ISim

Wariant:

wejście	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
wyjście	1	E	B	F	-	C	0	A	-	4	7	D	6	3	5	9

## 2 Plik VHD

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 entity m2 is
4 Port ( X : in STD_LOGIC_VECTOR(3 downto 0);
5       Y : out STD_LOGIC_VECTOR(3 downto 0));
6 end m2;
7 architecture Behavioral of m2 is
8 begin
9   process (X)
10  begin
11    case X is
12      when "0000" => Y <= "0001";
13      when "0001" => Y <= "1110";
14      when "0010" => Y <= "1011";
15      when "0011" => Y <= "1111";
16
17      when "0101" => Y <= "1100";
18      when "0110" => Y <= "0000";
19      when "0111" => Y <= "1010";
20
21      when "1001" => Y <= "0100";
22      when "1010" => Y <= "0111";
23      when "1011" => Y <= "1101";
24      when "1100" => Y <= "0110";
25      when "1101" => Y <= "0011";
26      when "1110" => Y <= "0101";
```

```

27 when "1111"=>Y<="1001";
28 when others=>Y<="----";
29 end case;
30 end process;
31 end Behavioral;

```

### 3 Plik UCF

```

1 NET "X[0]" LOC="A10";
2 NET "X[1]" LOC="D14";
3 NET "X[2]" LOC="C14";
4 NET "X[3]" LOC="P15";
5 NET "Y[3]" LOC="L14";
6 NET "Y[2]" LOC="N14";
7 NET "Y[1]" LOC="M14";
8 NET "Y[0]" LOC="U18";

```

### 4 Plik testbench

```

1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4 -- Uncomment the following library declaration if using
5 -- arithmetic functions with Signed or Unsigned values
6 --USE ieee.numeric_std.ALL;
7
8 ENTITY tran44tb IS
9 END tran44tb;
10
11 ARCHITECTURE behavior OF tran44tb IS
12
13     -- Component Declaration for the Unit Under Test (UUT)
14
15     COMPONENT m2
16     PORT(
17         X : IN  std_logic_vector(3 downto 0);
18         Y : OUT std_logic_vector(3 downto 0)
19     );
20     END COMPONENT;
21
22
23     --Inputs
24     signal X : std_logic_vector(3 downto 0) := (others => '0');
25
26     --Outputs
27     signal Y : std_logic_vector(3 downto 0);
28     -- No clocks detected in port list. Replace <clock> below with
29     -- appropriate port name
30
31 BEGIN
32
33     -- Instantiate the Unit Under Test (UUT)
34     uut: m2 PORT MAP (
35         X => X,
36         Y => Y
37     );
38
39     X<="0000",
40     "0001" after 100ns,
41     "0010" after 200ns,
42     "0011" after 300ns,
43     "0100" after 400ns,

```

```

44     "0101" after 500ns,
45     "0110" after 600ns,
46     "0111" after 700ns,
47     "1000" after 800ns,
48     "1001" after 900ns,
49     "1010" after 1000ns,
50     "1011" after 1100ns,
51     "1100" after 1200ns,
52     "1101" after 1300ns,
53     "1110" after 1400ns,
54     "1111" after 1500ns;
55
56 END;

```

## 5 Wyniki symulacji

