Embedded Systems Design

Lecture 10

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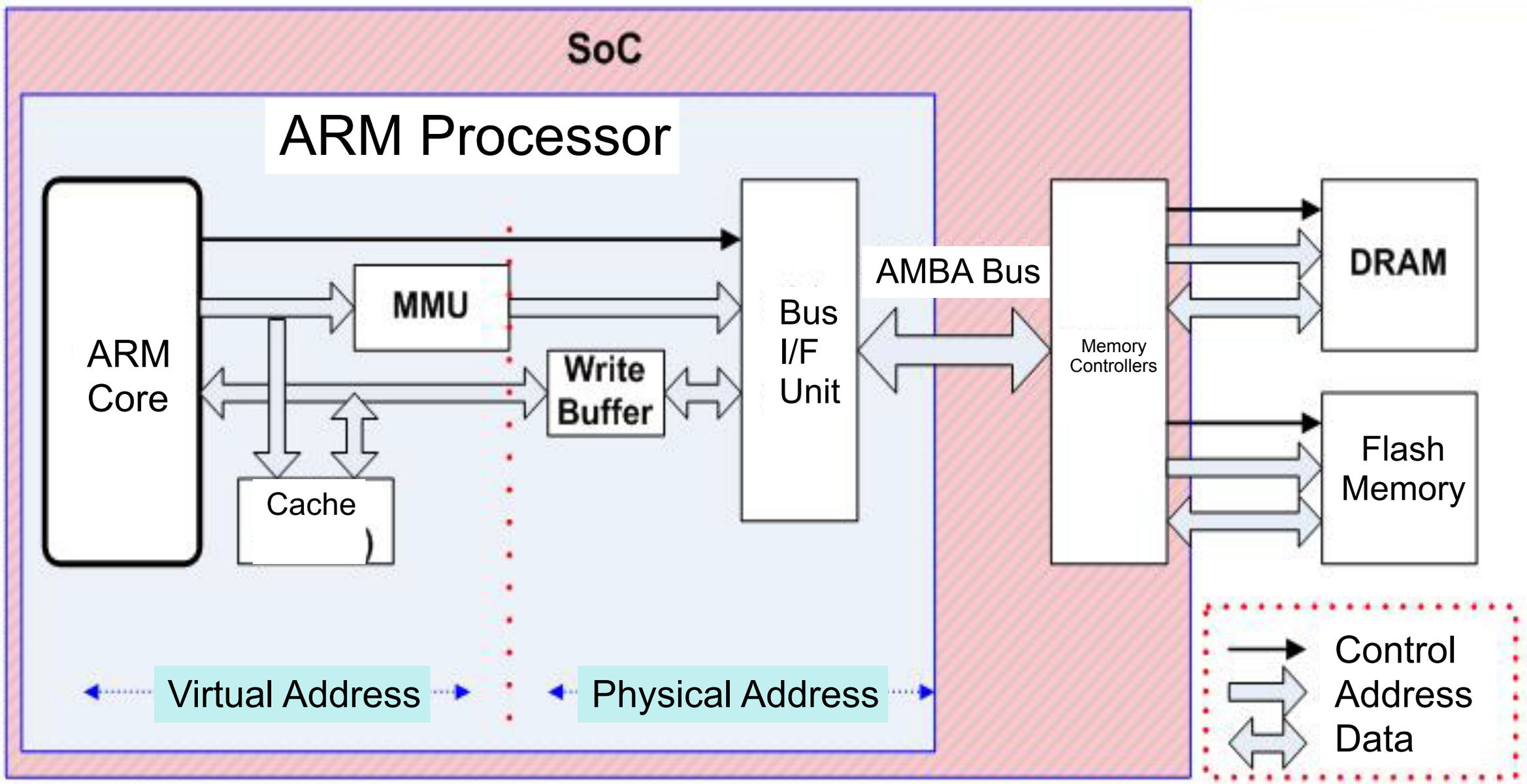
ARM Processor Features

- Co-processor based additional features
  - Old original ARM cores have only MMU-less fixed point computation engines
  - Additional features including cache memory, MMU, write buffer, and TCM (Tightly-coupled memory) are supported as CO-PROCESSORS
  - All the additional features are configured through Co-processor 15

ARM Core and Memory Architecture



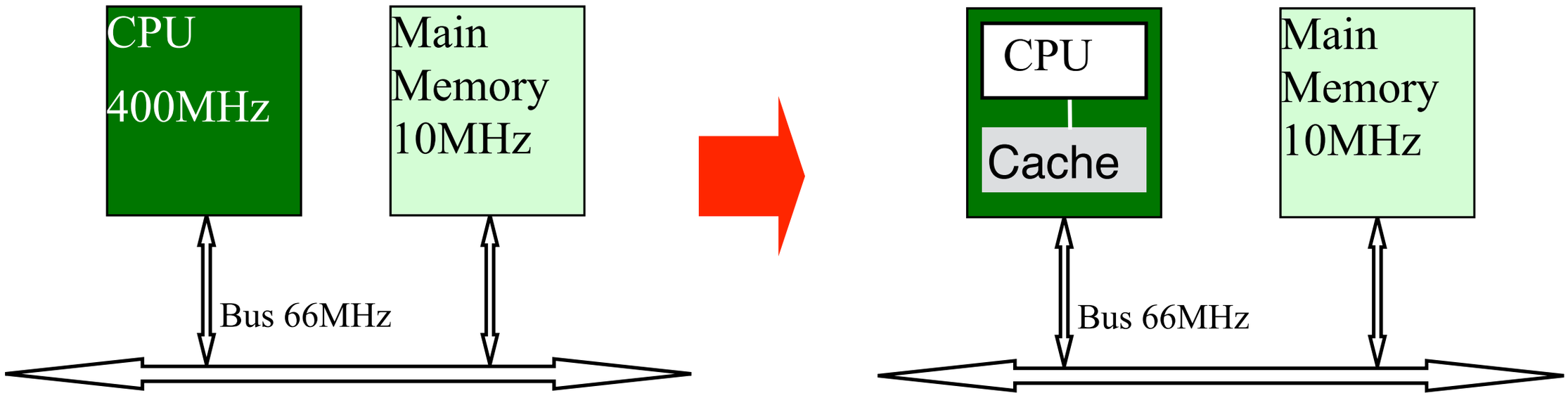
ARM Processor Configuration

- CP15 is used for configuration and control
  - Cache, MMU or MPU, Endian
- Co-processor setting
  - Co-processor setting is possible only through MRC or MCR instructions (Transfers data from general registers to CP15 registers)

Representative CP15 Registers

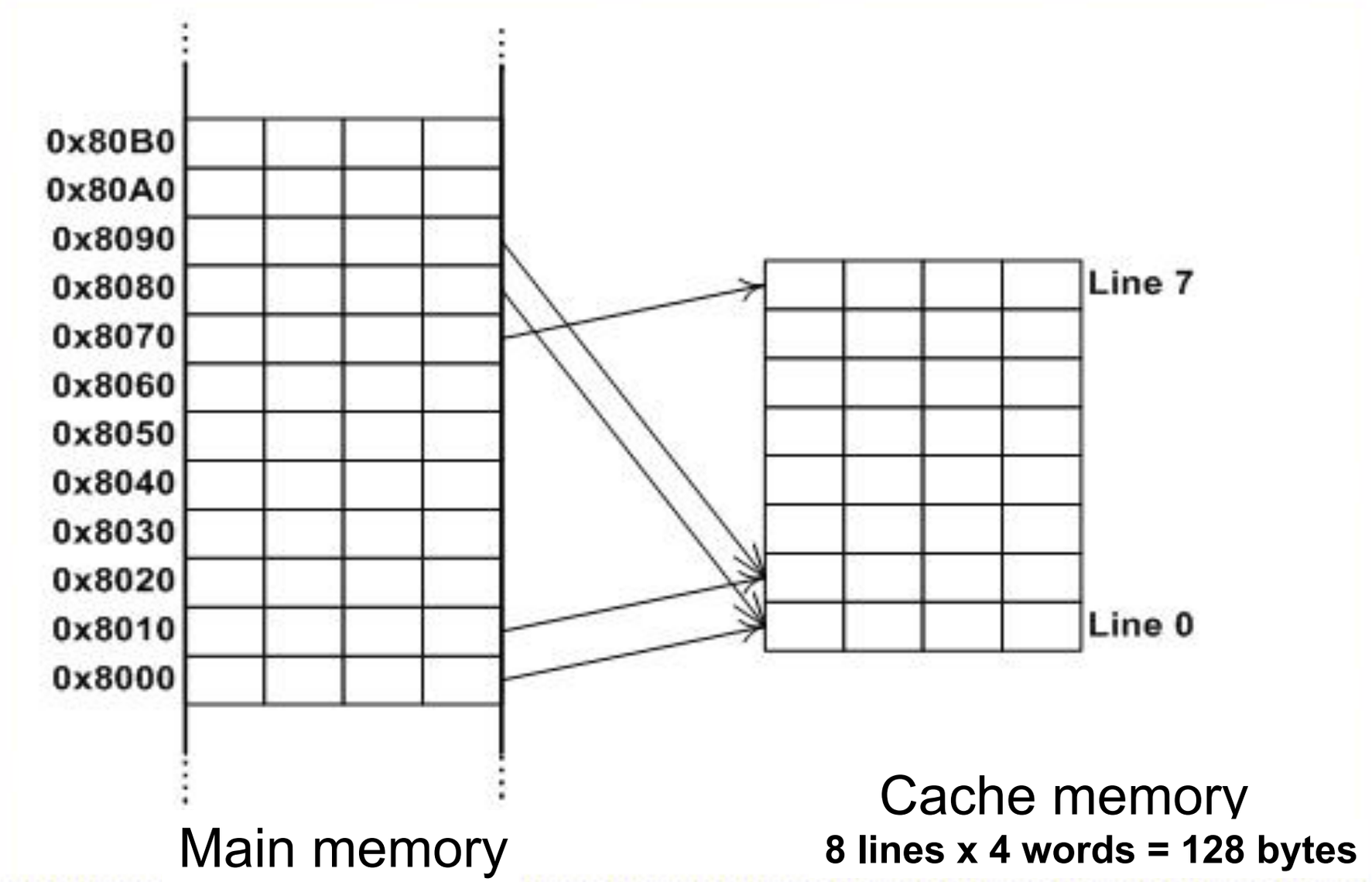
Register	Usage	
0	ID code register	<opc_2>=0
	Cache type register	<opc_2>=1
1	Control Register	Cache, MMU enable, Endian Clock, etc.
2	Translation table base register	
3	Domain access control register	
5	Fault status register	
6	Fault address register	
7	Cache operation register	Cache control
8	TLB operation register	
9	Cache lockdown register	
10	TLB lockdown register	
13	FSCE PID register	Fast Context Switching Extension
14	Debug support register	DCC enabled
4, 11, 12	Reserved	

Cache Memory

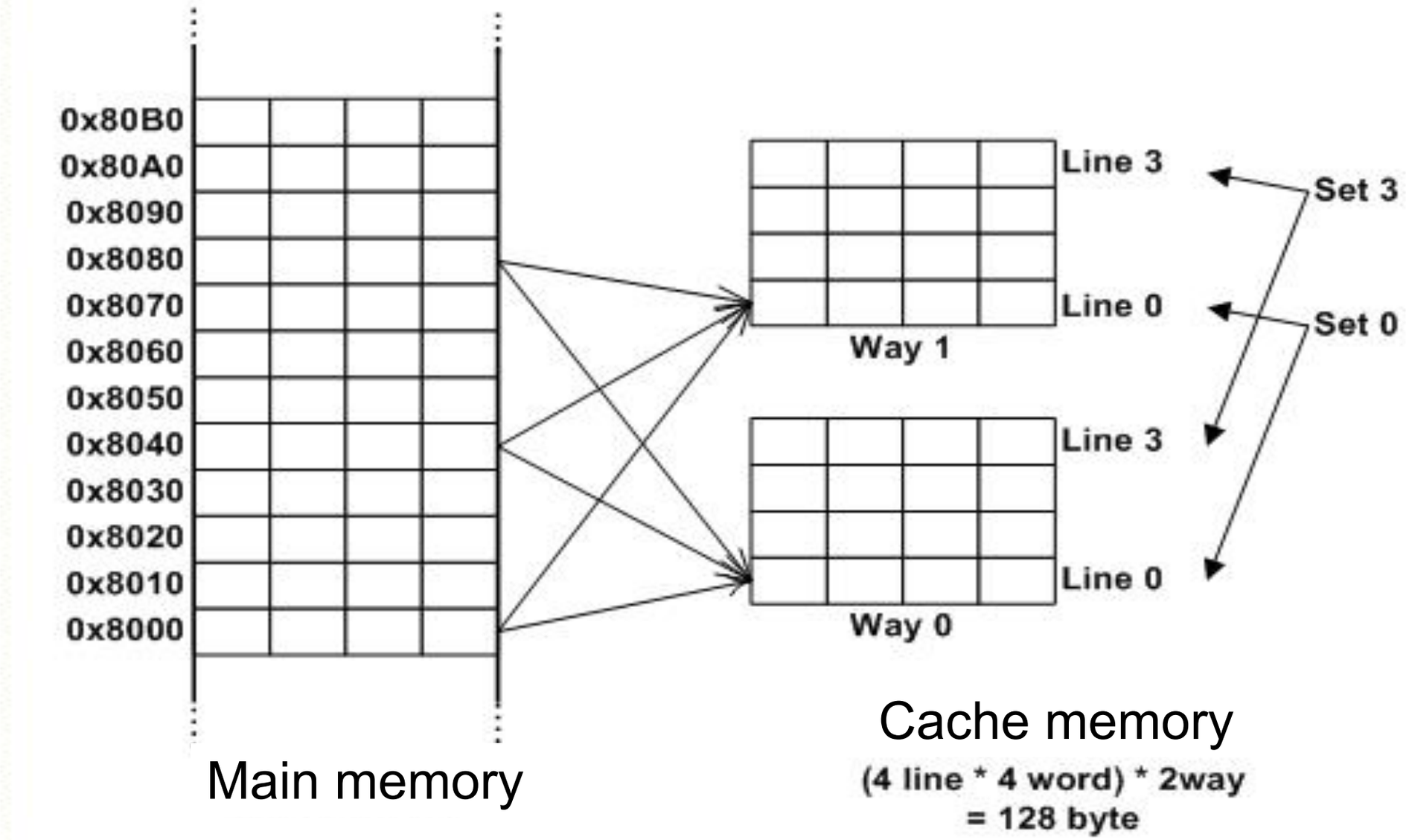


- Cache memory fills the speed gap between CPU and Memory
- Cache configurations
  - Direct mapped, set associative, fully associative
  - Cache line size
- Performance factors
  - Cache hit (miss) ratio

Direct-Mapped Cache

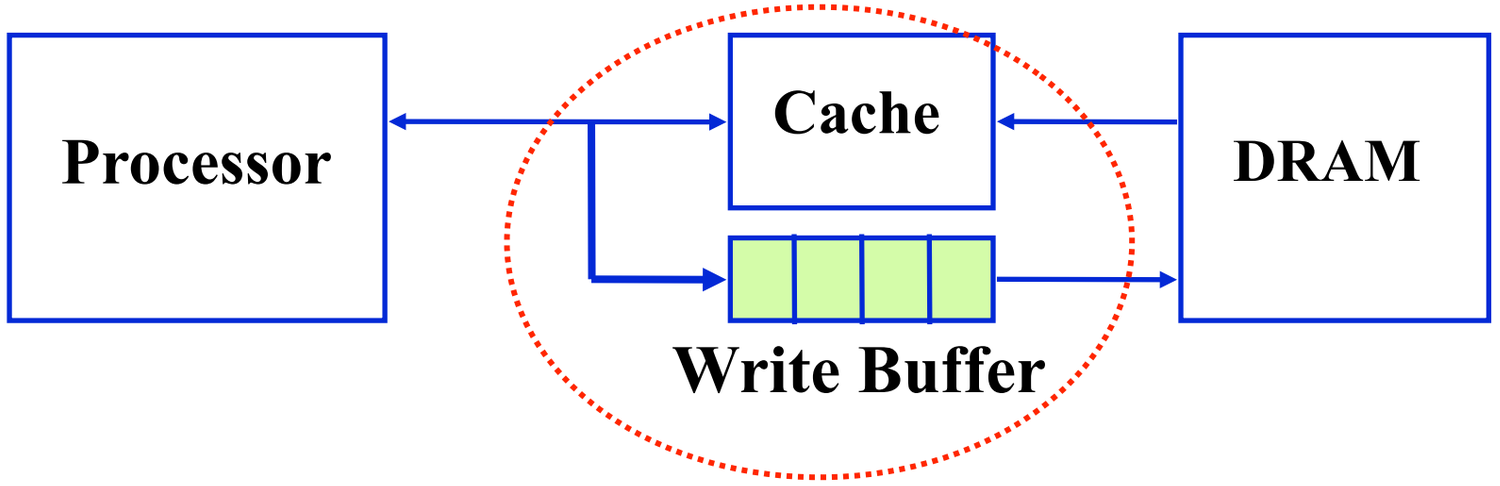


Set-Associative Cache



Write Buffer

- To overcome the speed gap during writing from CPU to memory
- CPU completes writing operation through writing to write buffer before reaching actual main memory

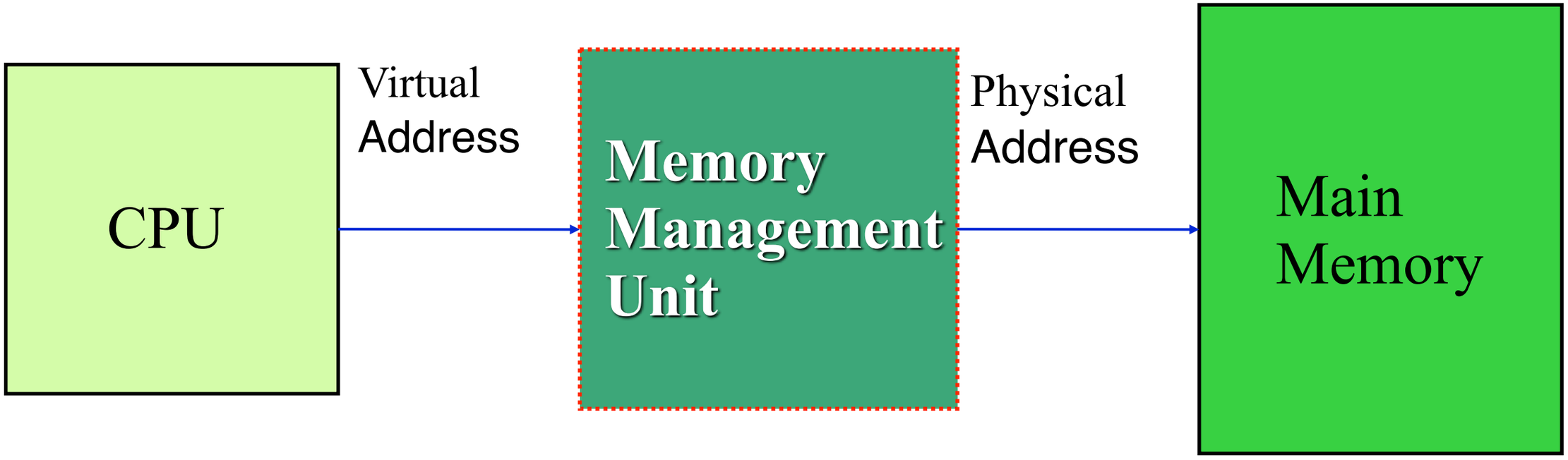


Special Cache Control

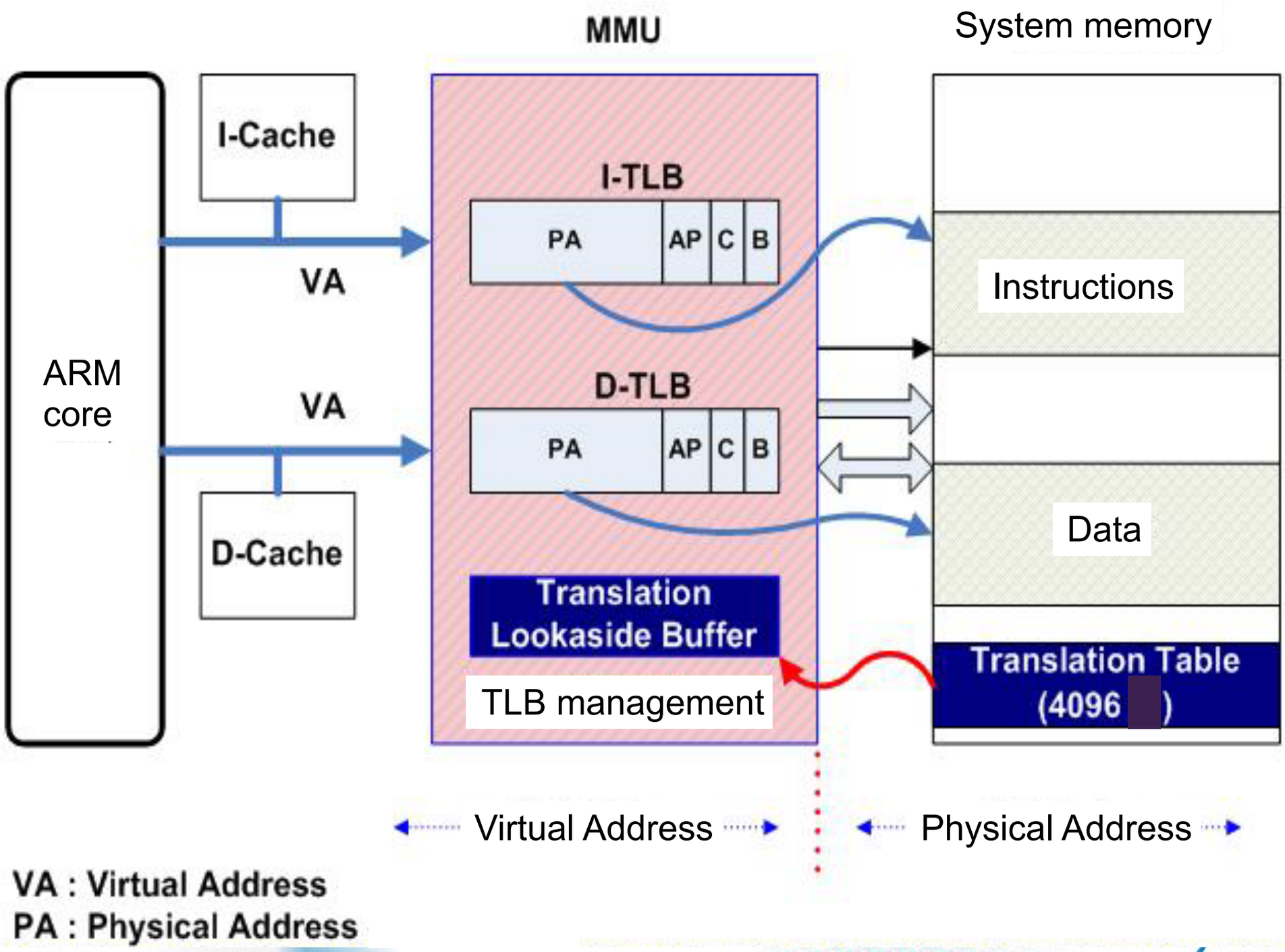
- Cache flush
  - Cleans up cache contents to fetch new data from memory
  - Needed at context switch
- Cache lockdown
  - Prevents certain cache lines from being replaced

MMU (Memory Management Unit)

- Roles of MMU
  - Address translation
  - Protection



Address Translation by MMU

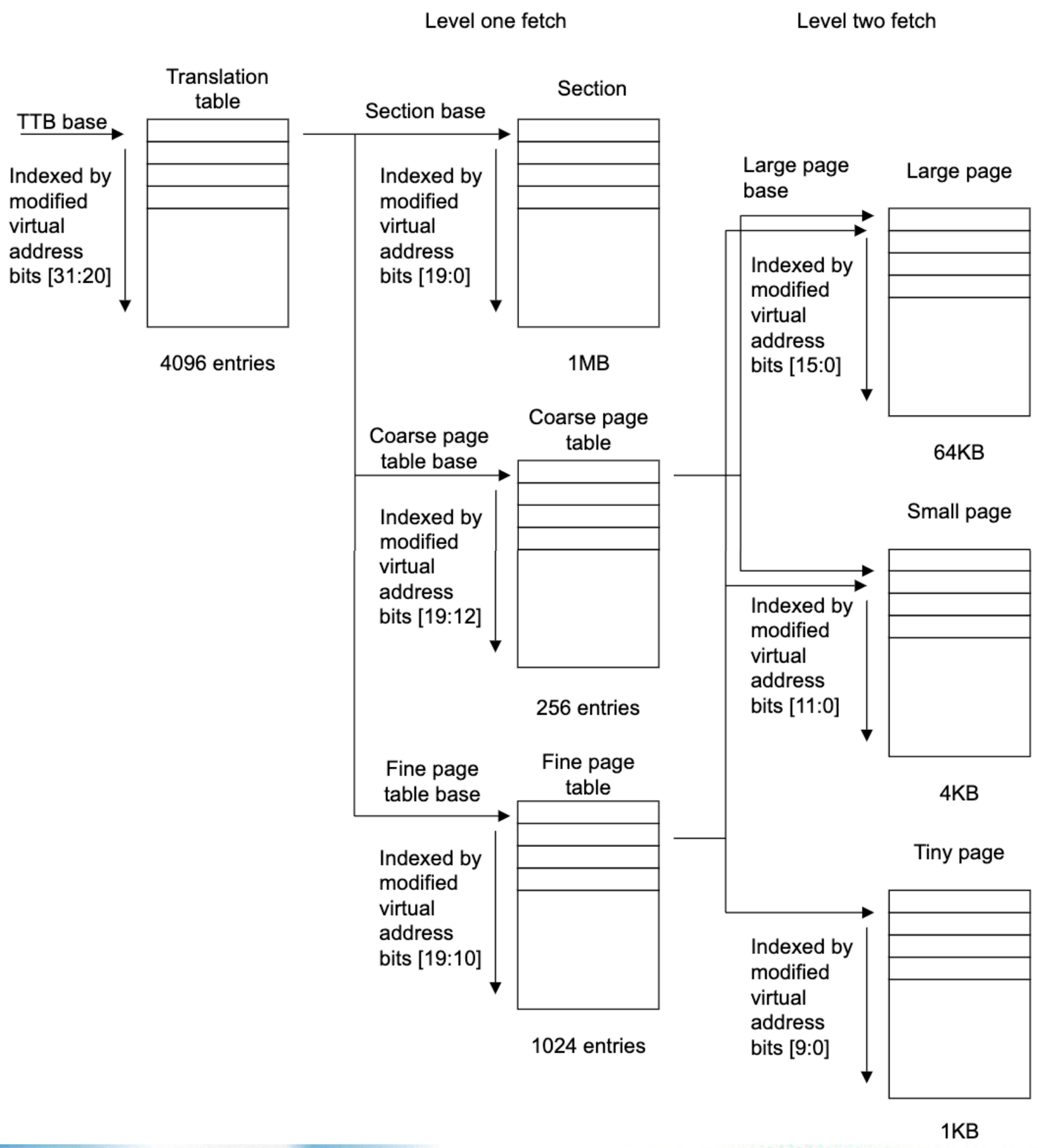


TLB (Translation Lookaside Buffer)

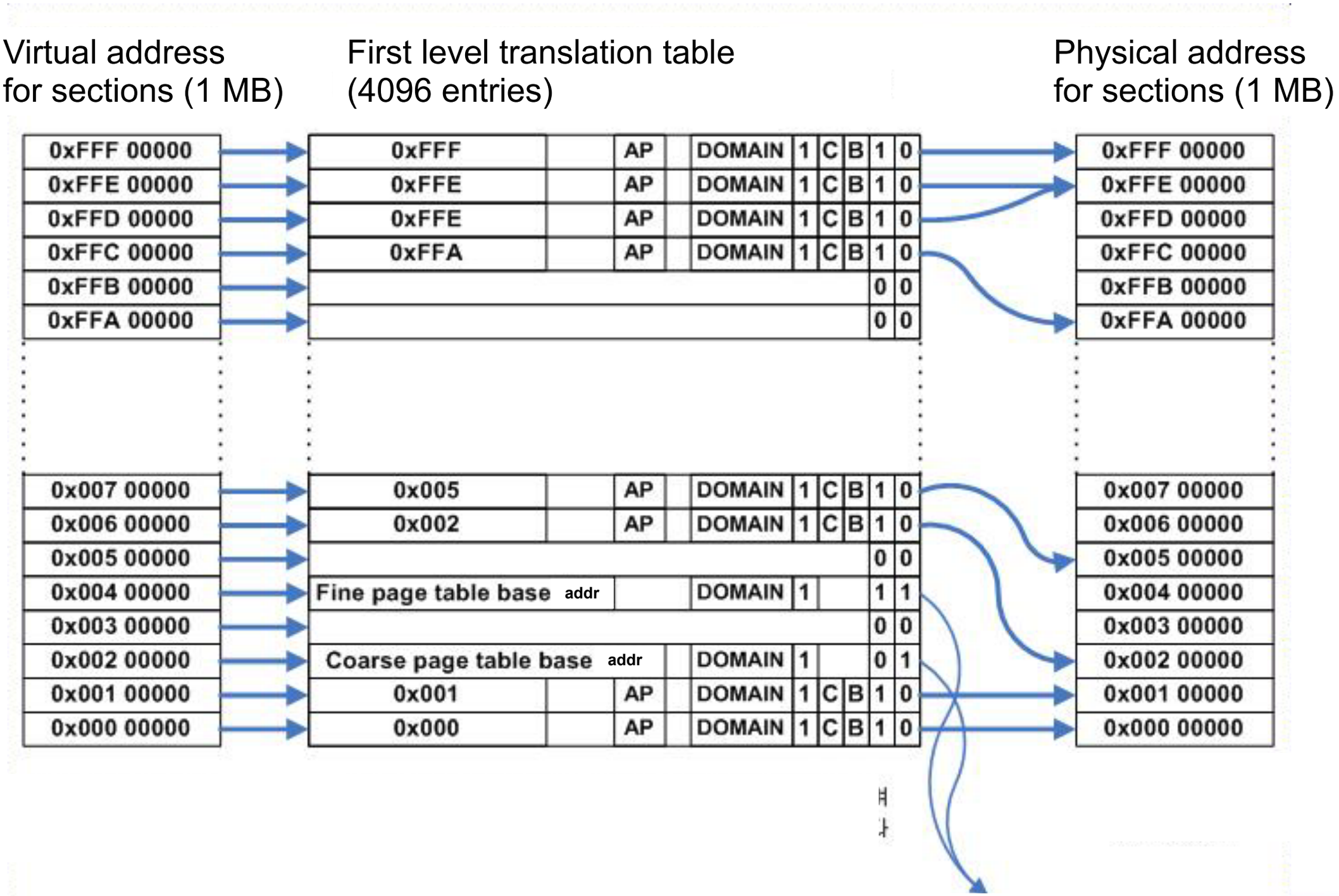
- Cache for address translation data
- Provides fast address translation when TLB access hits
  - TLB miss requires Page Table lookup in main memory
- TLB needs flush operation at context switch

Page Sizes in ARM

- Section
  - 1 MB page
- Tiny page
  - 1 KB page
- Small page
  - 4 KB page
    - Typical page size
- Large page
  - 64 KB page

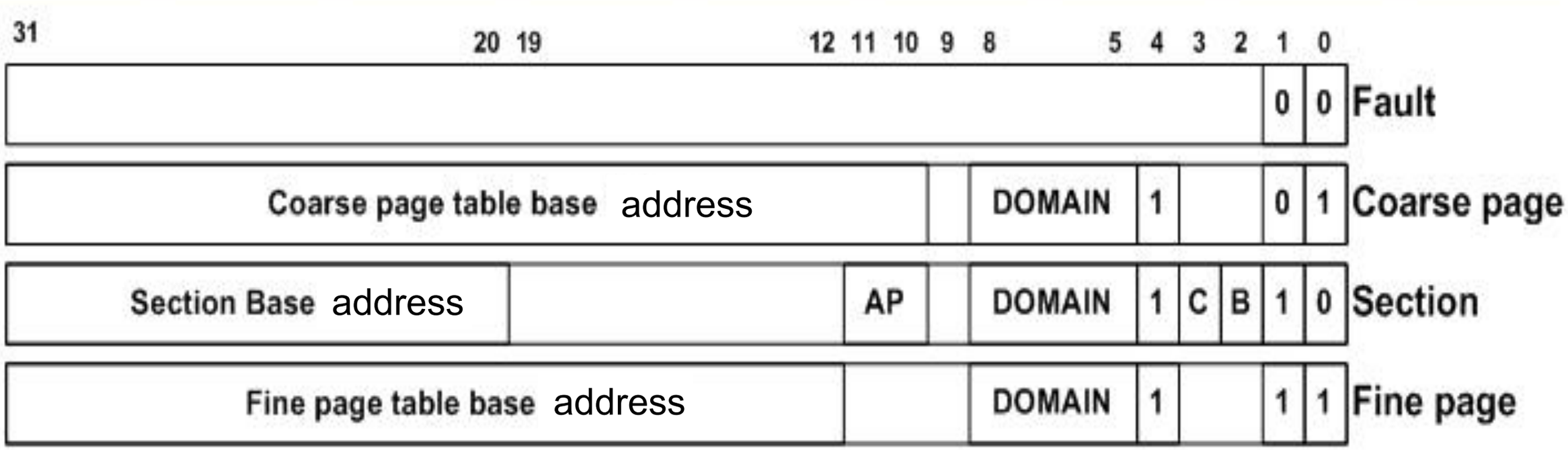

Level one fetch
Level two fetch
Translation table
TTB base
Indexed by modified virtual address bits [31:20]
4096 entries
Section
Section base
Indexed by modified virtual address bits [19:0]
1MB
Coarse page table
Coarse page table base
Indexed by modified virtual address bits [19:12]
256 entries
Fine page table
Fine page table base
Indexed by modified virtual address bits [19:10]
1024 entries
Large page
Large page base
Indexed by modified virtual address bits [15:0]
64KB
Small page
Indexed by modified virtual address bits [11:0]
4KB
Tiny page
Indexed by modified virtual address bits [9:0]
1KB

Address Translation

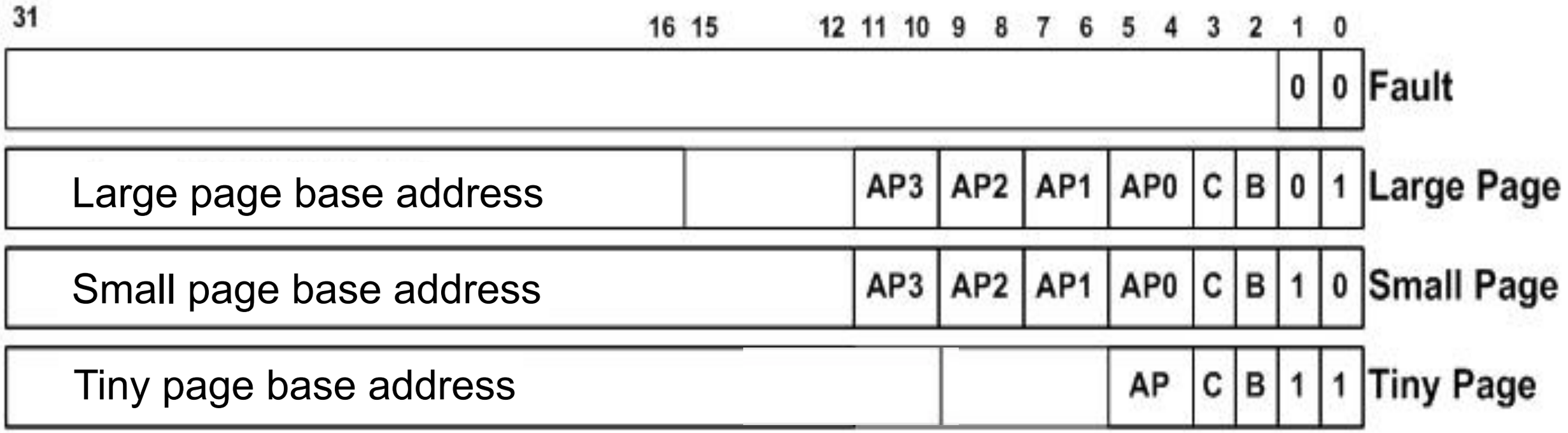


Level 1 Descriptor

- Coarse page table: max 256 entries (256 x 4B = 1KB)
  - Split 1MB space into 256 x 4KB (small page) or 16 x 64KB (large page)
- Fine page table: max 1024 entries (1024 x 4B = 4KB)
  - Split 1MB space into 1024 x 1KB (tiny page)



Level 2 Descriptor

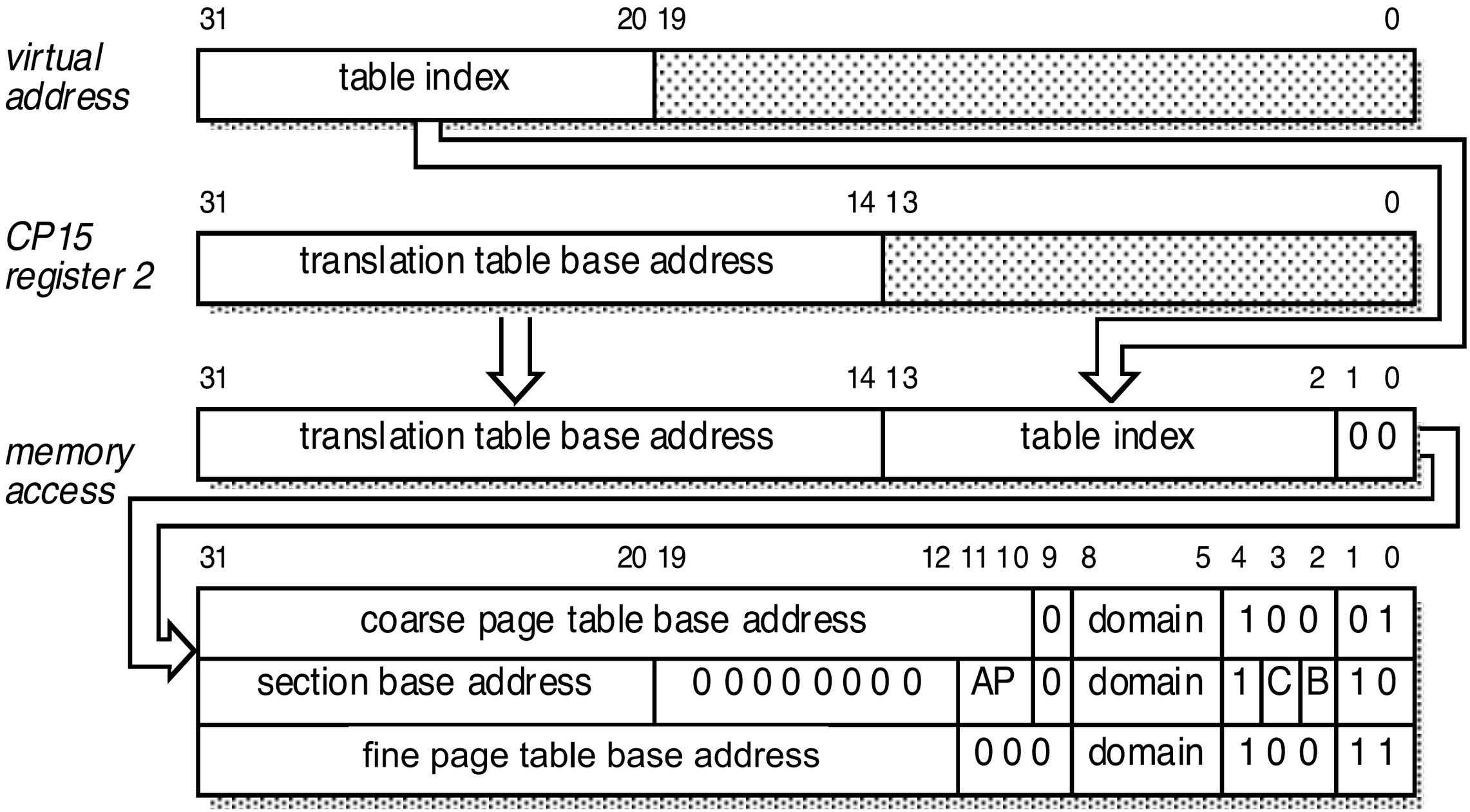


Caching and Write Buffer Control

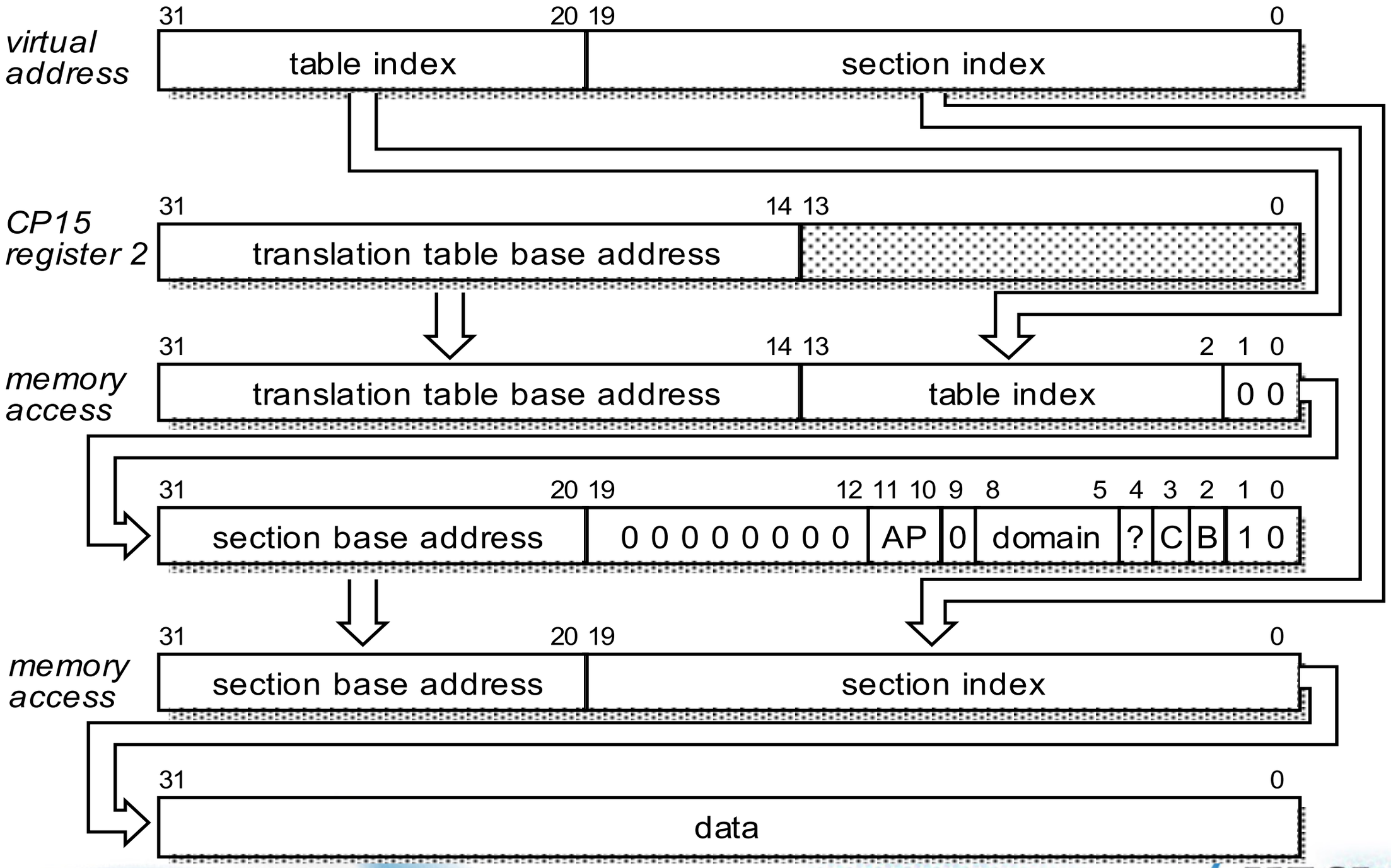
- Caching or write buffering can be configured for each section/page
  - Cacheable bit
  - Bufferable bit
- When a page needs to be configured as NON-CACHEABLE/ NON-BUFFERABLE?
- How to control in page table

C	B	Meaning	Cache write operation
0	0	Non-cacheable, non-bufferable	
0	1	Non-cacheable, bufferable	
1	0	Cacheable, non-bufferable	Write-through Cache
1	1	Cacheable, bufferable	Write-back Cache

First-Level Translation



Section Translation Sequence



Small Page Translation