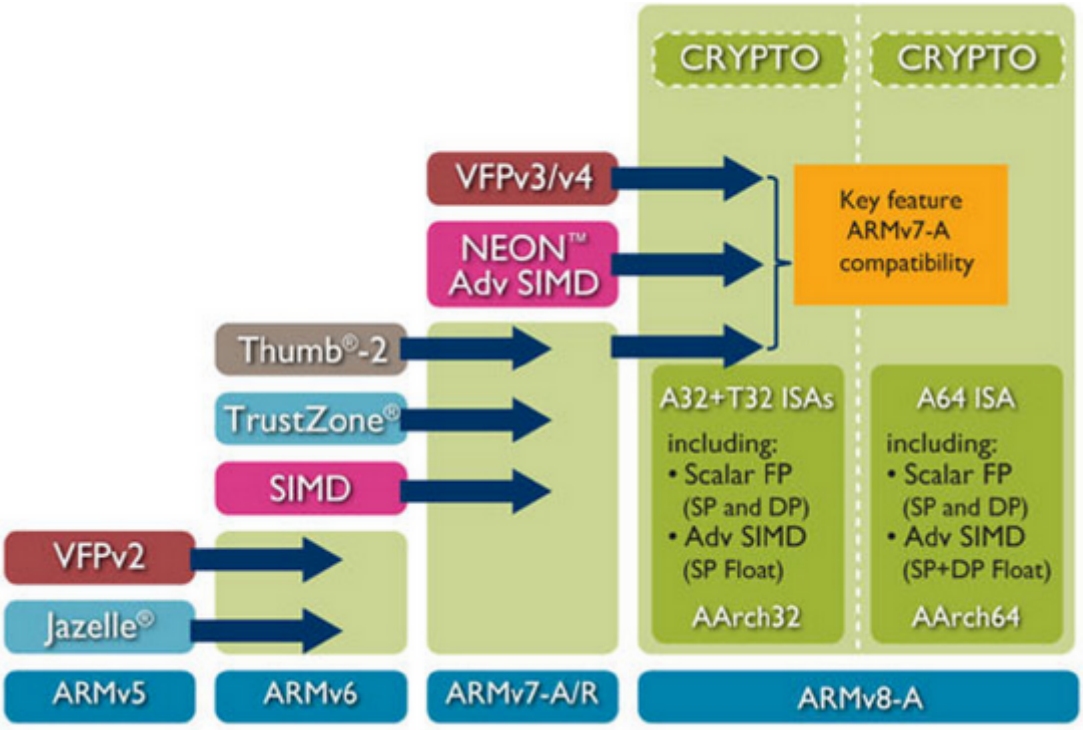
ARM

ARM, Ltd.

- Acorn RISC Machine or Advanced RISC Machines
- Established in 1990
  - Spin-off from Acorn Computer
  - Founded by 12 engineers and CEO
  - Based in Cambridge, UK
  - Acquired by SoftBank, 2016
- Business areas
  - CPU Intellectual Properties
  - No chip manufacturing
  - Over 300 semiconductor partners

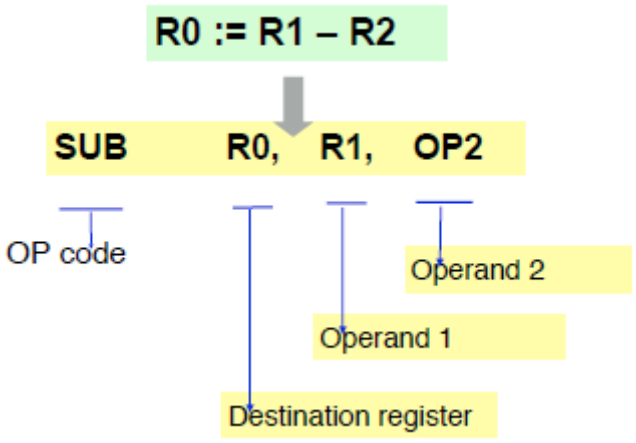
ARM Architecture

- Programmer's model
  - Defines CPU architecture
  - Components
    - Intstruction set
    - Data access architecture
    - Operation mode
    - Register architecture
    - Exception handling mechanism
- An architecture has a number of CPU implementations
  - Around 20 CPU models are based on ARMv4 architecture

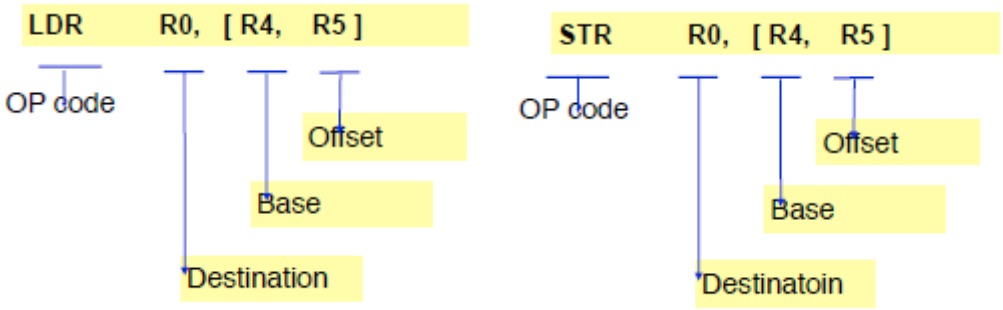


ARM Instruction

- Data processing instruction

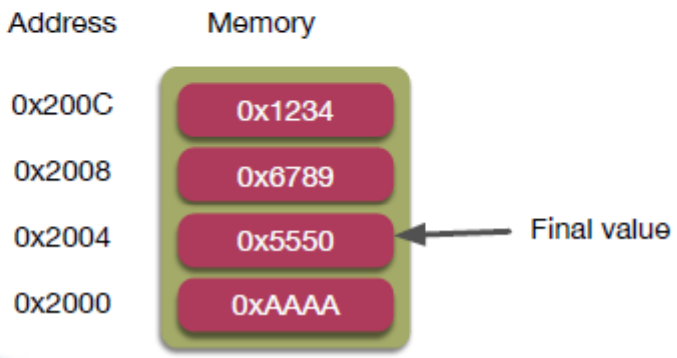


- LDR/STR

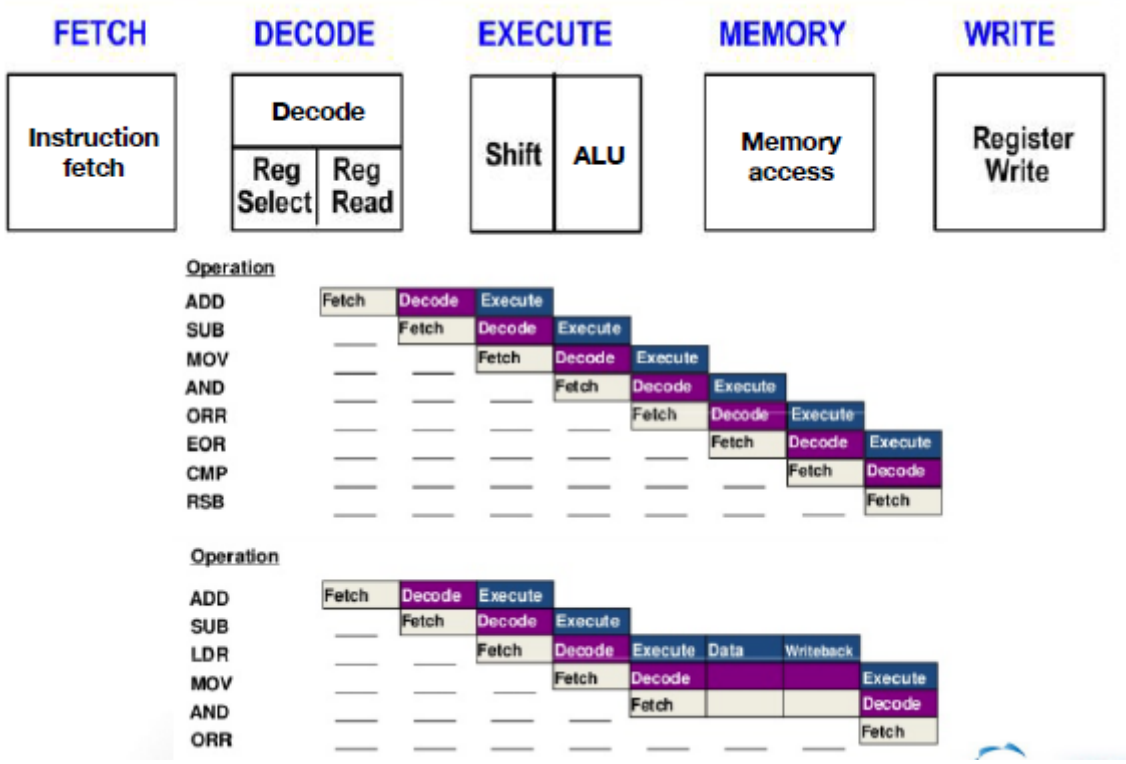


- Assembly Instructions

Address	Instruction	Description
0x1000	LDR R0, [R4, R5]	; R4 = 0x2000, R5 = 0xC ; Load the value in [0x200C] to R0
0x1004	LDR R1, [R4, #8]	; Load the value in [0x2008] to R1
0x1008	ADD R2, R0, #5	; R2 := R0 + 5
0x100C	SUB R3, R1, R2	; R3 := R1 – R2
0x1010	STR R3, [R4, #4]	; Store the value in R3 to [0x2004]



Pipelines



Instruction Set

- ARM Processor Instructions
  - 32 bits ARM instructions
    - Conditional execution
    - Load-Store, Branch instructions are using indirect address mode
    - 11 different instruction types in ARM mode instruction sets

	Instruction Type	Instruction
1	Branch, Branch with Link	B, BL
2	Data Processing	ADD, ADC, SUB, SBC, RSB, RSC, AND, ORR, BIC, MOV, MVN, CMP, CMN, TST, TEQ
3	Multiply	MUL, MLA, SMULL, SMLAL, SMULL, UMLAL
4	Load/Store	LDR, LDRB, LDRBT, LDRH, LDRSB, LDRSH, LDRT, STR, STRB, STRBT, STRH, STRT
5	Load/Store Multiple	LDM, STM
6	Swap	SWP, SWPB
7	Software Interrupt(SWI)	SWI
8	PSR Transfer	MRS, MSR
9	Coprocessor	MRC, MCR, LDC, STC
10	Branch Exchange	BX
11	Undefined	

  - 16 bits Thumb instructions
- Java Support
  - 16 bits Jazelle instruction-based
  - Hardware-based JVM processing optimizations

ARM/Thumb Interwork

- ARM state

    - ready to run 32 bits ARM instructions
    - when an exception occurs,
      CPU state is changed to ARM state regardless of the current state
- Thumb state
    - 16 bits instructions sets are available
    - BX instruction changes CPU modes at run-time

Operating mode

- User mode
- FIQ(Fast Interrupt Request)
- IRQ(Interrupt Request)
- SVC
- Abort mode
- Undefined Mode
- System Mode

Mode Switch

- Exception
    - When exception occurs, HW automatically switches the operating mode to appropriate one
        - When FIQ occurs, HW automatically switches the operating mode to FIQ mode and runs the exception handler
    - Exception types tightly correspond to operating mode
    - Exception Vectors

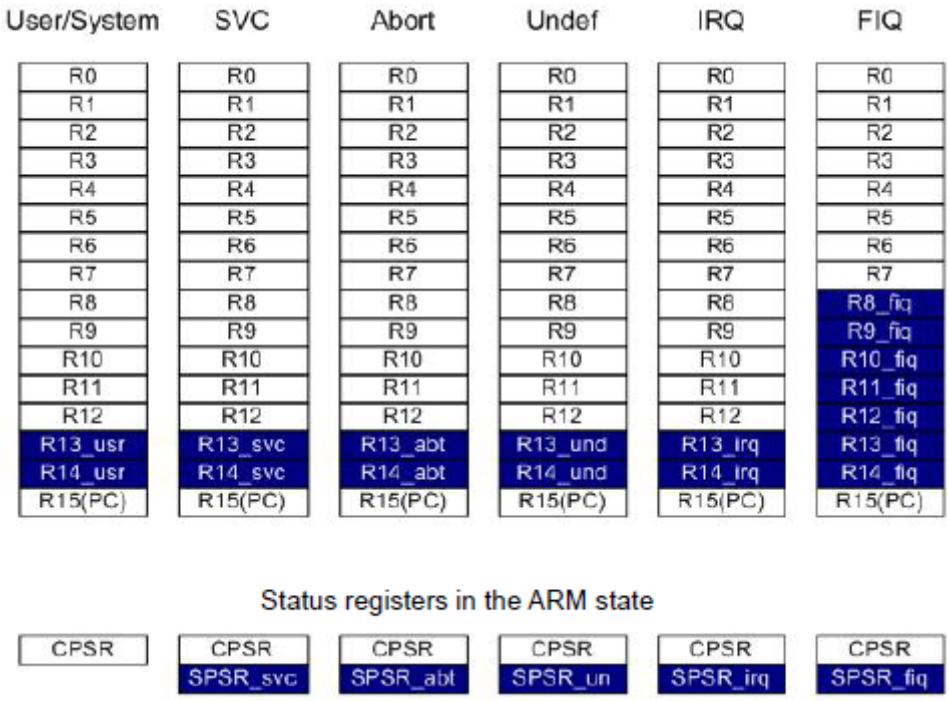
Exception	Vector Address	Priority	Operating Mode
Reset	0x0000 0000	1 (High)	Supervisor(SVC)
Undefined Instruction	0x0000 0004	6 (Low)	Undefined
Software Interrupt(SWI)	0x0000 0008	6	Supervisor(SVC)
Prefetch Abort	0x0000 000C	5	Abort
Data Abort	0x0000 0010	2	Abort
Reserved	0x0000 0014		
IRQ	0x0000 0018	4	IRQ
FIQ	0x0000 001C	3	FIQ

- System calls
    - System calls are implemented by 'SWI' instruction in ARM
    - HW automatically switches the operating mode from USER to SVC

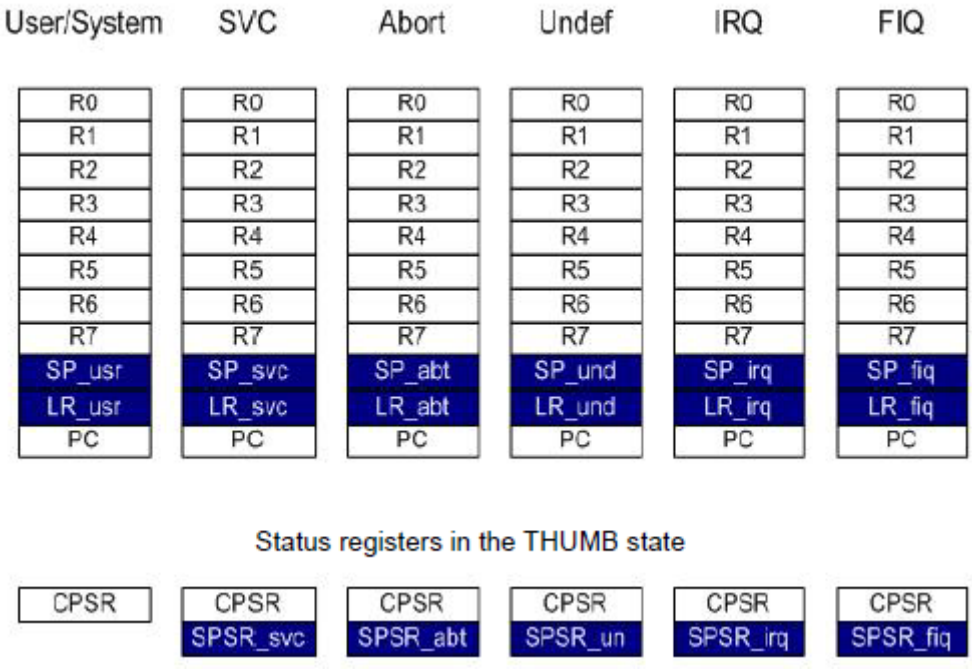
ARM Registers

- General purpose registers
    - 30 registers for data processing instructions
- Special registers

    - PC : R15
    - Current Program Status Register(CPSR)
    - Saved Program Status Register(SPSR)
        - saves CPSR of immediately preceding operating mode when mode switch occurs
- ARM registers for operating modes



- Thumb Mode Registers



Stack Pointer(R13)

- A general purpose register dedicated for another special purpose
- Stores the current SP position
- Each operating mode has it's own SP register
- ARM does not provide PUSH/POP instructions
    - Stack operations are implemented using LDM/STM instructions

Link Register(LR or R14)

- Stores return address when subroutine call occurs
    - BL instruction automatically store the return address to LR
    - Moving the data stored in LR to PC leads to returning from subroutine

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MOV PC, LR
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    - The address stored in LR can be modified using data processing instructions
- Each operating mode has it's own LR register

Program Counter (PC or R15)

- Stores the current address to execute instructions
- The contents of PC can be directly modified using data processing instructions
- Only one PC register in a system

Program Status Register

- PSR Registers in ARM
    - 1 CPSR
    - 5 SPSR(for each operating mode)
- PSR Register Fields

    - Condition Flag
        - reflects ALU processing results
    - Control Bits
        - To control CPU Status