# Embedded Systems Design
Lecture 10

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ARM Processor Features

- Co-processor based additional features
  - Old original ARM cores have only MMU-less fixed point computation engines
  - Additional features including cache memory, MMU, write buffer, and TCM (Tightly-coupled memory) are supported as CO-PROCESSORS
  - All the additional features are configured through Co-processor 15

ARM Core and Memory Architecture
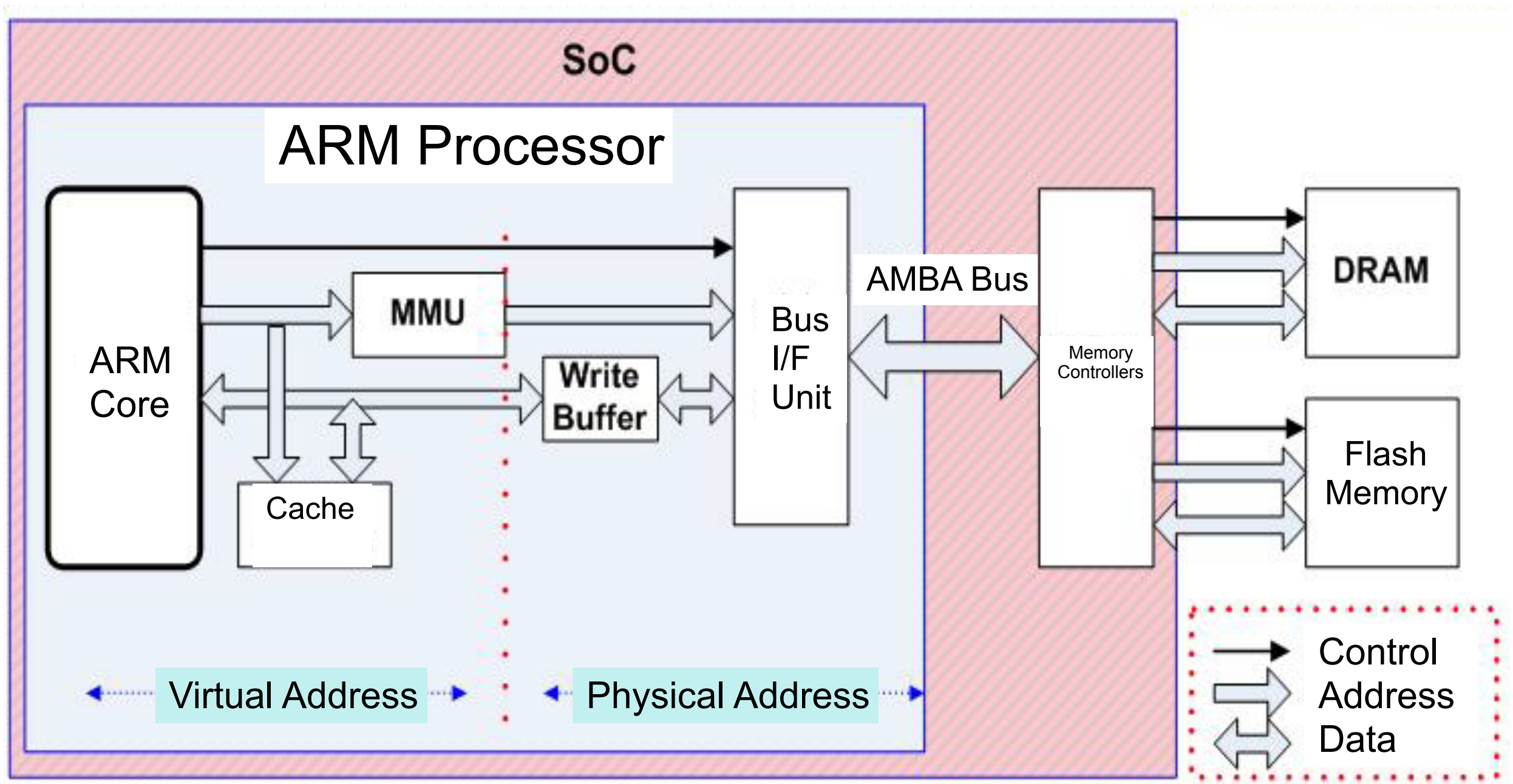
ARM Processor Configuration

- CP15 is used for configuration and control
  - Cache, MMU or MPU, Endian
- Co-processor setting
  - Co-processor setting is possible only through MRC or MCR instructions (Transfers data from general registers to CP15 registers)

Representative CP15 Registers

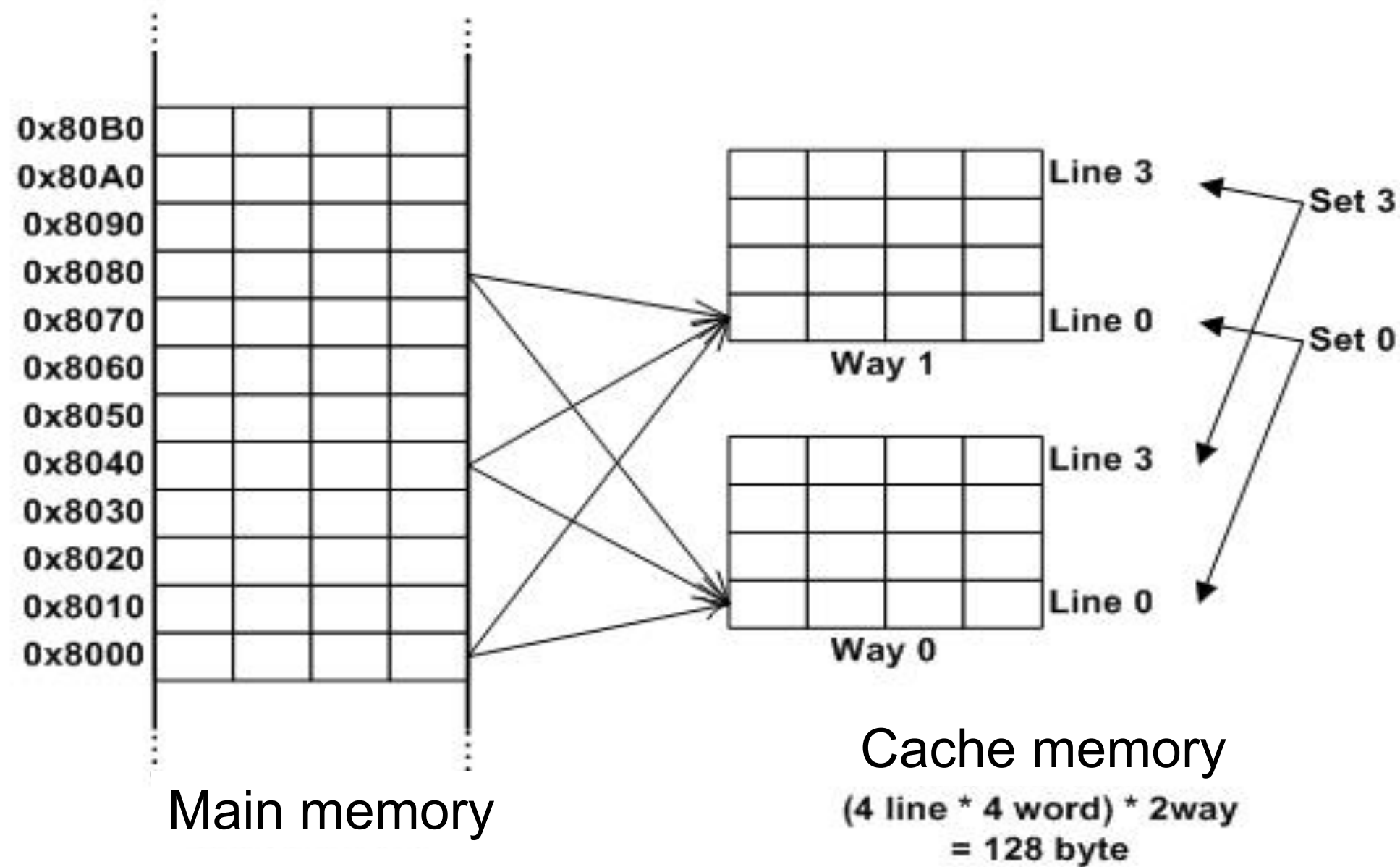| Register	Usage	
0	ID code register	<opc_2>=0
	Cache type register	<opc_2>=1
1	Control Register	Cache, MMU enable, Endian Clock, etc.
2	Translation table base register	
3	Domain access control register	
5	Fault status register	
6	Fault address register	
7	Cache operation register	Cache control
8	TLB operation register	
9	Cache lockdown register	
10	TLB lockdown register	
13	FSCE PID register	Fast Context Switching Extension
14	Debug support register	DCC enabled
4, 11, 12	Reserved	

Cache Memory
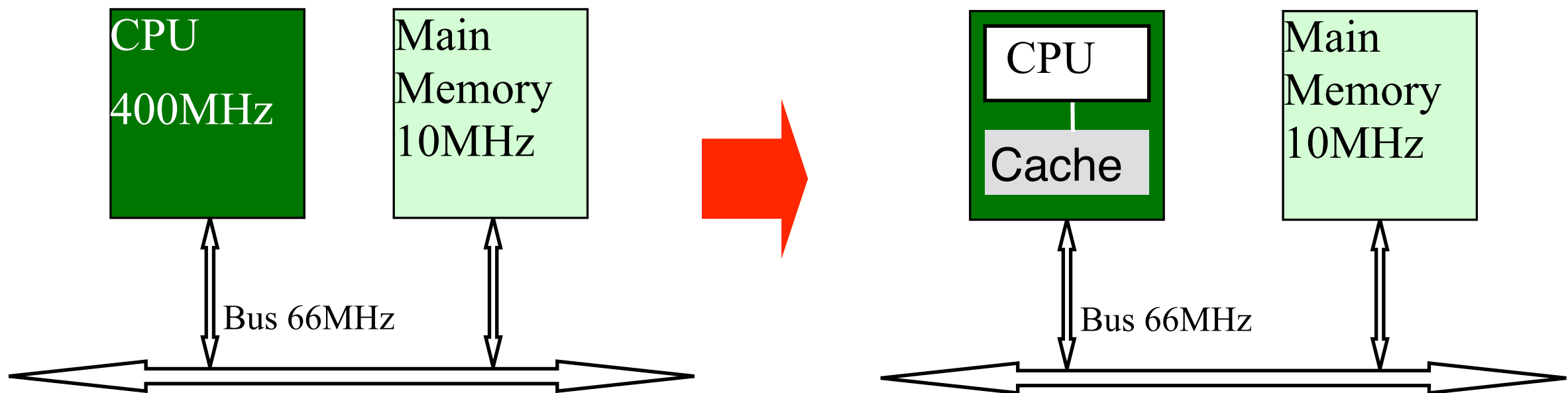
- Cache memory fills the speed gap between CPU and Memory

- Cache configurations
  - Direct mapped, set associative, fully associative
  - Cache line size

- Performance factors
  - Cache hit (miss) ratio

Direct-Mapped Cache

Main memory

Cache memory
8 lines x 4 words = 128 bytes

Set-Associative Cache

Main memory
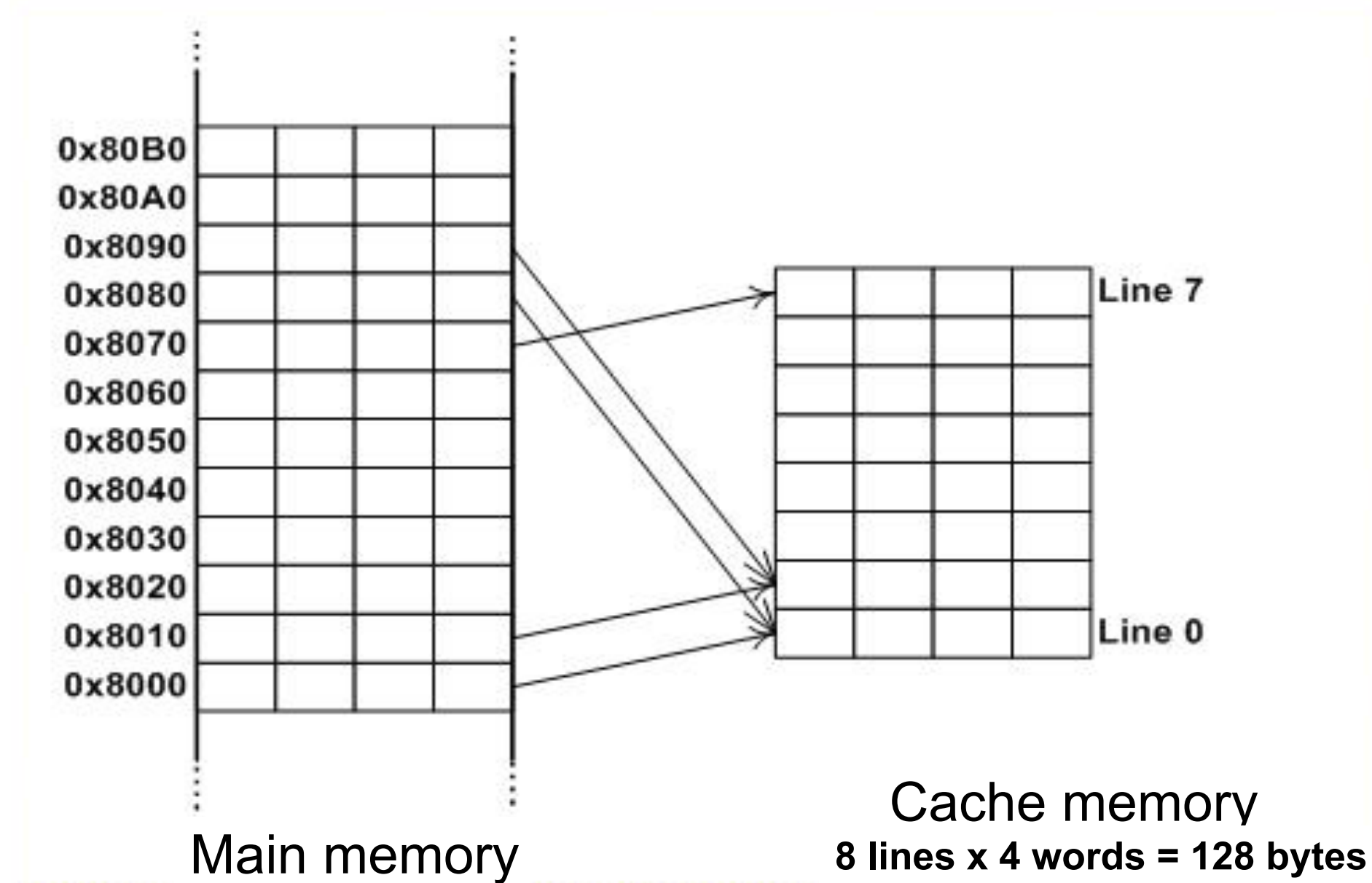
Cache memory

(4 line * 4 word) * 2way
= 128 byte
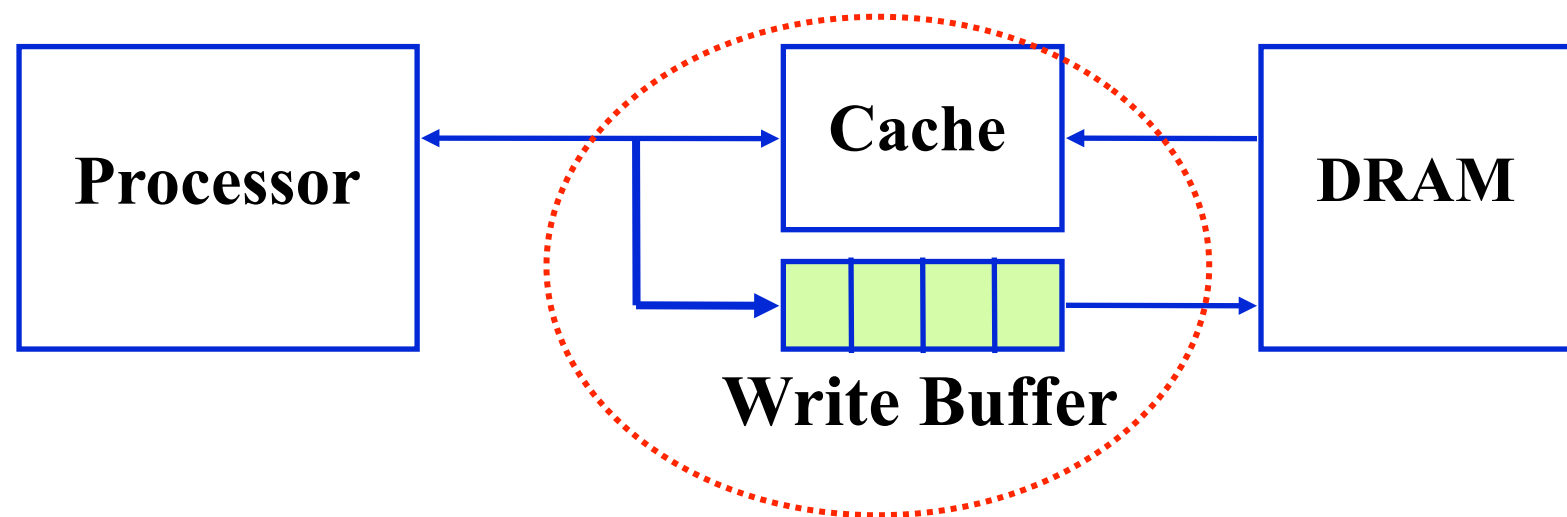
Write Buffer

- To overcome the speed gap during writing from CPU to memory
- CPU completes writing operation through writing to write buffer before reaching actual main memory

Special Cache Control

- Cache flush
  - Cleans up cache contents to fetch new data from memory
  - Needed at context switch
- Cache lockdown
  - Prevents certain cache lines from being replaced

MMU (Memory Management Unit)

- Roles of MMU
  - Address translation
  - Protection

```
┌──────────┐   Virtual              ┌──────────────┐   Physical              ┌──────────┐
│          │   Address              │   Memory     │   Address               │          │
│   CPU    │─────────────────────→  │   Management │─────────────────────→   │  Main    │
│          │                        │   Unit       │                         │  Memory  │
└──────────┘                        └──────────────┘                         └──────────┘
```

Address Translation by MMU

MMU

System memory

I-Cache

I-TLB

| PA | | AP | C | B |

VA

Instructions

ARM core

VA

D-TLB

| PA | | AP | C | B |

D-Cache

Data

Translation Lookaside Buffer

TLB management

Translation Table (4096   )

Virtual Address   Physical Address

VA : Virtual Address
PA : Physical Address
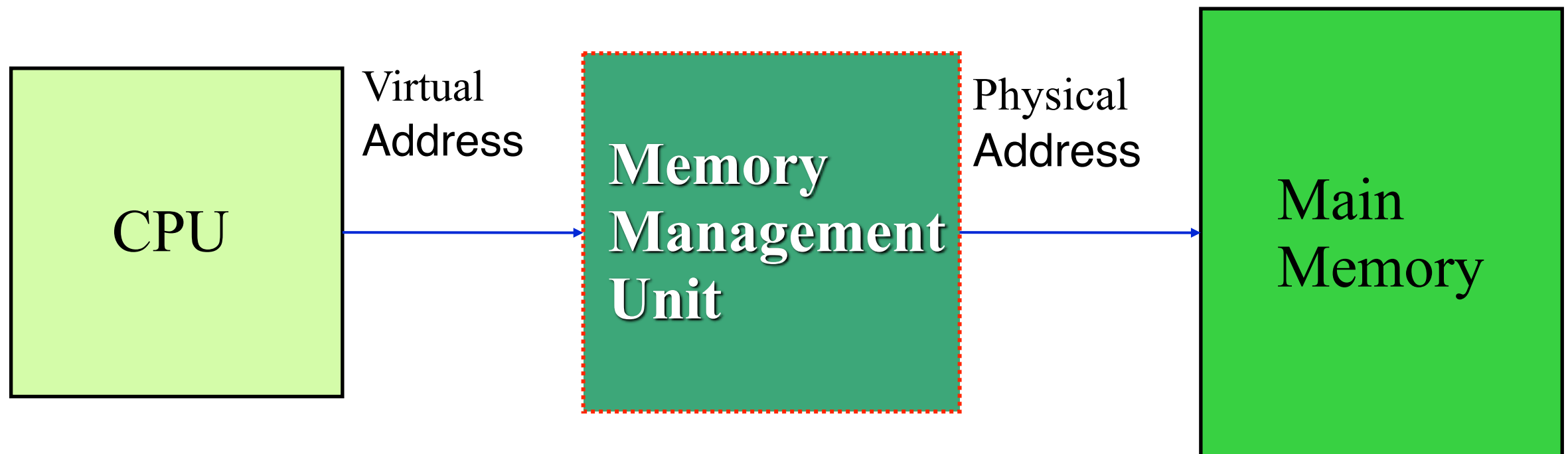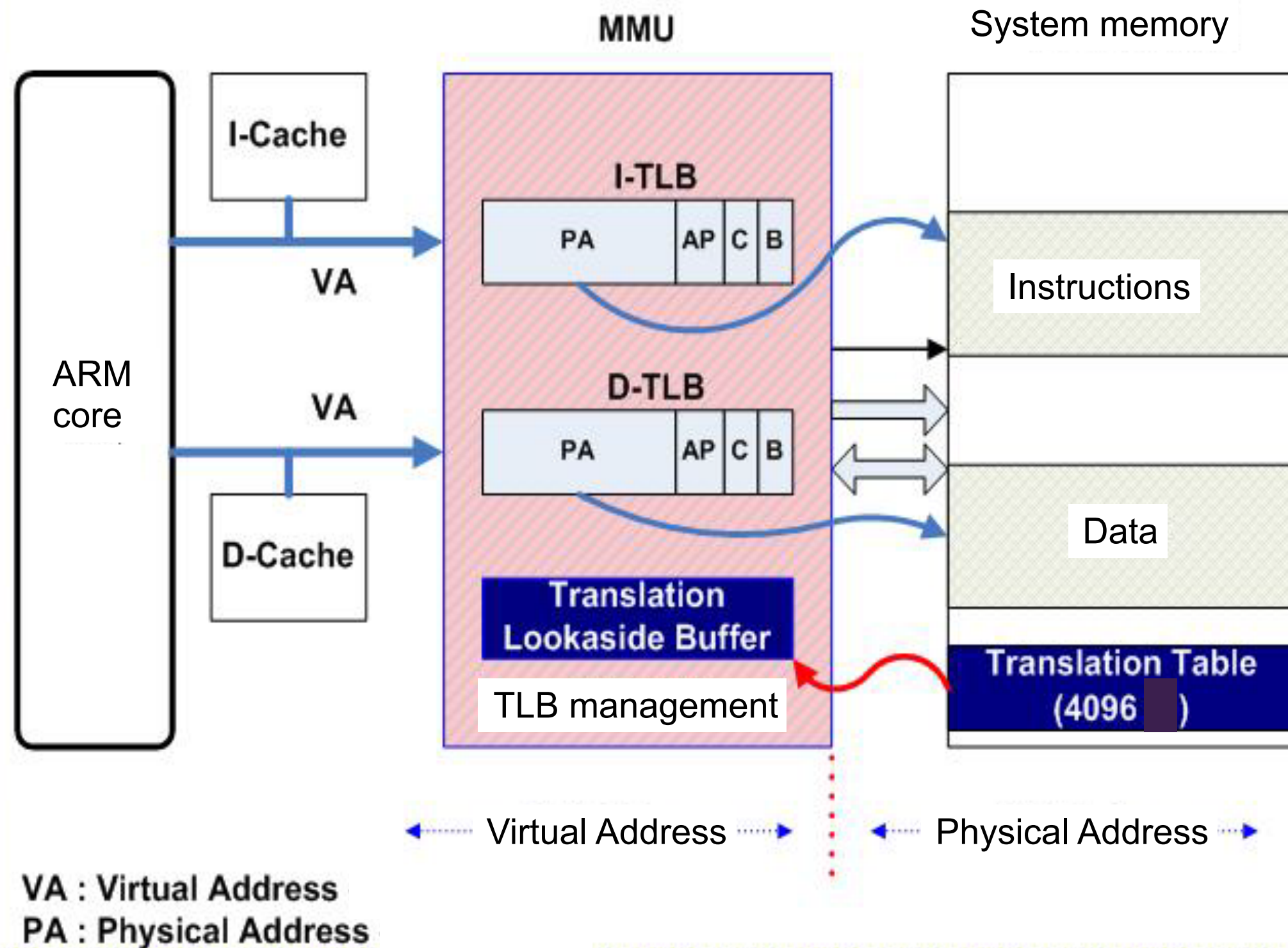
TLB (Translation Lookaside Buffer)

- Cache for address translation data
- Provides fast address translation when TLB access hits
  - TLB miss requires Page Table lookup in main memory
- TLB needs flush operation at context switch
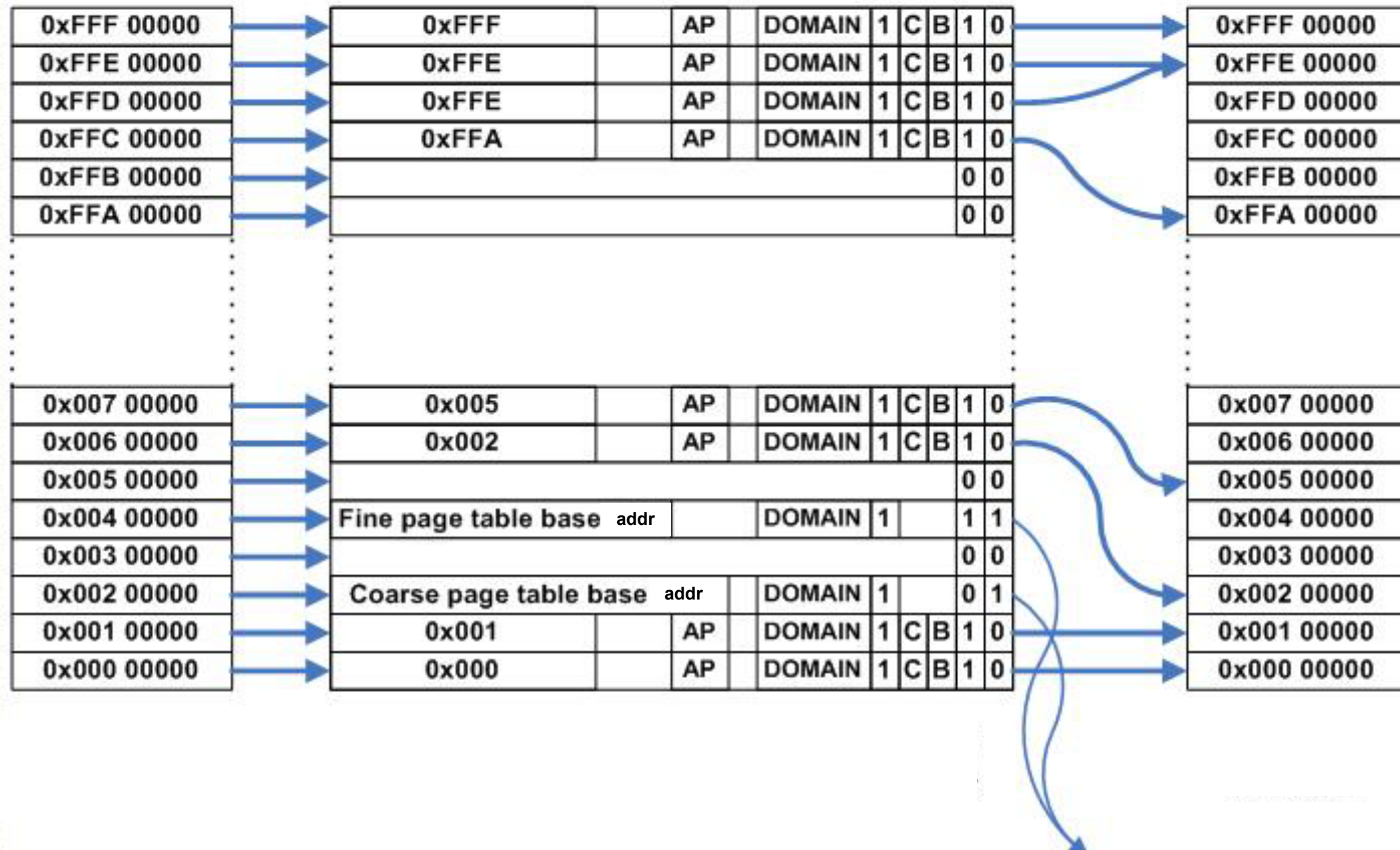
Page Sizes in ARM

- Section
  - 1 MB page
- Tiny page
  - 1 KB page
- Small page
  - 4 KB page
    - Typical page size
- Large page
  - 64 KB page

Address Translation

Virtual address for sections (1 MB)

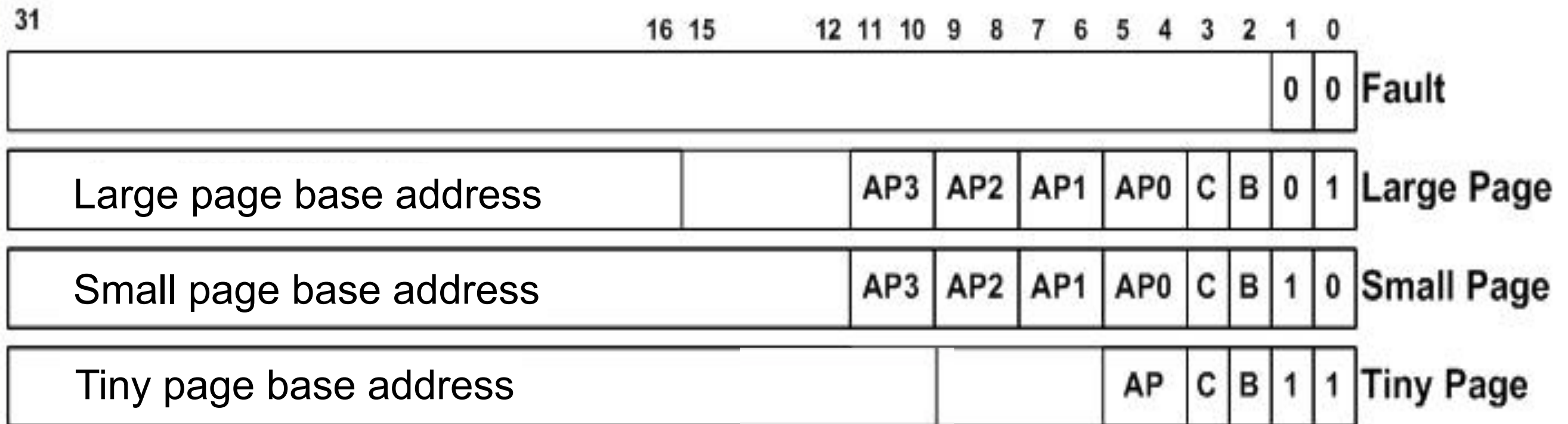First level translation table (4096 entries)

Physical address for sections (1 MB)

Virtual address		First level table										Physical address
0xFFF 00000		0xFFF		AP	DOMAIN	1	C	B	1	0		0xFFF 00000
0xFFE 00000		0xFFE		AP	DOMAIN	1	C	B	1	0		0xFFE 00000
0xFFD 00000		0xFFE		AP	DOMAIN	1	C	B	1	0		0xFFD 00000
0xFFC 00000		0xFFA		AP	DOMAIN	1	C	B	1	0		0xFFC 00000
0xFFB 00000									0	0		0xFFB 00000
0xFFA 00000									0	0		0xFFA 00000

Virtual address		First level table										Physical address
0x007 00000		0x005		AP	DOMAIN	1	C	B	1	0		0x007 00000
0x006 00000		0x002		AP	DOMAIN	1	C	B	1	0		0x006 00000
0x005 00000									0	0		0x005 00000
0x004 00000		Fine page table base addr			DOMAIN	1			1	1		0x004 00000
0x003 00000									0	0		0x003 00000
0x002 00000		Coarse page table base addr			DOMAIN	1			0	1		0x002 00000
0x001 00000		0x001		AP	DOMAIN	1	C	B	1	0		0x001 00000
0x000 00000		0x000		AP	DOMAIN	1	C	B	1	0		0x000 00000

Second level translation table reference

Level 1 Descriptor

Level 2 Descriptor

31		16 15		12 11 10 9 8 7 6 5 4 3 2 1 0									
											0	0	Fault
Large page base address				AP3	AP2	AP1	AP0	C	B	0	1		Large Page
Small page base address			AP3	AP2	AP1	AP0	C	B	1	0			Small Page
Tiny page base address						AP	C	B	1	1			Tiny Page

Caching and Write Buffer Control

- Caching or write buffering can be configured for each section/page
  - Cacheable bit
  - Bufferable bit
- When a page needs to be configured as NON-CACHEABLE/ NON-BUFFERABLE?
- How to control in page table

C	B	Meaning	Cache write operation
0	0	Non-cacheable, non-bufferable	
0	1	Non-cacheable, bufferable	
1	0	Cacheable, non-bufferable	Write-through Cache
1	1	Cacheable, bufferable	Write-back Cache

ESL
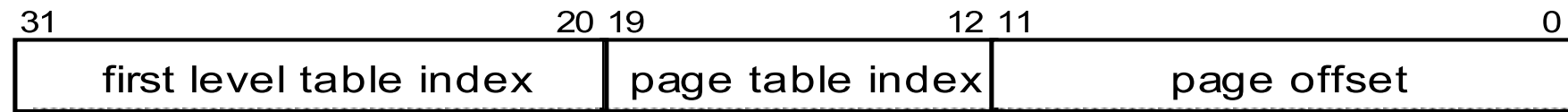Kookmin Univ. Embedded Systems Lab
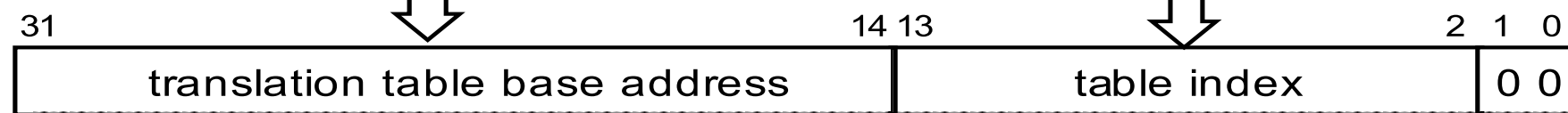
First-Level Translation
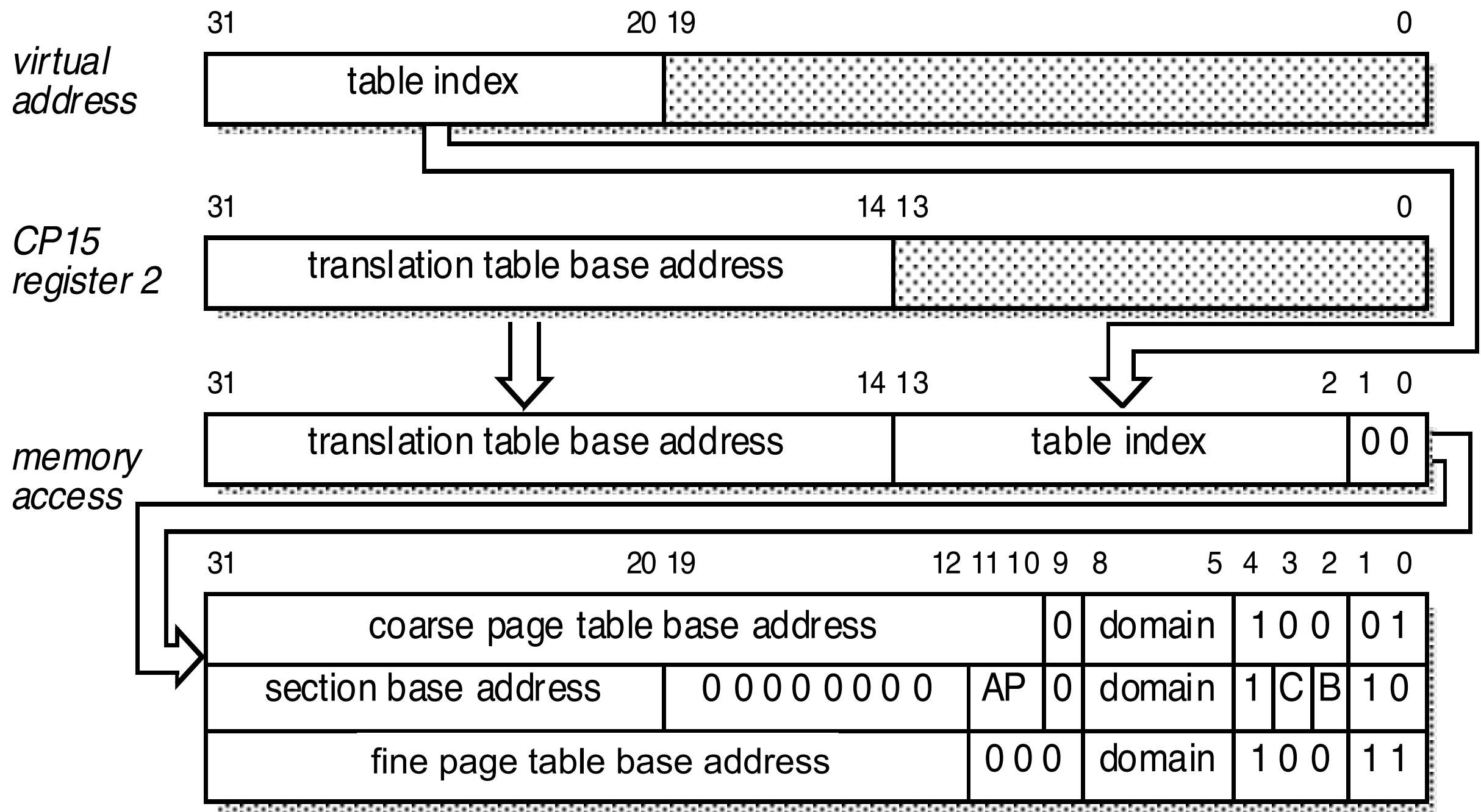
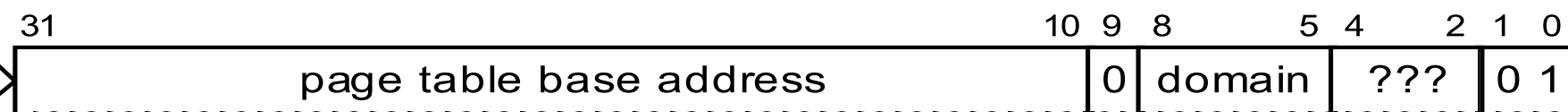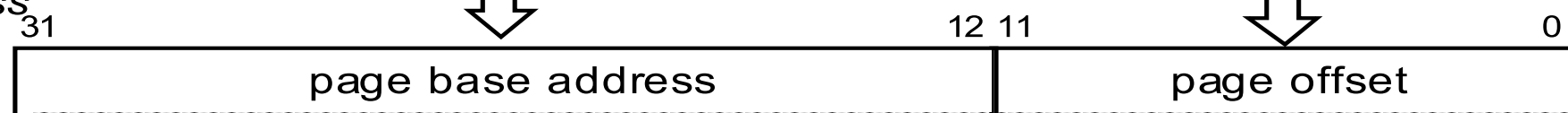# Section Translation Sequence
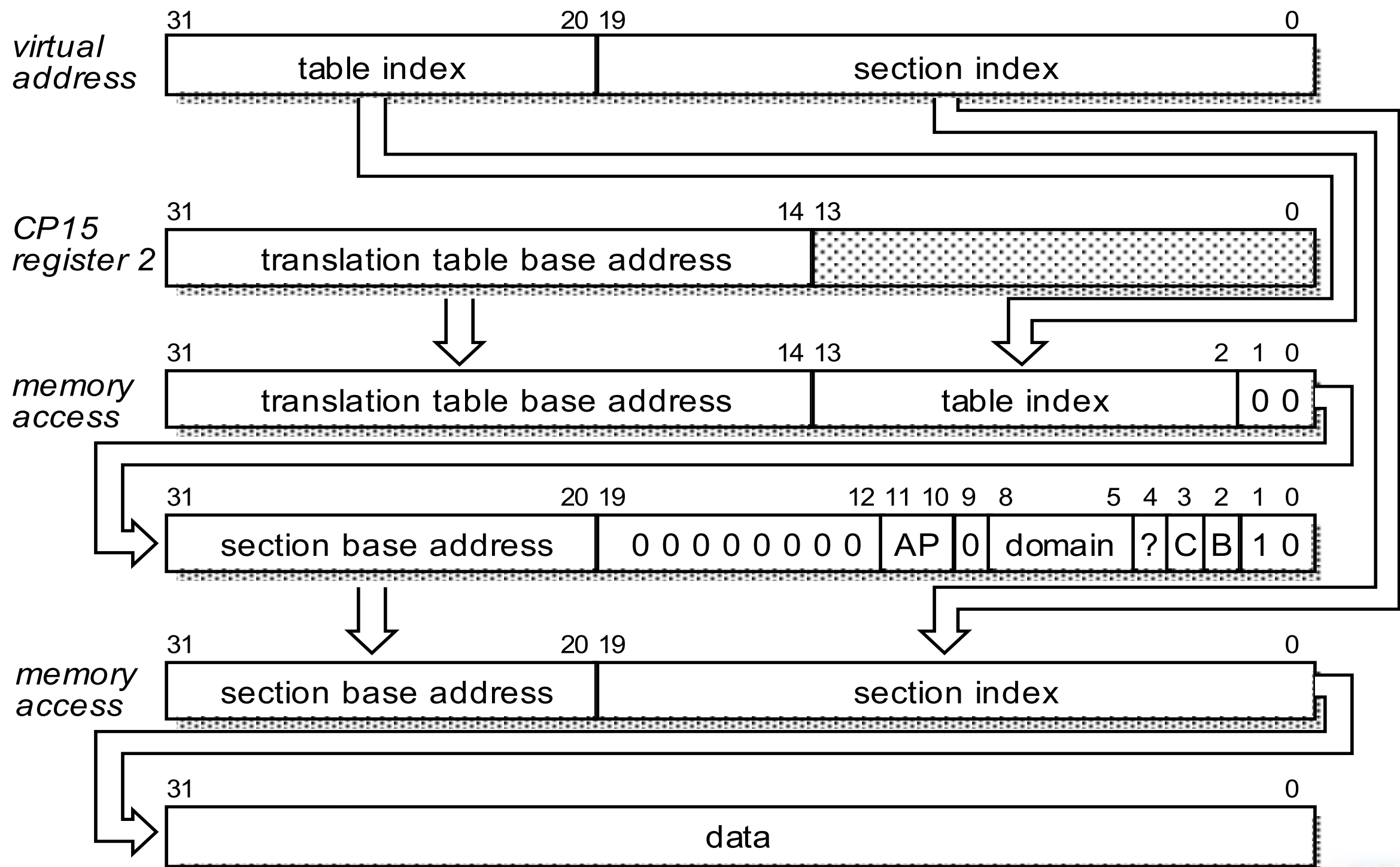
Small Page Translation

virtual address

31	20 19	12 11	0
first level table index	page table index	page offset	

CP15 register 2

31	14 13	0
translation table base address		

31	14 13	2 1 0
translation table base address	table index	0 0

31	10 9 8	5 4	2 1 0
page table base address	0	domain	???	0 1

memory access

31	10 9	2 1 0
page table base address	page table index	0 0

31	12 11 10 9 8 7 6 5 4 3 2 1 0
page base address	AP3 AP2 AP1 AP0 C B 1 0

memory access

31	12 11	0
page base address	page offset	

31	0
data	

memory access

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