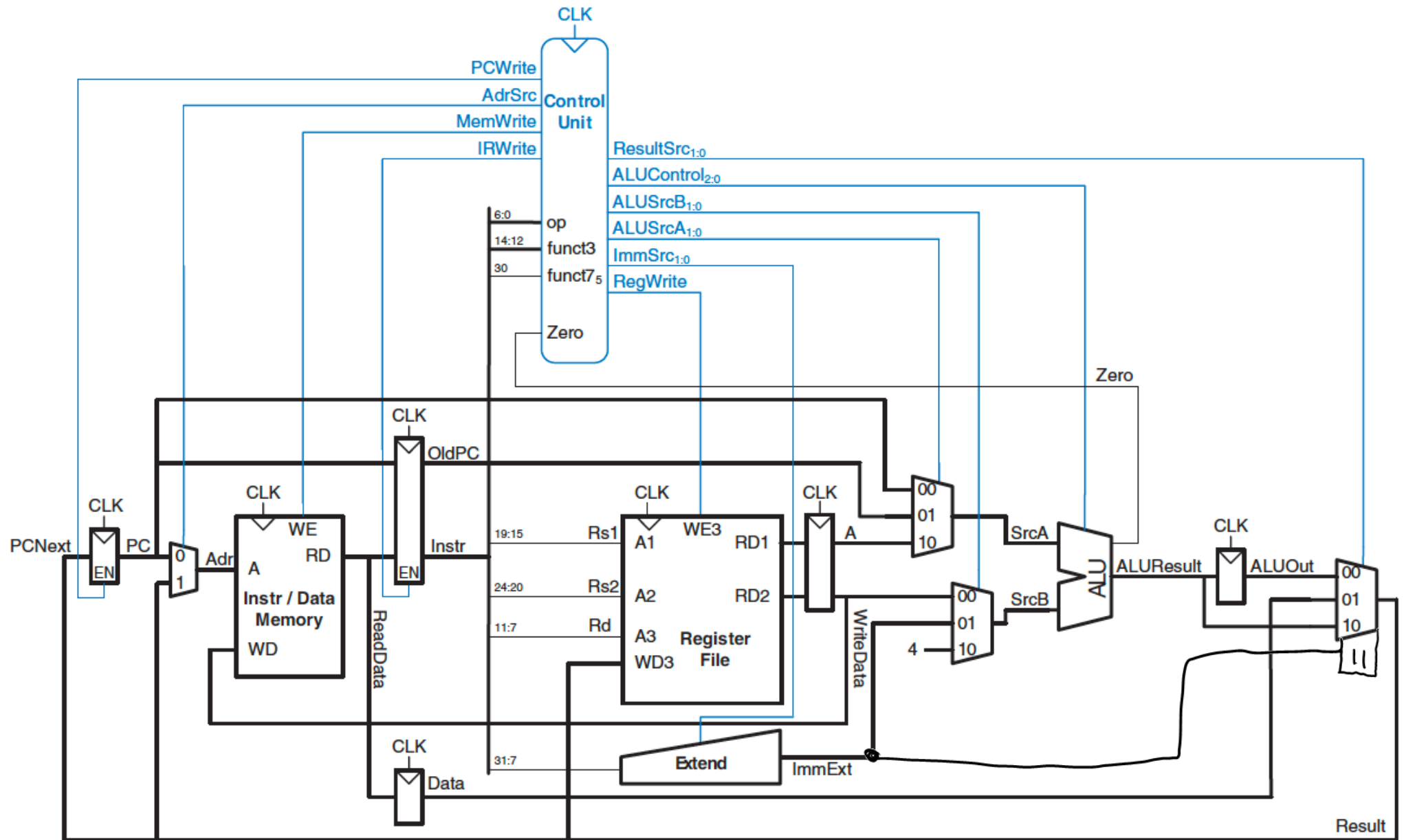
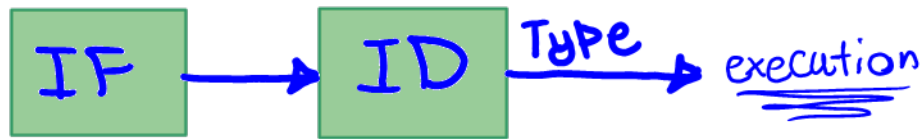


# RISC-V Multi-Cycle Data-Path

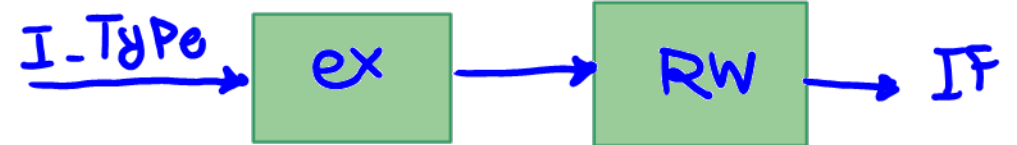


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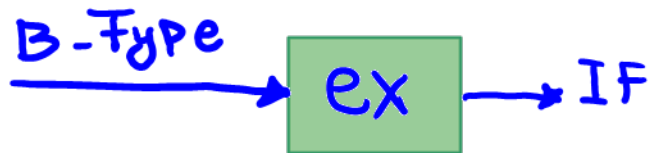
IRwrite  
 ALUSrcA=00  
 ALUSrcB=10  
 PCen  
 ALUOp=+  
 resultsrc=10

ALUSrcA=01  
 ALUSrcB=01  
 ALUOp=+  
 Imm-src=B-Type

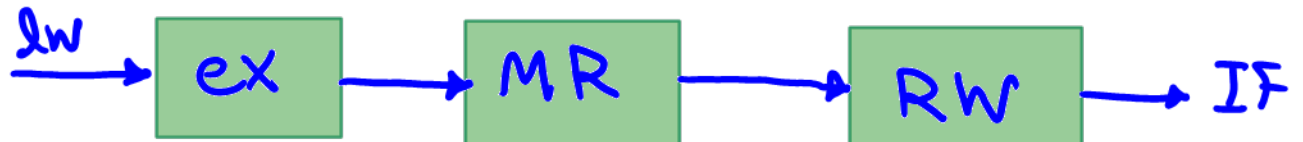


ALUOp=\*  
 ALUSrcA=10  
 ALUSrcB=01  
 Imm-src=I-type

reg-write  
 Resultsrc=00



PCen=\*  
 Resultsrc=00  
 ALUSrcA=10  
 ALUSrcB=00  
 ALUOp=-



ALUOp=+  
 ALUSrcA=10  
 ALUSrcB=01  
 Imm-src=I-type

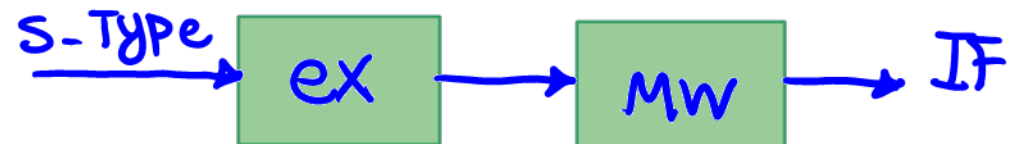
resultsrc=0  
 adrSrc

Resultsrc=01  
 Regwrite



ALUOp=\*  
 ALUSrcA=10  
 ALUSrcB=00

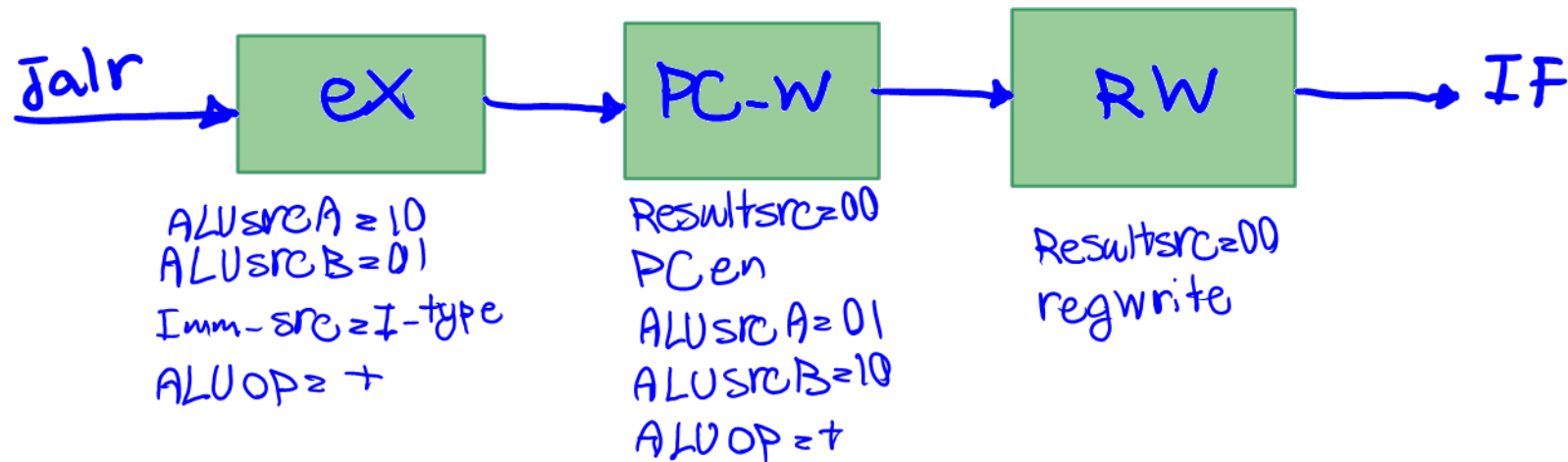
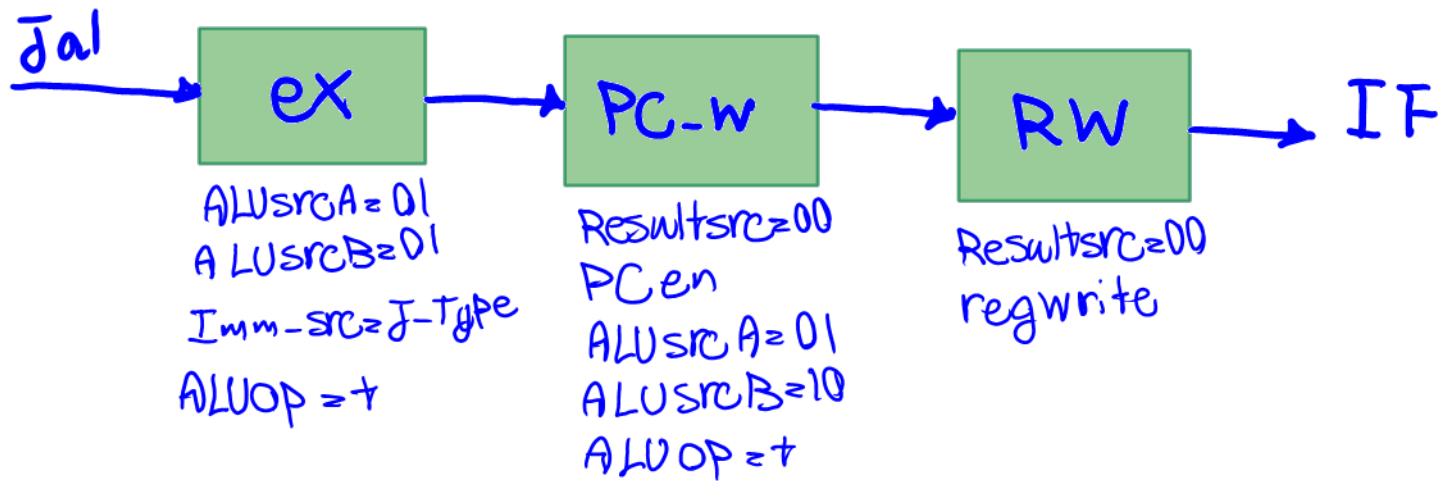
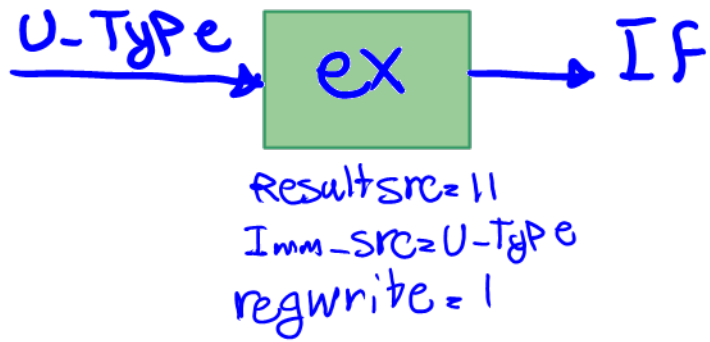
regwrite  
 Resultsrc=00



ALUOp=+  
 ALUSrcA=10  
 ALUSrcB=01  
 Imm-src=S-type

memwrite  
 adrSrc  
 Resultsrc=00

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