Reversible logic synthesis and RevKit

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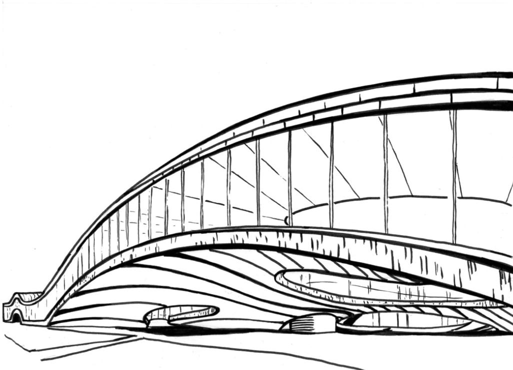

Introduction and background

Reversible logic synthesis

Introduction into RevKit

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Introduction into RevKit

Quantum computing is getting real

- 17-qubit quantum computer from IBM based on superconducting qubits (16-qubit version available via cloud service)
- 9-qubit quantum computer from Google based on superconducting circuits
- 5-qubit quantum computer at University of Maryland based on ion traps
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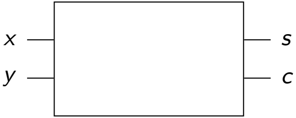
- "Quantum supremacy" experiment may be possible with $\approx$50 qubits (45-qubit simulation has been performed classically)
- Smallest practical problems require $\approx$100 (logical) qubits

Challenges in logic synthesis for quantum computing

1. Quantum computers process qubits not bits

Classical half-adder



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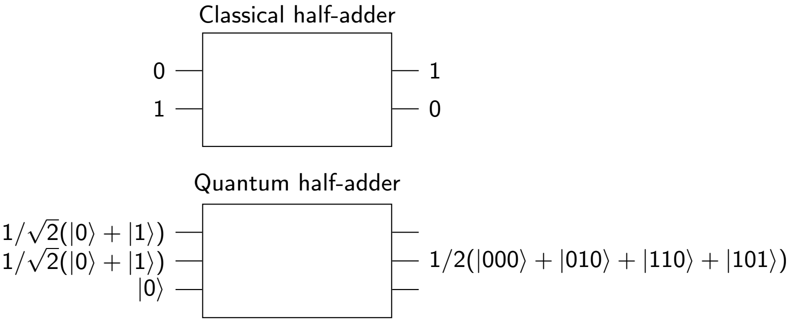

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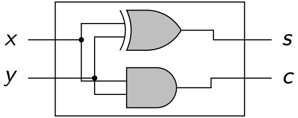

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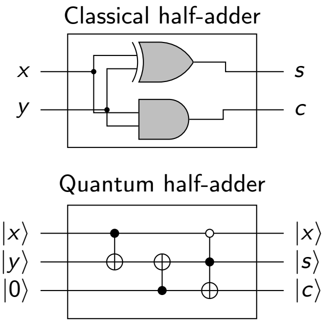

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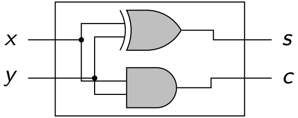

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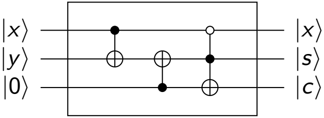

Challenges in logic synthesis for quantum computing

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4. Circuit is not allowed to produce intermediate results, called garbage qubits

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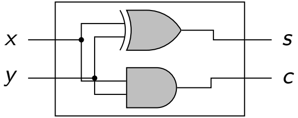

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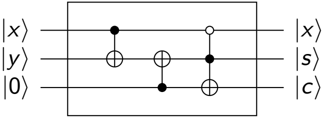
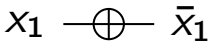
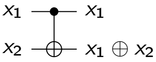


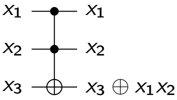
Reversible gates



NOT

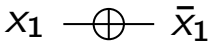


CNOT



Toffoli

Reversible gates



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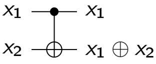

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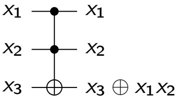

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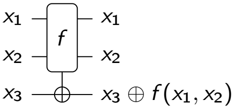
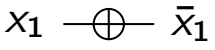


Single-target

Reversible gates



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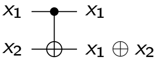

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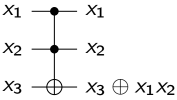

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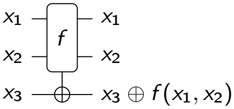

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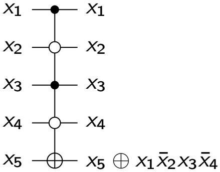
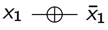


Multiple-controlled Toffoli

Reversible gates



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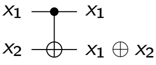

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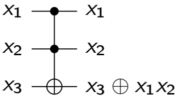

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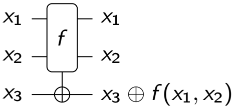

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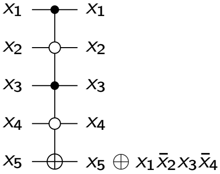

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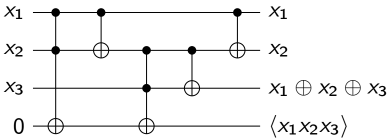

Full adder

Quantum gates

- Qubit is vector $|\varphi\rangle = \binom{\alpha}{\beta}$ with $|\alpha^2| + |\beta^2| = 1$.
- Classical 0 is $|0\rangle = \binom{1}{0}$; Classical 1 is $|1\rangle = \binom{0}{1}$

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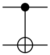
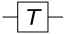
$|\varphi_1\rangle$, $|\varphi_2\rangle$  $\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} |\varphi_1\varphi_2\rangle$

CNOT

$|\varphi\rangle$  $\frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} |\varphi\rangle$

Hadamard

$|\varphi\rangle$  $\begin{pmatrix} 1 & 0 \\ 0 & e^{\frac{i\pi}{4}} \end{pmatrix} |\varphi\rangle$

T

Composing quantum gates

- Applying a quantum gate to a quantum state (matrix-vector multiplication)

$$|\varphi\rangle = \left(\begin{smallmatrix}\alpha \\ \beta\end{smallmatrix}\right) \;-\!\boxed{U}\!-\; U|\varphi\rangle$$

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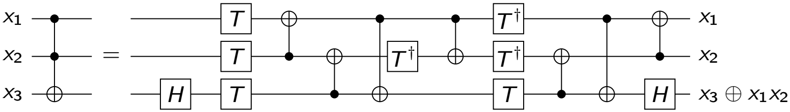
- Applying quantum gates in parallel (Kronecker product)

$$\left.\begin{array}{l} |\varphi_1\rangle = \begin{pmatrix} \alpha_1 \\ \beta_1 \end{pmatrix} \;-\!\boxed{U_1}\!- \\ |\varphi_2\rangle = \begin{pmatrix} \alpha_2 \\ \beta_2 \end{pmatrix} \;-\!\boxed{U_2}\!- \end{array}\right\} (U_1 \otimes U_2)|\varphi_1\varphi_2\rangle$$

Mapping Toffoli gates



Clifford+T circuit [Amy *et al.*, *TCAD* **32**, 2013]

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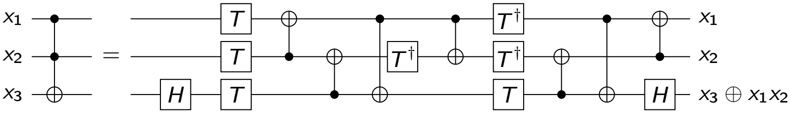

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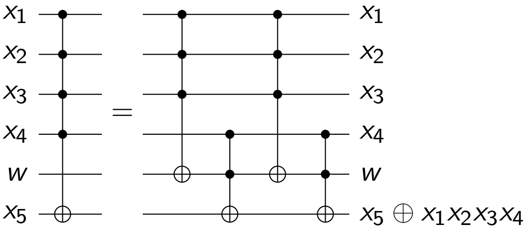

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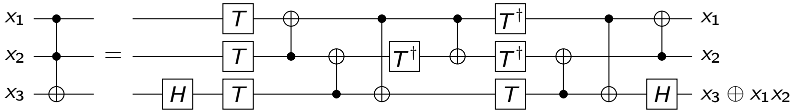

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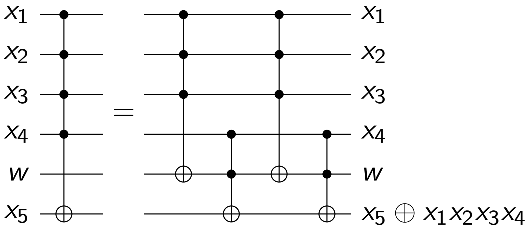

Costs are number of qubits and number of T gates

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- Implement core functionality in C++ and expose it via CLI commands

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- More details: msoeken.github.io/revkit.html

RevKit [Generalities]

- RevKit is commands plus stores
- Stores for each relevant data structure: e.g., reversible circuits, reversible truth tables, AND-inverter graphs, binary decision diagrams, . . .
- Stores can contain several instances, commands work on current element

```
revkit> read_real -s "t a b c, f b a c"
revkit> store -c
[i] circuits in store:
  *  0: 3 lines, 2 gates
revkit> tof
revkit> ps -c
Lines:        3
Gates:        4
T-count:      14
Logic qubits: 4
revkit> write_liquid file.fs
```

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Reversible logic synthesis

Introduction into RevKit

Reversible logic synthesis

$$\text{Boolean function} \xrightarrow[\text{embedding}]{} \text{Rev. function} \xrightarrow[\text{synthesis}]{} \text{Rev. circuit}$$

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Embedding of irreversible functions

c	x	y	c	s
	0	0	0	0
	0	1	0	1
	1	0	0	1
	1	1	1	0

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- Add additional outputs to disambiguate duplicate output pattern, preferably inputs
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- Optional: assign output pattern to new input pattern
- Upper bound: Number of original inputs + number of original outputs (all inputs are preserved)
- Computing whether optimum embedding is possible with ℓ additional lines is coNP-hard

Reversible synthesis classification

	line opt.	*gate opt.*	**nonreversible func.**	**reversible func.**
functional	✔	✔		SAT-based Enumerative
functional	✔	✘		Transformation-based Cycle-based Decomposition-based Metaheuristic Greedy
structural	✘	✘	ESOP-based Hierarchical Building block	

SAT-based exact synthesis

- **Idea:** Solve question *"does there exist a reversible circuit realizing f with r gates?"* as SAT problem

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RevKit: `exs`

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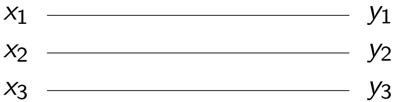
Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	111
001	000
010	110
011	100
100	010
101	001
110	011
111	101



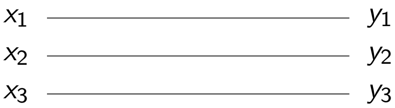
- Apply gates adjust output pattern with input pattern
- By visiting input patterns in numeric order, and by only using positive controlled Toffoli gates, it is ensured that no previous patterns are modified

RevKit: `tbs`

D. Michael Miller, Dmitri Maslov, Gerhard W. Dueck: A transformation based algorithm for reversible logic synthesis, *DAC* **40** (2003), 318–323.

Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	111
001	000
010	110
011	100
100	010
101	001
110	011
111	101



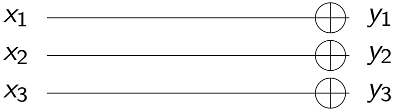
- Apply gates adjust output pattern with input pattern
- By visiting input patterns in numeric order, and by only using positive controlled Toffoli gates, it is ensured that no previous patterns are modified

RevKit: `tbs`

D. Michael Miller, Dmitri Maslov, Gerhard W. Dueck: A transformation based algorithm for reversible logic synthesis, *DAC* **40** (2003), 318–323.

Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	000
001	111
010	001
011	011
100	101
101	110
110	100
111	010



- Apply gates adjust output pattern with input pattern
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RevKit: `tbs`

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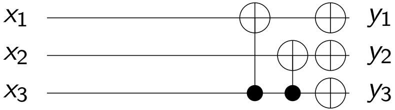
Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	000
001	001
010	111
011	101
100	011
101	110
110	100
111	010



- Apply gates adjust output pattern with input pattern
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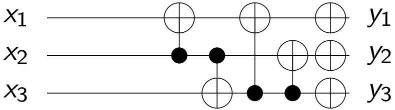
Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	000
001	001
010	010
011	101
100	110
101	011
110	100
111	111



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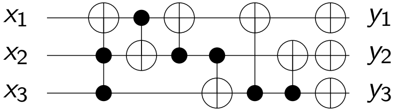
RevKit: `tbs`

Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	000
001	001
010	010
011	011
100	100
101	111
110	110
111	101



- Apply gates adjust output pattern with input pattern
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RevKit: `tbs`

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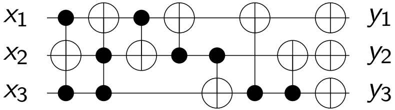
Explicit transformation-based synthesis

$x_1x_2x_3$	$y_1y_2y_3$
000	000
001	001
010	010
011	011
100	100
101	101
110	110
111	111



- Apply gates adjust output pattern with input pattern
- By visiting input patterns in numeric order, and by only using positive controlled Toffoli gates, it is ensured that no previous patterns are modified

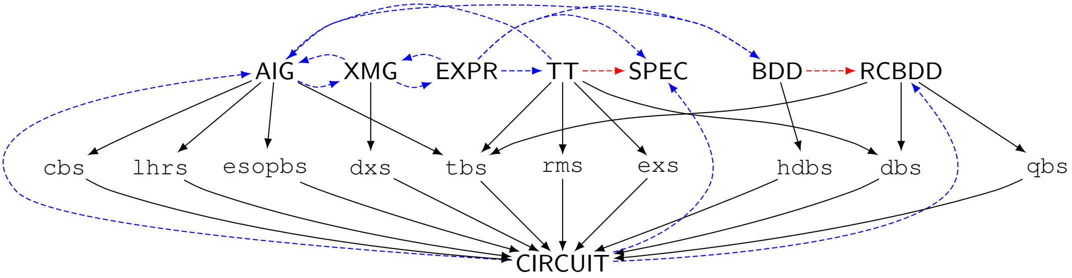
RevKit: `tbs`

D. Michael Miller, Dmitri Maslov, Gerhard W. Dueck: A transformation based algorithm for reversible logic synthesis, *DAC* **40** (2003), 318–323.

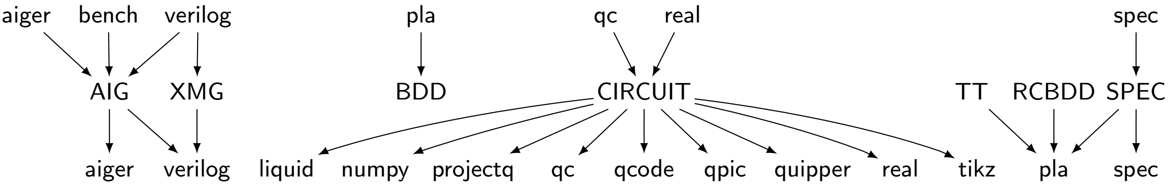
RevKit [Synthesis commands]

	line opt.	*gate opt.*	**nonreversible func.**	**reversible func.**
functional	✔	✔		SAT-based `exs` Enumerative
functional	✔	✘		Transformation-based `tbs`, `rms`, `qbs` Cycle-based `cyclebs` Decomposition-based `dbs` Metaheuristic Greedy
structural	✘	✘	ESOP-based `esopbs` Hierarchical `cbs`, `dxs`, `hdbs`, `lhrs` Building block	

RevKit [Synthesis and formats]



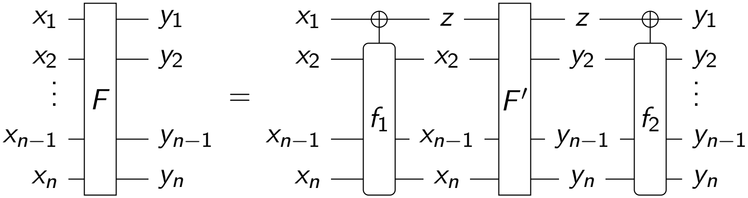
RevKit [File formats]



RevKit [Functional synthesis]

```
revkit> revgen --hwb 6
revkit> tbs
revkit> dbs -n
revkit> store -c
[i] circuits in store:
     0: 6 lines, 141 gates
  *  1: 6 lines, 89 gates
revkit> rec
[i] circuits are equivalent
revkit> reverse
revkit> concat -n
revkit> store -c
[i] circuits in store:
     0: 6 lines, 141 gates
     1: 6 lines, 89 gates
  *  2: 6 lines, 230 gates
revkit> is_identity
[i] circuit represents the identity function
```

Decomposition-based synthesis: idea

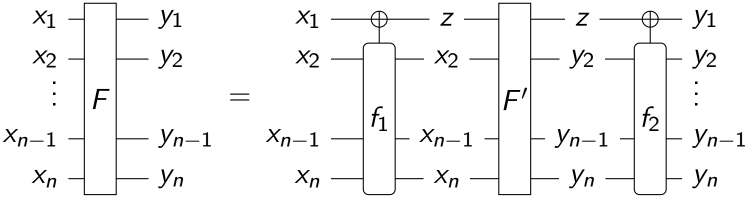


- Every reversible function can be decomposed into three reversible sub-functions $\mathrm{T}_{f_1}(X \setminus \{x_i\}, x_i)$, F', $\mathrm{T}_{f_2}(X \setminus \{x_i\}, x_i)$, where F' is a reversible function that does not change in x_i, for all i

RevKit: `dbs`

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: idea



- Every reversible function can be decomposed into three reversible sub-functions $\mathrm{T}_{f_1}(X \setminus \{x_i\}, x_i)$, F', $\mathrm{T}_{f_2}(X \setminus \{x_i\}, x_i)$, where F' is a reversible function that does not change in x_i, for all i
- Recursive application of this procedure on B in order $i = 1, 2, \ldots, n-1, n$, yields a reversible circuit with $2n-1$ gates, where the targets are aligned in a V-shape

RevKit: `dbs`

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3					y_1	y_2	y_3
0	0	0					0	0	0
0	0	1					0	0	1
0	1	0					0	1	0
0	1	1					1	1	0
1	0	0					1	1	1
1	0	1					0	1	1
1	1	0					1	0	1
1	1	1					1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3							y_1	y_2	y_3
0	0	0	0	0			0	0	0	0	0
0	0	1	0	1			0	1	0	0	1
0	1	0	1	0			1	0	0	1	0
0	1	1	1	1			1	0	1	1	0
1	0	0	0	0			1	1	1	1	1
1	0	1	0	1			1	1	0	1	1
1	1	0	1	0			0	1	1	0	1
1	1	1	1	1			0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3								y_1	y_2	y_3
0	0	0	0	0	0			0	0	0	0	0
0	0	1		0	1			0	1	0	0	1
0	1	0		1	0			1	0	0	1	0
0	1	1		1	1			1	0	1	1	0
1	0	0		0	0			1	1	1	1	1
1	0	1		0	1			1	1	0	1	1
1	1	0		1	0			0	1	1	0	1
1	1	1		1	1			0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1		0	1								0	1	0	0	1
0	1	0		1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0								1	1	1	1	1
1	0	1		0	1								1	1	0	1	1
1	1	0		1	0								0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1		0	1								0	1	0	0	1
0	1	0		1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1		0	1								1	1	0	1	1
1	1	0		1	0								0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1		0	1				0	1	0	0	1
0	1	0		1	0				1	0	0	1	0
0	1	1		1	1				1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1		0	1			0	1	1	0	1	1
1	1	0		1	0				0	1	1	0	1
1	1	1		1	1				0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1		0	1				0	1	0	0	1
0	1	0		1	0				1	0	0	1	0
0	1	1		1	1				1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0		1	0				0	1	1	0	1
1	1	1		1	1				0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1	1	0	1				0	1	0	0	1
0	1	0		1	0				1	0	0	1	0
0	1	1		1	1				1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0		1	0				0	1	1	0	1
1	1	1		1	1				0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0		1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0		1	0								0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0		1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0		1	0							0	0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0		1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0	0	1	0							0	0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0	1	1	0								1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0	0	1	0							0	0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0	1	1	0							1	1	0	0	1	0
0	1	1		1	1								1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0	0	1	0							0	0	1	1	0	1
1	1	1		1	1								0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1	1	0	1			1	0	1	0	0	1
0	1	0	1	1	0			1	1	0	0	1	0
0	1	1		1	1			0	1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0	0	1	0			0	0	1	1	0	1
1	1	1		1	1				0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1	1	0	1			1	0	1	0	0	1
0	1	0	1	1	0			1	1	0	0	1	0
0	1	1	0	1	1			0	1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0	0	1	0			0	0	1	1	0	1
1	1	1		1	1				0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0								0	0	0	0	0
0	0	1	1	0	1							1	0	1	0	0	1
0	1	0	1	1	0							1	1	0	0	1	0
0	1	1	0	1	1							0	1	0	1	1	0
1	0	0	1	0	0							1	1	1	1	1	1
1	0	1	0	0	1							0	1	1	0	1	1
1	1	0	0	1	0							0	0	1	1	0	1
1	1	1	1	1	1								0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0				0	0	0	0	0
0	0	1	1	0	1			1	0	1	0	0	1
0	1	0	1	1	0			1	1	0	0	1	0
0	1	1	0	1	1			0	1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0	0	1	0			0	0	1	1	0	1
1	1	1	1	1	1			1	0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3									y_1	y_2	y_3
0	0	0	0	0	0			0	0	0	0	0	0
0	0	1	1	0	1			1	0	1	0	0	1
0	1	0	1	1	0			1	1	0	0	1	0
0	1	1	0	1	1			0	1	0	1	1	0
1	0	0	1	0	0			1	1	1	1	1	1
1	0	1	0	0	1			0	1	1	0	1	1
1	1	0	0	1	0			0	0	1	1	0	1
1	1	1	1	1	1			1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3											y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	1	1	1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	1	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	0	0	0	1	0	1	1	0
1	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1
1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0		1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0		1	0		1	0	1	1	0	1	1
1	1	0	0	1	0	0		0	0		1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

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Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0		1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0		1	0		1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0		1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0		1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0		1	0		1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0		1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0		1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0		1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0		0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1		1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1		1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1		0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1		0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1		0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1		0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1	1	0	1		1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1		1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Decomposition-based synthesis: example

x_1	x_2	x_3													y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0

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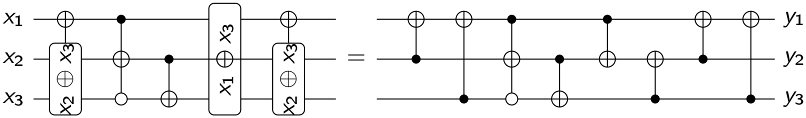
Decomposition-based synthesis: example

x_1	x_2	x_3														y_1	y_2	y_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0	0	1
0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0



A. De Vos, Y. Van Rentergem: Young subgroups for reversible computers, *Adv. in Math. of Comm.* 2 (2008), 183–200.

Reversible synthesis classification

	line opt.	*gate opt.*	**nonreversible func.**	**reversible func.**
functional	✔	✔		SAT-based Enumerative
functional	✔	✘		Transformation-based Cycle-based Decomposition-based Metaheuristic Greedy
structural	✘	✘	ESOP-based Hierarchical Building block	

ESOP-based synthesis

$$
\begin{aligned}
f(x_1, x_2, x_3, x_4) &= [(x_4 x_3 x_2 x_1)_2 \text{ is prime}] \\
&= \bar{x}_4 \bar{x}_3 x_2 \lor \bar{x}_4 x_3 x_1 \lor x_4 \bar{x}_3 x_2 x_1 \lor x_4 x_3 \bar{x}_2 x_1
\end{aligned}
$$

RevKit: `esopbs`

K. Fazel, M.A. Thornton, and J.E. Rice: ESOP-based Toffoli Gate Cascade Generation, *PACRIM* (2007)

ESOP-based synthesis

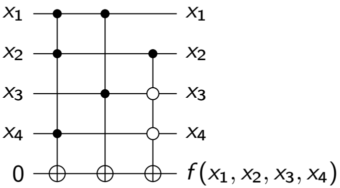
$$
\begin{aligned}
f(x_1, x_2, x_3, x_4) &= [(x_4x_3x_2x_1)_2 \text{ is prime}] \\
&= \bar{x}_4\bar{x}_3x_2 \lor \bar{x}_4x_3x_1 \lor x_4\bar{x}_3x_2x_1 \lor x_4x_3\bar{x}_2x_1 \\
&= x_4x_2x_1 \oplus x_3x_1 \oplus \bar{x}_4\bar{x}_3x_2
\end{aligned}
$$

RevKit: `esopbs`

K. Fazel, M.A. Thornton, and J.E. Rice: ESOP-based Toffoli Gate Cascade Generation, *PACRIM* (2007)

ESOP-based synthesis

$$f(x_1, x_2, x_3, x_4) = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$
$$= \bar{x}_4\bar{x}_3x_2 \lor \bar{x}_4x_3x_1 \lor x_4\bar{x}_3x_2x_1 \lor x_4x_3\bar{x}_2x_1$$
$$= x_4x_2x_1 \oplus x_3x_1 \oplus \bar{x}_4\bar{x}_3x_2$$

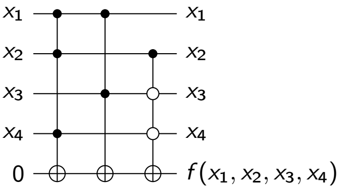


RevKit: `esopbs`

K. Fazel, M.A. Thornton, and J.E. Rice: ESOP-based Toffoli Gate Cascade Generation, *PACRIM* (2007)

ESOP-based synthesis

$$f(x_1,x_2,x_3,x_4) = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$
$$= \bar{x}_4\bar{x}_3x_2 \lor \bar{x}_4x_3x_1 \lor x_4\bar{x}_3x_2x_1 \lor x_4x_3\bar{x}_2x_1$$
$$= x_4x_2x_1 \oplus x_3x_1 \oplus \bar{x}_4\bar{x}_3x_2$$

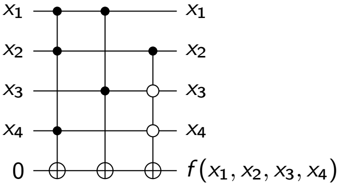


$$f_1 = [3 \mid (x_4x_3x_2x_1)_2]$$
$$= \bar{x}_1\bar{x}_2x_3 \oplus \bar{x}_1\bar{x}_4 \oplus x_1\bar{x}_3x_4 \oplus$$
$$x_1x_2x_4 \oplus x_2\bar{x}_3\bar{x}_4$$
$$f_2 = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$

RevKit: `esopbs`

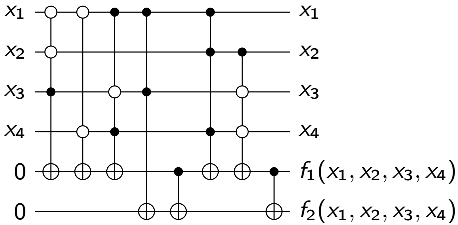
ESOP-based synthesis

$$f(x_1,x_2,x_3,x_4) = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$
$$= \bar{x}_4\bar{x}_3x_2 \vee \bar{x}_4x_3x_1 \vee x_4\bar{x}_3x_2x_1 \vee x_4x_3\bar{x}_2x_1$$
$$= x_4x_2x_1 \oplus x_3x_1 \oplus \bar{x}_4\bar{x}_3x_2$$



RevKit: `esopbs`

$$f_1 = [3 \mid (x_4x_3x_2x_1)_2]$$
$$= \bar{x}_1\bar{x}_2x_3 \oplus \bar{x}_1\bar{x}_4 \oplus x_1\bar{x}_3x_4 \oplus$$
$$x_1x_2x_4 \oplus x_2\bar{x}_3\bar{x}_4$$
$$f_2 = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$



RevKit [General commands]

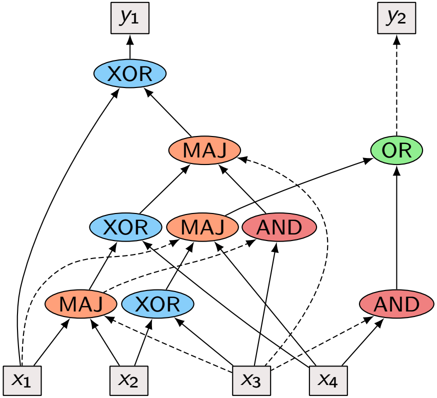
- **alias** — creates an alias
- **convert** — converts one store element into another
- **current** — changes current store element
- **help** — shows all commands
- **print** — prints current store element as ASCII
- **ps** — prints statistics about current store element
- **quit** — quits RevKit
- **set** — sets global (settings) variable
- **show** — generates visual representation of current store element (as DOT file)
- **store** — interact with the store

Reversible synthesis classification

	line opt.	*gate opt.*	**nonreversible func.**	**reversible func.**
functional	✔	✔		SAT-based Enumerative
functional	✔	✘		Transformation-based Cycle-based Decomposition-based Metaheuristic Greedy
structural	✘	✘	ESOP-based Hierarchical Building block	

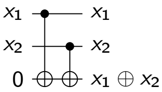
XMG-based synthesis

- XMG consists of **XOR** gates with 2 inputs and **MAJ** gates with 3 inputs
- MAJ gates with constant input can represent **AND** and **OR** gates
- Edges can be complemented (dashed lines in graph)

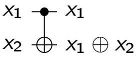


RevKit: `dxs`

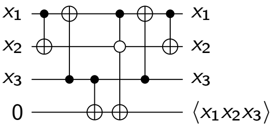
XMG-based synthesis



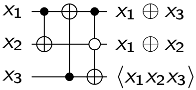
XOR



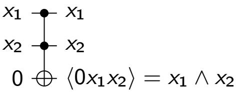
XOR (in-place)



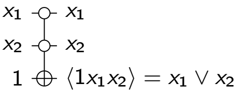
MAJ



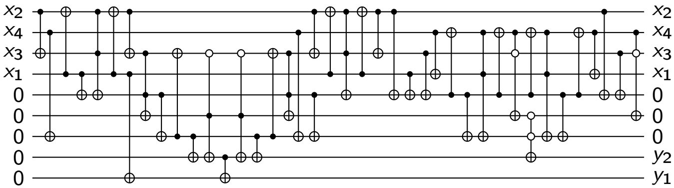
MAJ (in-place)



AND



OR



LUT-based hierarchical reversible synthesis

Goal: Automatically synthesizing large Boolean functions into Clifford+T networks of reasonable quality (qubits and T-count)

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

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RevKit: `lhrs`

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affects # T gates

RevKit: `lhrs`

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

 |

LUT mapping

- Realizing a logic function or logic circuit in terms of a k-LUT logic network
- A k-LUT is any Boolean function with at most k inputs
- One of the most effective methods used in logic synthesis

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

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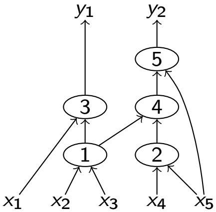
k-LUT network to reversible network



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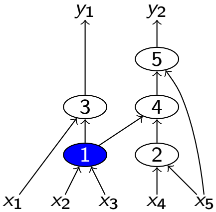
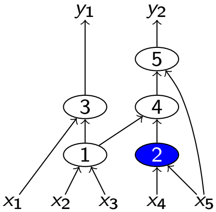


- ! k-LUT corresponds to k-controlled single-target gate

k-LUT network to reversible network



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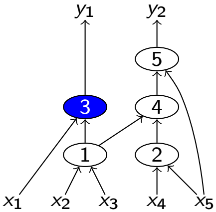

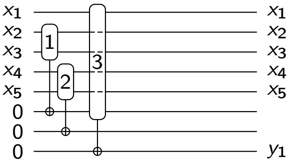

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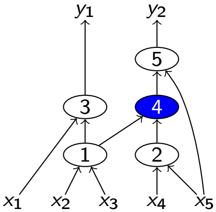

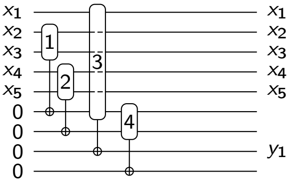

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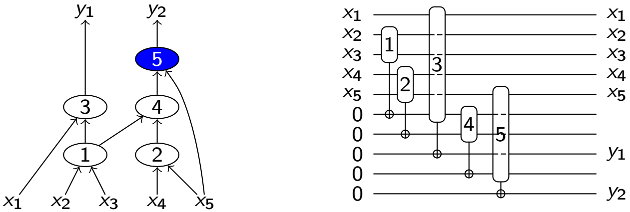

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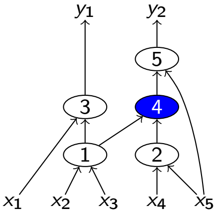

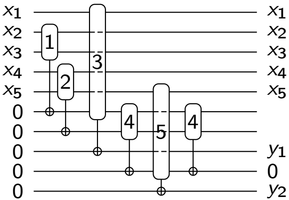

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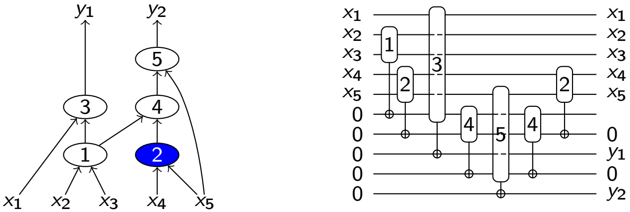
k-LUT network to reversible network



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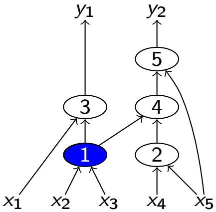

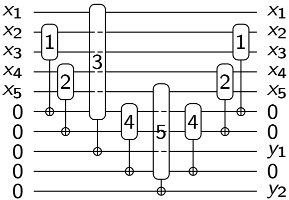

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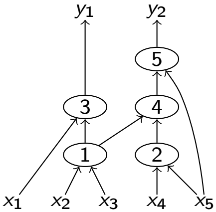

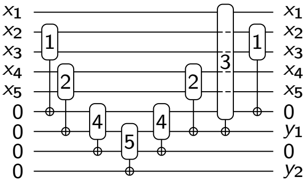

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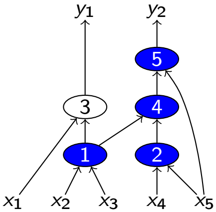
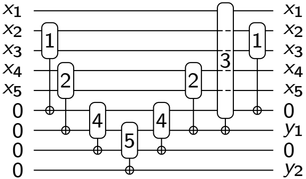
Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

k-LUT network to reversible network





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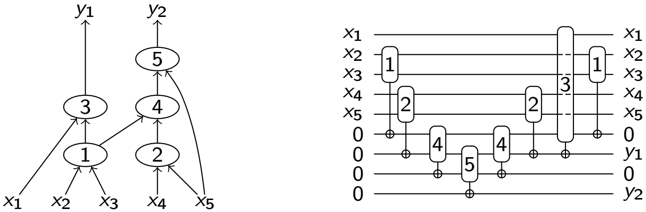
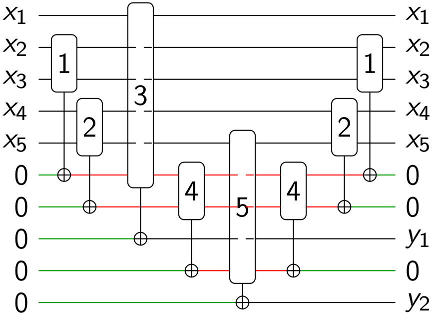


- ! k-LUT corresponds to k-controlled single-target gate
- ▸ non-output LUTs need to be uncomputed
- ▸ order of LUT traversal determines number of ancillas
- ▸ maximum output cone determines minimum number of ancillas
- ☺ fast mapping that generates a fixed-space skeleton for subnetwork synthesis

Single-target gate LUT mapping



- Mapping problem: Given a single-target gate $\mathrm{T}_f(X, x_t)$ (with control function f, control lines X, and target line x_t), a set of clean ancillas X_c, and a set of dirty ancillas X_d, find the best mapping into a Clifford+T network, such that all ancillas are restored to their original value.

Single-target gate mapping algorithms

- Direct

Single-target gate mapping algorithms

- Direct
  - Map each control function using ESOP based synthesis

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Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

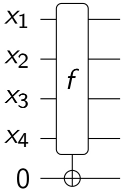
Single-target gate mapping algorithms

- Direct
  - Map each control function using ESOP based synthesis
  - Does not use ancillae
- LUT-based
  - Map control function into smaller LUT network
  - Map small LUTs into pre-computed optimum quantum circuits

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

Direct mapping

$$f(x_1, x_2, x_3, x_4) = [(x_4x_3x_2x_1)_2 \text{ is prime}]$$
$$= \bar{x}_4\bar{x}_3x_2 \vee \bar{x}_4x_3x_1 \vee x_4\bar{x}_3x_2x_1 \vee x_4x_3\bar{x}_2x_1$$



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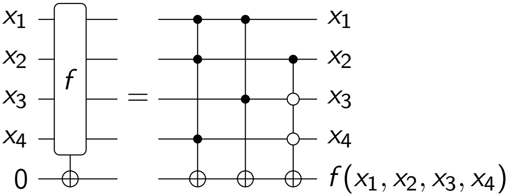
$$\begin{aligned} f(x_1, x_2, x_3, x_4) &= [(x_4x_3x_2x_1)_2 \text{ is prime}] \\ &= \bar{x}_4\bar{x}_3x_2 \lor \bar{x}_4x_3x_1 \lor x_4\bar{x}_3x_2x_1 \lor x_4x_3\bar{x}_2x_1 \\ &= x_4x_2x_1 \oplus x_3x_1 \oplus \bar{x}_4\bar{x}_3x_2 \end{aligned}$$



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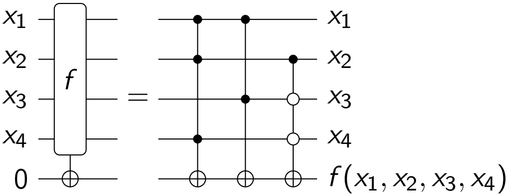
$$



- Each multiple-controlled Toffoli gate is mapped to Clifford+T

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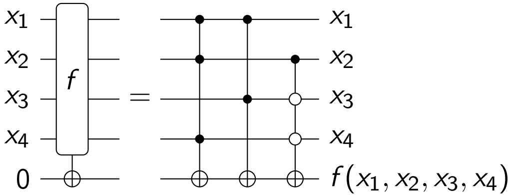
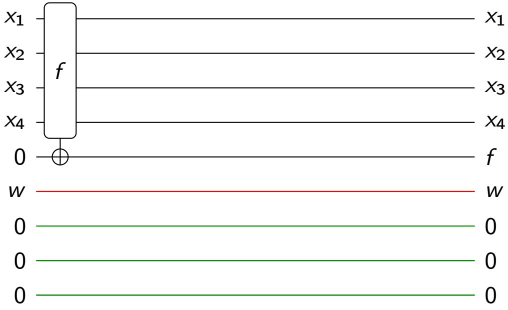


- Each multiple-controlled Toffoli gate is mapped to Clifford+T
- ☹ ESOP minimization tools (e.g., exorcism) optimize for cube count

LUT-based single-target gate mapping



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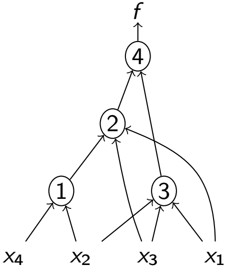

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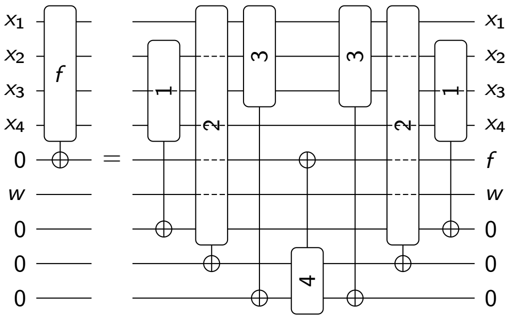
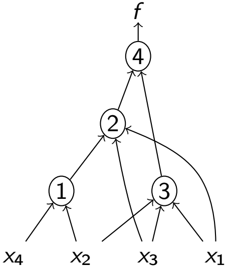
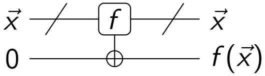




Affine transformations



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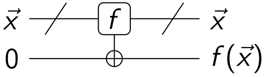
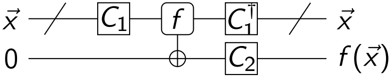
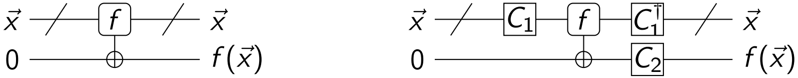




- Let C_1 and C_2 be circuits that only consist of NOT and CNOT gates

Affine transformations



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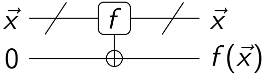
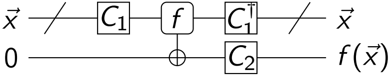
Affine transformations





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☺ Instead of 65 536 4-input functions we only need to consider 18

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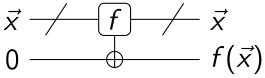

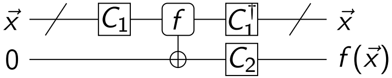

- Let C_1 and C_2 be circuits that only consist of NOT and CNOT gates
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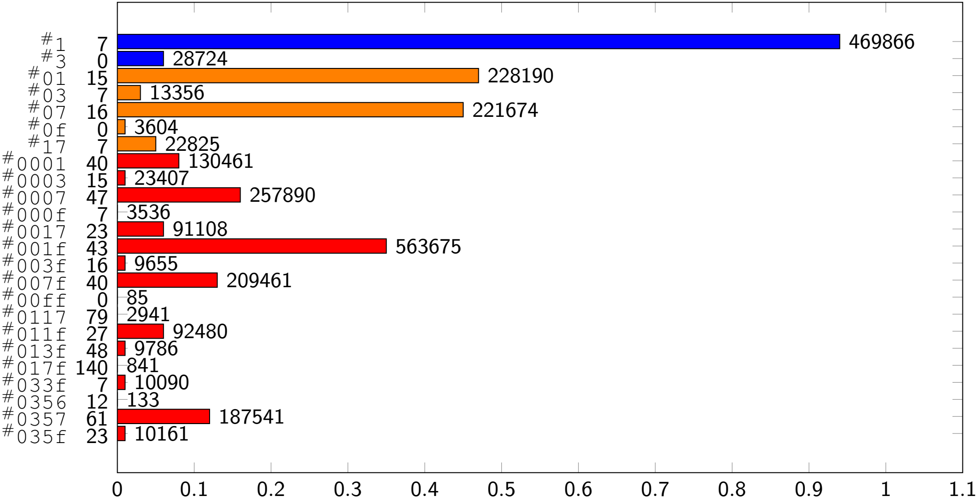
- ☺ Instead of 65 536 4-input functions we only need to consider 18
- ☺ Instead of 4 294 967 296 5-input functions we only need to consider 206

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

Circuits for affine equivalence classes



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The LHRS ecosystem

arxiv.org/abs/1706.02721

LHRS

- Mapping into LUTs
- Aligning LUTs as single-target gates
- Mapping single-target gates

Soeken, Roetteler, Wiebe, De Micheli: Hierarchical reversible logic synthesis using LUTs, *DAC* (2017), arXiv:1706.02721

The LHRS ecosystem

arxiv.org/abs/1706.02721

</> program

```
let gaussian a b c d x =
  let den = (x - b) * (x - b)
  let nom = -2.0f * c * c
  a * exp (den / nom)
```

LHRS

- Mapping into LUTs
- Aligning LUTs as single-target gates
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The LHRS ecosystem

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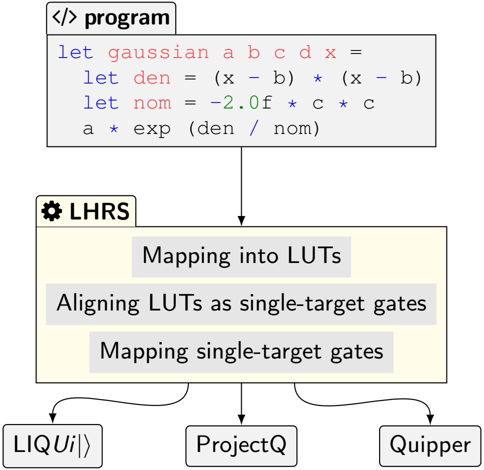

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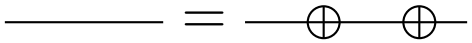
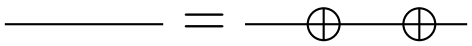
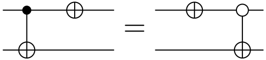
Circuit rewriting

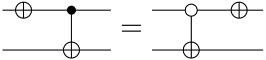


M. Soeken, M.K. Thomsen: White dots *do* matter: rewriting reversible logic circuits, *RC* **5**, (2013), 196–208

Circuit rewriting







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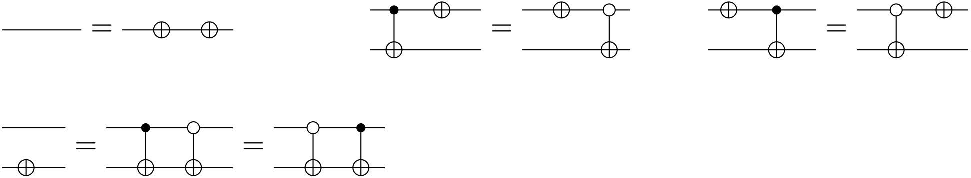

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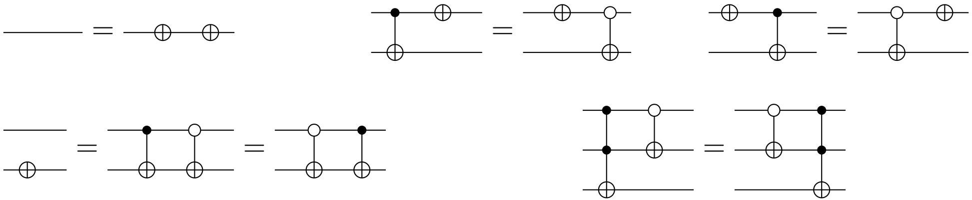

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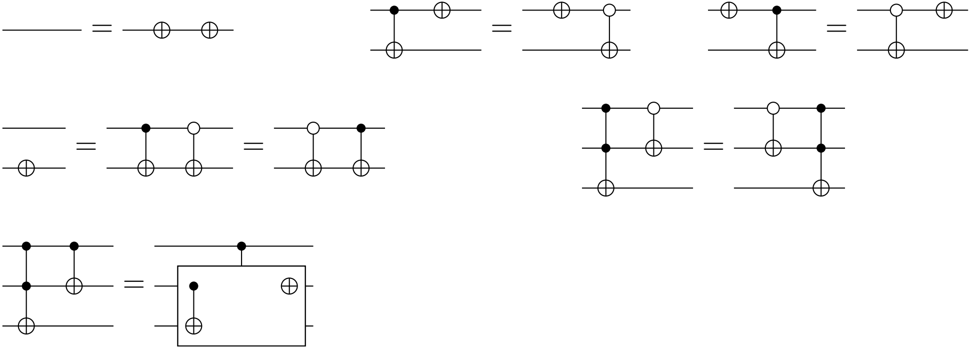

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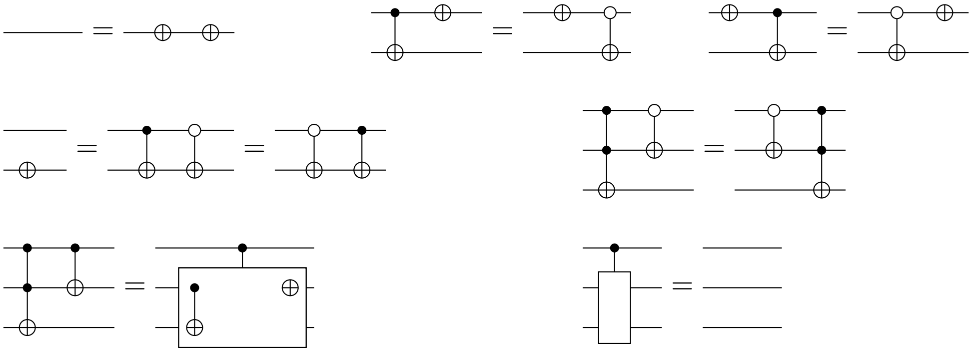

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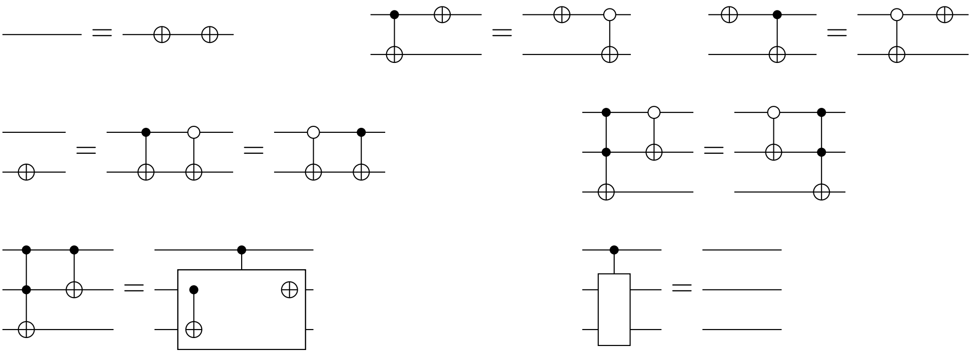

? Open problem: These six rules (plus SWAP rule) are complete, i.e., one can rewrite any circuit realizing some function into any other circuit realizing the same function

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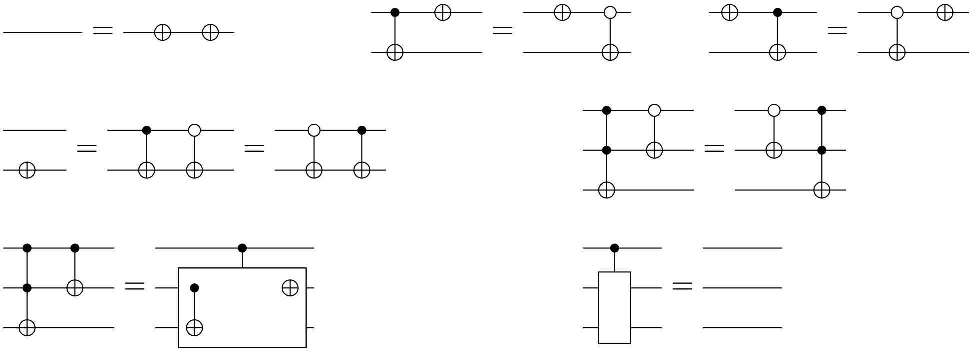

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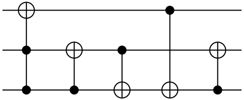
- Rule set has been extended to consider ancillae

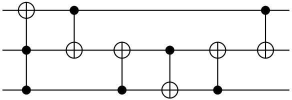
M. Soeken, M.K. Thomsen: White dots *do* matter: rewriting reversible logic circuits, *RC* 5, (2013), 196–208

Circuit rewriting: example

Circuit G_1



Circuit G_2



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Circuit rewriting: example

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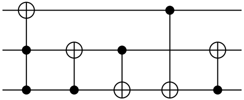
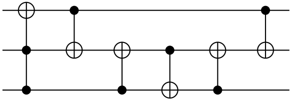


Circuit G_2



- Can be used for equivalence checking to check $G_1 \equiv G_2$
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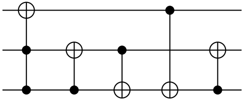
- Rewrite G to identity

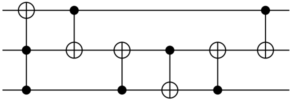
M. Soeken, M.K. Thomsen: White dots *do* matter: rewriting reversible logic circuits, *RC* 5, (2013), 196–208

Circuit rewriting: example

Circuit G_1



Circuit G_2



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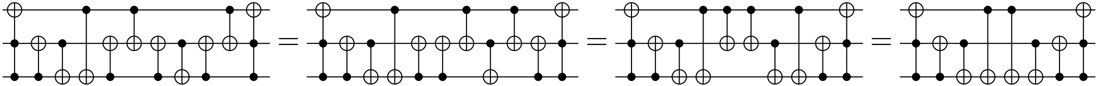
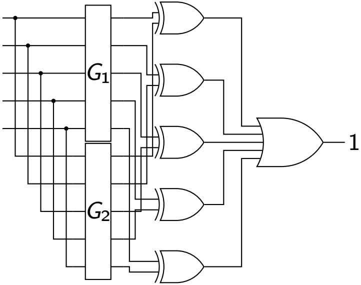


Equivalence checking of reversible circuits

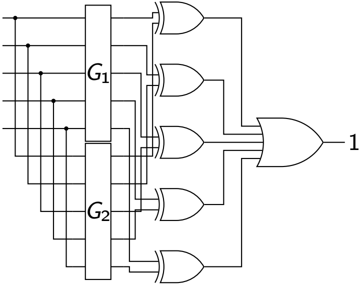
Conventional approach



Exploiting reversibility

Equivalence checking of reversible circuits

Conventional approach



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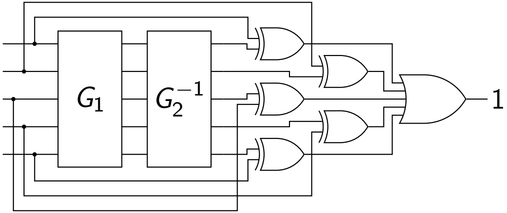
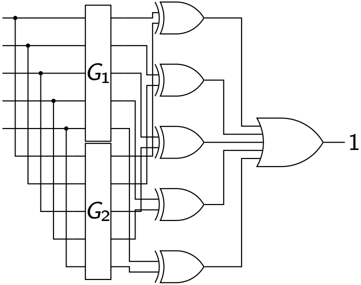


RevKit: `rec`

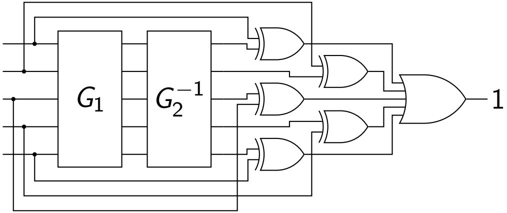
L.G. Amarù, P.-E. Gaillardon, R. Wille, and G. De Micheli: *DATE* 19 (2016)

Equivalence checking of reversible circuits

Conventional approach



Exploiting reversibility



RevKit: `rec`

- Circuit is translated into a SAT formula and solved with a SAT solver
- A satisfying solution is witnessing a counter-example
- Solvers with support for XOR clauses allow for more natural encoding and better runtimes

Introduction and background

Reversible logic synthesis

Introduction into RevKit

Reversible logic synthesis and RevKit

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