

6809 Instruction Set																						
Instruction	Mnemonic	Addressing Mode												Description	CC bit							
		Immediate			Direct			Indexed			Extended				Inherent			5	3	2	1	0
		Op	~	#	Op	~	#	Op	~	#	Op	~	#		Op	~	#	H	N	Z	V	C
ABX													3A	3	1	X = B+X (Unsigned)						
ADC	ADCA	89	2	2	99	4	2	A9	4+	2+	B9	5	3			A = A+M+C	+	+	+	+	+	
	ADCB	C9	2	2	D9	4	2	E9	4+	2+	F9	5	3			B = B+M+C	+	+	+	+	+	
ADD	ADDA	8B	2	2	9B	4	2	AB	4+	2+	BB	5	3			A = A+M	+	+	+	+	+	
	ADDB	CB	2	2	DB	4	2	EB	4+	2+	FB	5	3			B = B+M	+	+	+	+	+	
	ADDD	C3	4	3	D3	6	2	E3	6+	2+	F3	7	3			D = D+M:M+1		+	+	+	+	
AND	ANDA	84	2	2	94	4	2	A4	4+	2+	B4	5	3			A = A && M		+	+	0		
	ANDB	C4	2	2	D4	4	2	E4	4+	2+	F4	5	3			B = B && M		+	+	0		
	ANDCC	1C	3	2												C = CC && IMM	?	?	?	?	?	
ASL	ASLA												48	2	1	Arithmetic shift left	8	+	+	+	+	
	ASLB												58	2	1		8	+	+	+	+	
	ASL				08	6	2	68	6+	2+	78	7	3				8	+	+	+	+	
ASR	ASRA												47	2	1	Arithmetic shift right	8	+	+		+	
	ASRB												57	2	1		8	+	+		+	
	ASR				07	6	2	67	6+	2+	77	7	3				8	+	+		+	
BIT	BITA	85	2	2	95	4	2	A5	4+	2+	B5	5	3			Bit Test A (M&&A)		+	+	0		
	BITB	C5	2	2	D5	4	2	E5	4+	2+	F5	5	3			Bit Test B (M&&B)		+	+	0		
CLR	CLRA												4F	2	1	A = 0	0	1	0	0		
	CLRB												5F	2	1	B = 0	0	1	0	0		
	CLR				0F	6	2	6F	6+	2+	7F	7	3			M = 0	0	1	0	0		
CMP	CMPA	81	2	2	91	4	2	A1	4+	2+	B1	5	3			Compare M from A	8	+	+	+	+	
	CMPB	C1	2	2	D1	4	2	E1	4+	2+	F1	5	3			Compare M from B	8	+	+	+	+	
	CMPD	10 83	5	4	10 93	7	3	10 A3	7+	3+	10 B3	8	4			Compare M:M+1 from D		+	+	+	+	
	CMPS	11 8C	5	4	11 9C	7	3	11 AC	7+	3+	11 BC	8	4			Compare M:M+1 from S		+	+	+	+	
	CMPU	11 83	5	4	11 93	7	3	11 A3	7+	3+	11 B3	8	4			Compare M:M+1 from U		+	+	+	+	
	CMPX	8C	4	3	9C	6	2	AC	6+	2+	BC	7	3			Compare M:M+1 from X		+	+	+	+	
	CMPY	10 8C	5	4	10 9C	7	3	10 AC	7+	3+	10 BC	8	4			Compare M:M+1 from Y		+	+	+	+	
COM	COMA												43	2	1	A = complement(A)		+	+	0	1	
	COMB												53	2	1	B = complement(B)		+	+	0	1	
	COM				03	6	2	63	6+	2+	73	7	3			M = complement(M)		+	+	0	1	
CWAI		3C	=> 20	2												CC = CC ^ IMM; Wait for Interrupt					7	
DAA													19	2	1	Decimal Adjust A		+	+	0	+	
DEC	DECA												4A	2	1	A = A - 1		+	+	+		
	DECB												5A	2	1	B = B - 1		+	+	+		
	DEC				0A	6	2	6A	6+	2+	7A	7	3			M = M - 1		+	+	+		

EOR	EORA	88	2	2	98	4	2	A8	4+	2+	B8	5	3		A = A XOR M		+	+	0	
	EORB	C8	2	2	D8	4	2	E8	4+	2+	F8	5	3		B = M XOR B		+	+	0	
EXG	R1,R2	1E	8	2											exchange R1,R2					
INC	INCA											4C	2	1	A = A + 1		+	+	+	
	INCB											5C	2	1	B = B + 1		+	+	+	
	INC				0C	6	2	6C	6+	2+	7C	7	3		M = M + 1		+	+	+	
JMP					0E	3	2	6E	3+	2+	7E	4	3		pc = EA					
JSR					9D	7	2	AD	7+	2+	BD	8	3		jump to subroutine					

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		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op		~	#	H	N	Z	V	C
LD	LDA	86	2	2	96	4	2	A6	4+	2+	B6	5	3				A = M		+	+	0	
	LDB	C6	2	2	D6	4	2	E6	4+	2+	F6	5	3				B = M		+	+	0	
	LDD	CC	3	3	DC	5	2	EC	5+	2+	FC	6	3				D = M:M+1		+	+	0	
	LDS	10 CE	4	4	10 DE	6	3	10 EE	6+	3+	10 FE	7	4				S = M:M+1		+	+	0	
	LDU	CE	3	3	DE	5	2	EE	5+	2+	FE	6	3				U = M:M+1		+	+	0	
	LDX	8E	3	3	9E	5	2	AE	5+	2+	BE	6	3				X = M:M+1		+	+	0	
	LDY	10 8E	4	4	10 9E	6	3	10 AE	6+	3+	10 BE	7	4				Y = M:M+1		+	+	0	
LEA	LEAS							32	4+	2+							S = EA					
	LEAU							33	4+	2+							U = EA					
	LEAX							30	4+	2+							X = EA			+		
	LEAY							31	4+	2+							Y = EA			+		
LSL	LSLA													48	2	1	Logical shift left		+	+	+	+
	LSLB													58	2	1			+	+	+	+
	LSL				08	6	2	68	6+	2+	78	7	3						+	+	+	+
LSR	LSRA													44	2	1	Logical shift right		0	+		+
	LSRB													54	2	1			0	+		+
	LSR				04	6	2	64	6+	2+	74	7	3						0	+		+
MUL														3D	11	1	D = A*B (Unsigned)			+		9
NEG	NEGA													40	2	1	A = !A + 1	8	+	+	+	+
	NEGB													50	2	1	B = !B + 1	8	+	+	+	+
	NEG				00	6	2	60	6+	2+	70	7	3				M = !M + 1	8	+	+	+	+
NOP														12	2	1	No Operation					
OR	ORA	8A	2	2	9A	4	2	AA	4+	2+	BA	5	3				A = A M		+	+	0	
	ORB	CA	2	2	DA	4	2	EA	4+	2+	FA	5	3				B = B M		+	+	0	
	ORCC	1A	3	2													C = CC IMM	?	?	?	?	?
PSH	PSHS	34	5+	2													Push Registers on S Stack					
	PSHU	36	5+	2													Push Registers on U Stack					

PUL	PULS	35	5+	2										Pull Registers from S Stack							
	PULU	37	5+	2										Pull Registers from U Stack							
ROL	ROLA										49	2	1	Rotate left thru carry		+	+	+	+		
	ROLB										59	2	1			+	+	+	+		
	ROL				09	6	2	69	6+	2+	79	7	3				+	+	+	+	
ROR	RORA										46	2	1	Rotate Right thru carry		0	+		+		
	RORB										56	2	1			0	+		+		
	ROR				06	6	2	66	6+	2+	76	7	3				0	+		+	
RTI											3B	6/15	1	Return from Interrupt	?	?	?	?	?		
RTS											39	5	1	Return from subroutine							
SBC	SBCA	82	2	2	92	4	2	A2	4+	2+	B2	5	3	A = A - M - C			8	+	+	+	+
	SBCB	C2	2	2	D2	4	2	E2	4+	2+	F2	5	3	B = B - M - C			8	+	+	+	+
SEX											1D	2	1	Sign extend B into A		+	+	0			
ST	STA				97	4	2	A7	4+	2+	B7	5	3	M = A				+	+	0	
	STB				D7	4	2	E7	4+	2+	F7	5	3	M = B				+	+	0	
	STD				DD	5	2	ED	5+	2+	FD	6	3	M:M+1 = D				+	+	0	
	STS				10 DF	6	3	10 EF	6+	3+	10 FF	7	4	M:M+1 = S				+	+	0	
	STU				DF	5	2	EF	5+	2+	FF	6	3	M:M+1 = U				+	+	0	
	STX				9F	5	2	AF	5+	2+	BF	6	3	M:M+1 = X				+	+	0	
	STY				10 9F	6	3	10 AF	6+	3+	10 BF	7	4	M:M+1 = Y				+	+	0	
SUB	SUBA	80	2	2	90	4	2	A0	4+	2+	B0	5	3	A = A - M			8	+	+	+	+
	SUBB	C0	2	2	D0	4	2	E0	4+	2+	F0	5	3	B = B - M			8	+	+	+	+
	SUBD	83	4	3	93	6	2	A3	6+	2+	B3	7	3	D = D - M:M+1				+	+	+	+
SWI	SWI										3F	19	1	Software interrupt 1							
	SWI2										10 3F	20	2	Software interrupt 2							
	SWI3										11 3F	20	2	Software interrupt 3							
SYNC											13	>= 4	1	Synchronize to Interrupt							
TFR	R1,R2	1F	6	2										R2 = R1							
TST	TSTA										4D	2	1	Test A		+	+	0			
	TSTB										5D	2	1	Test B		+	+	0			
	TST				0D	6	2	6D	6+	2+	7D	7	3	Test M				+	+	0	

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Legend:		
! Complement of M	+ Test and set if true, cleared otherwise	OP Operation Code(Hexadecimal)
= Transfer from	- Not Affected	~ Number of MPU Cycles
H Half carry (from bit 3)	CC Condition Code Register	# Number of Program Bytes
N Negative (sign bit)	: Concatenation	+ Arithmetic Plus
Z Zero (Reset)	Logical or	Arithmetic Minus
V Overflow, 2's complement	&& Logical and	* Multiply
C Carry from ALU	EOR Logical Exclusive or	EA Effective Address:w

Notes:

1. This column gives a base cycle and byte count. To obtain total count, add the values obtained from the INDEXED ADDRESSING MODE table, in Appendix F.
2. R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
The 8 bit registers are: A, B, CC, DP
The 16 bit registers are: X, Y, U, S, D, PC
3. EA is the effective address.
4. The PSH and PUL instructions require 5 cycles plus 1 cycle for each byte pushed or pulled.
5. 5(6) means: 5 cycles if branch not taken, 6 cycles if taken (Branch instructions.
6. SWI sets I and F bits. SW12 and SW13 do not affect I and F.
7. Conditions Codes set as a direct result of the instruction.
8. Value of half carry flag is undefined.
9. Special Case Carry set if b7 is SET.

Instruction	Forms	Mode		Description	5 3 2 1 0				
		OP	Relative		H	N	Z	V	C
BCC	BCC	24	3 /	2 Branch C=0					
	LBCC	10	5(6)	4 Long Branch					
		24		C=0					
BCS	BCS	25	3	2 Branch C= 1					
	LBCCS	10	5(6)	4 Long Branch					
		25		C=1					
BEQ	BEQ	27	3	2 Branch Z=0					
	LBREQ	10	5(6)	4 Long Branch					
		27		Z=0					
BGE	BGE	2C	3	2 Branch2Zero					
	LBGE	10	5(6)	4 Long Branch2Zero					
		2C							
BGT	BGT	2E	3	2 Branch > Zero					
	LBGT	10	5(6)	4 Long Branch>Zero					

			2E	
BHI	BHI	22 3	2 Branch rhigher	
	LBHI	10 5(6)	4 Long Branch Higher	
		22		
BHS	BHS	24 3	2 Branch Higher	
			or Same	
	LBHS	10 5(6)	4 Long Branch Higher	
		24	or Same	
BLE	BLE	2F 3	2 BranchsZero	
	LBLE	10 5(6)	4 Long BranchsZero	
		2F		
BLO	BLO	25 3	2 Branch lower	
	LBLO	10 5(6)	4 Long Branch Lower	
		25		

Address in Mode		T			
Rela		5	3	2	1 ,0
Instruction	Forms	OP	#	Description H N Z V C	
BLS	BLS	23 3	2	Branch Lower	
				or Same	
	LBLS	10 5(6)	4	Long Branch Lower	
		23		or Same	
BLT	BLT	2D 3	2	Branch<Zero	
	LBLT	10 5(6)	4	Long Branch<Zero	
		2D			
BMI	BMI	2B 3	2	Branch Minus	
	LBMI	10 5(6)	4	Long Branch Minus	
		2B			
BNE	BNE	26 3	2	Branch Zt0	
	LBNE	10 5(6)	4	Long Branch	
		26		Z0	
BPL	BPL	2A "		Branch Plus	
	LBPL	10 5(6)	4	Long Branch Plus	
		2A			
BRA	BRA	20 3	2	Branch Always	
	LBRA	16 5	3	Long Branch Always	
BRN	BRN	21 3	2	Branch Never	
	LB RN	10 5	4	Long Branch Never	
		21			
BSR	BSR	8D 7	2	Branch to Subroutine	
	LBSR	17 9	3	Long Branch to	
				Subroutine	
BVC	BVC	28 3	2	Banch V=0	
	LBVC	10 5(6)	4	Long Branch	
		28		V=0	
BVS	BVS	29 3	2	Branch V= 1	
	LBVS	10 5(6)	4	Long Branch	
		29		V=1	