



ADC²³

**MATT SPEED
& ANDY NORMINGTON**

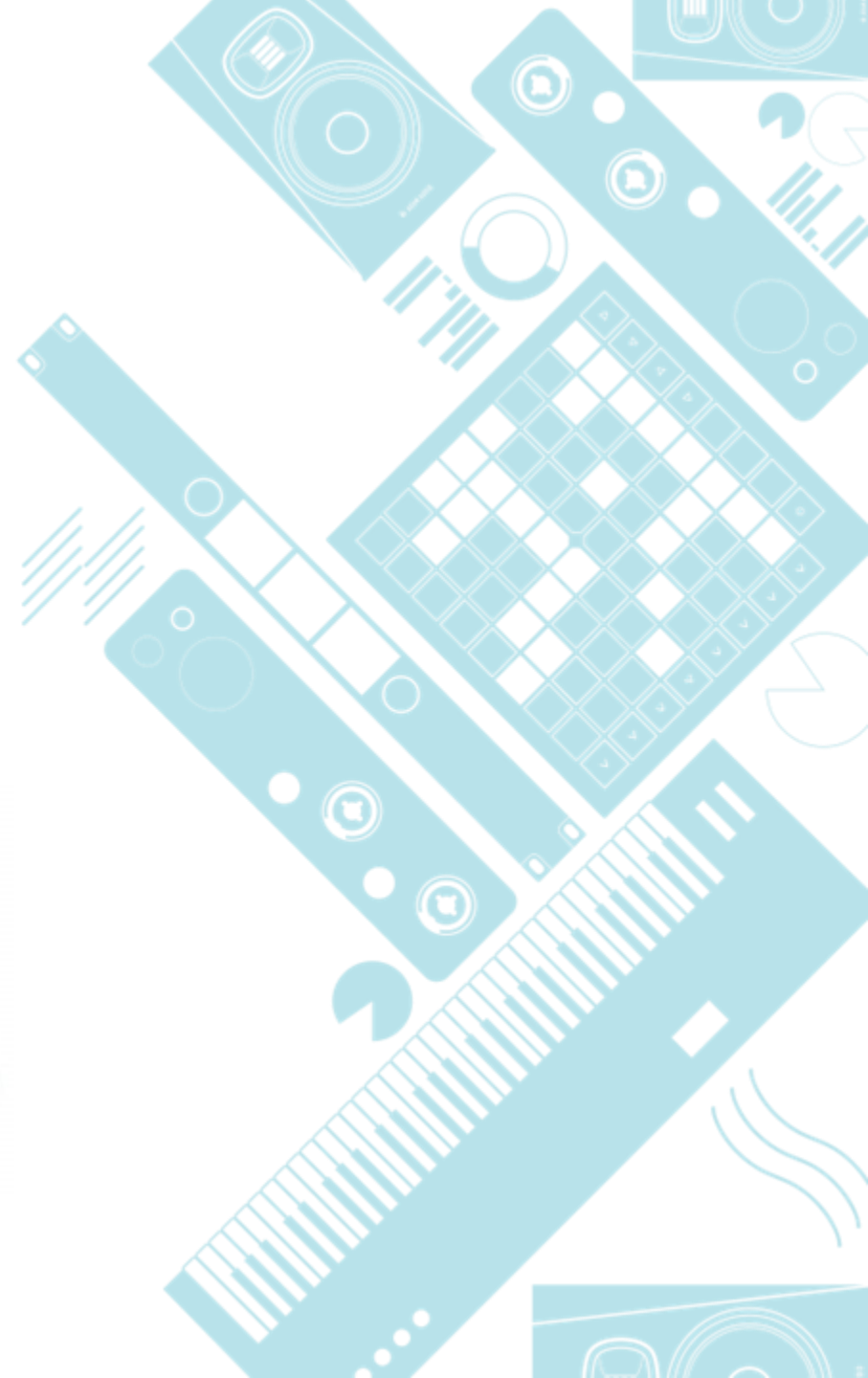
EMBEDDED SOFTWARE DEVELOPMENT

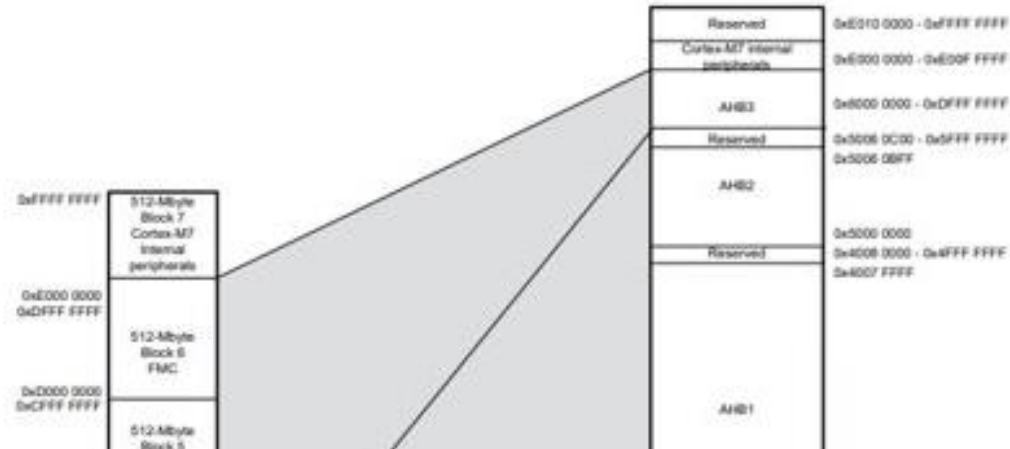
A WILD RIDE!

Embedded Software Development is not Desktop Software Development

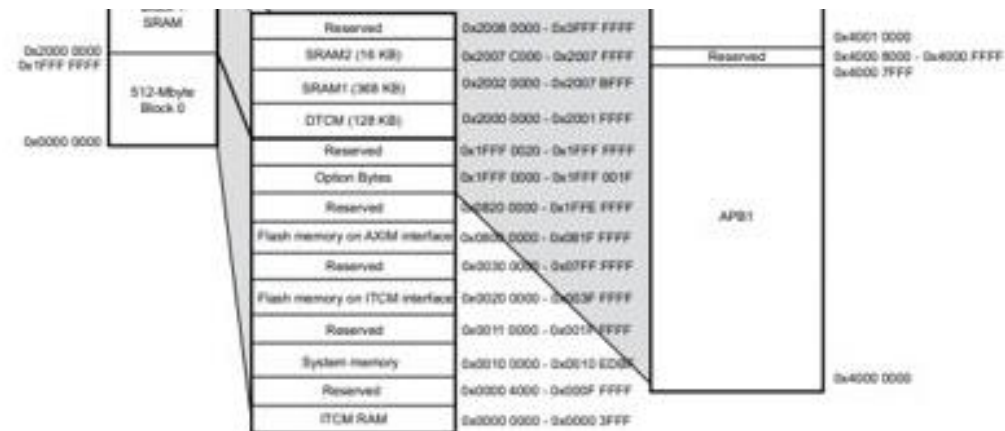


Microcontrollers are not Typical Microprocessors





**Programming is harder
when you don't have
much memory.**



**The range of
available devices is
very broad!**

Word
Size

Memory
Arch

Memory
Size

Clock
Speed

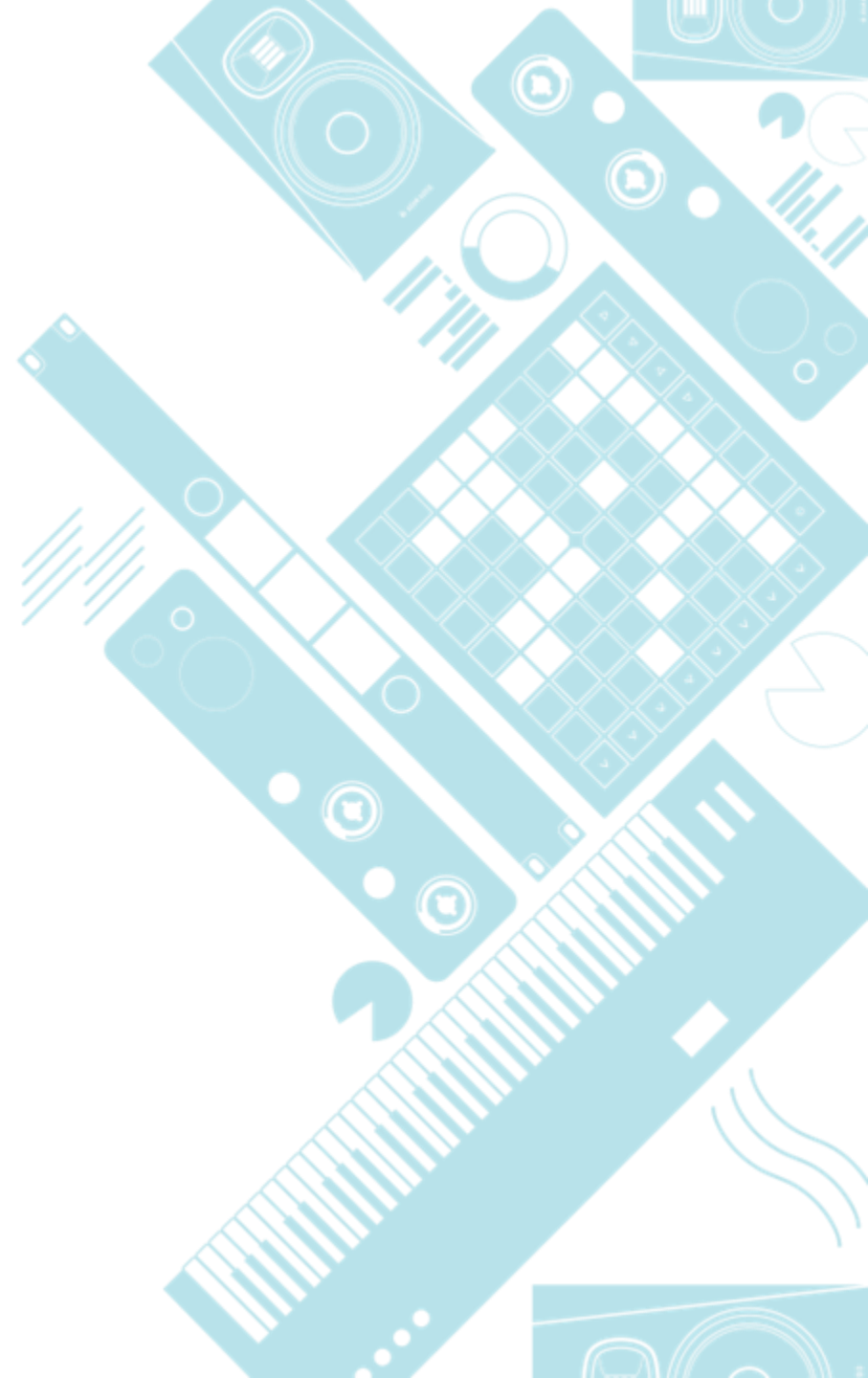
Instruction
Set

Vendor

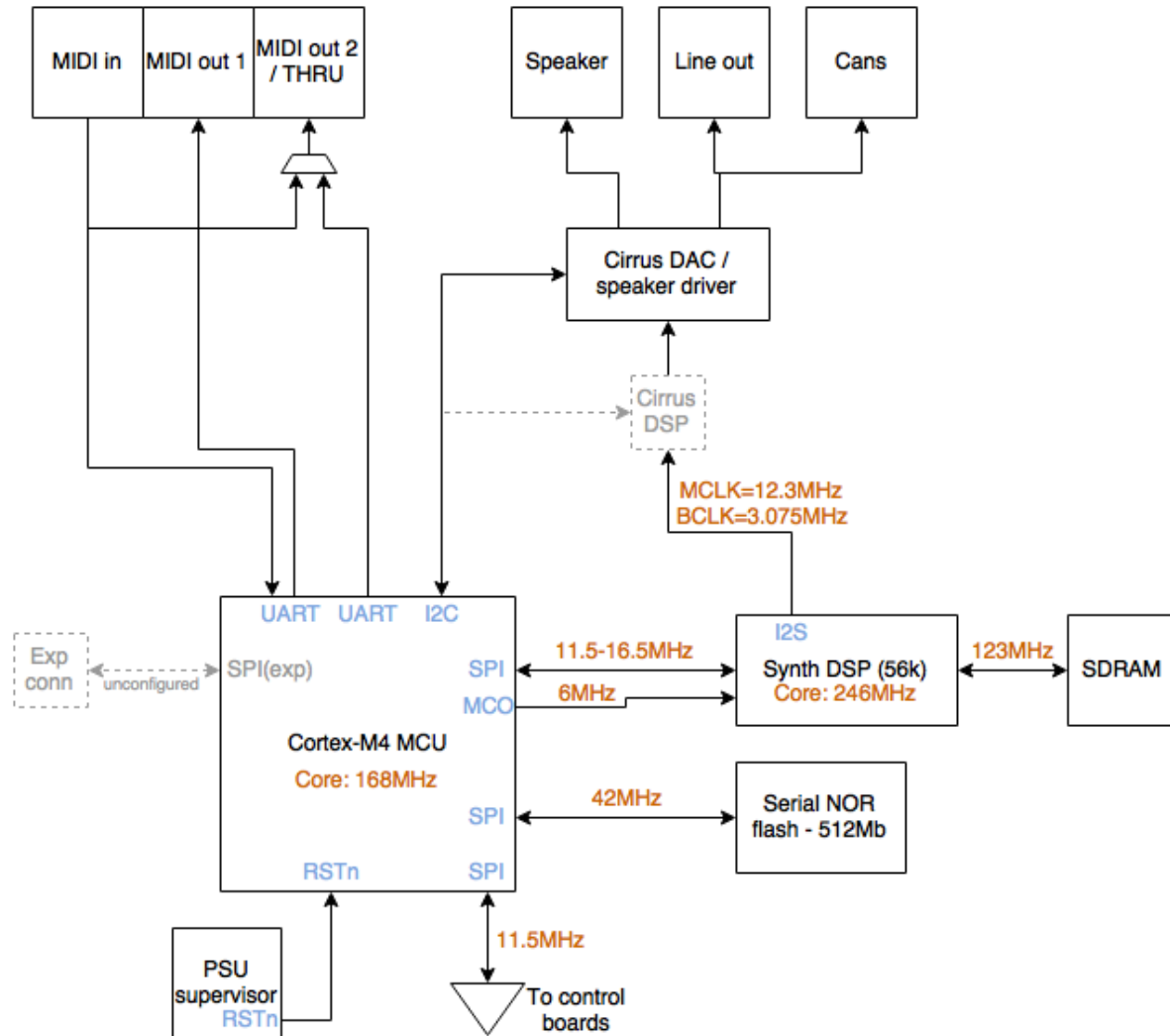
Package

Peripheral
Set

Device
Family



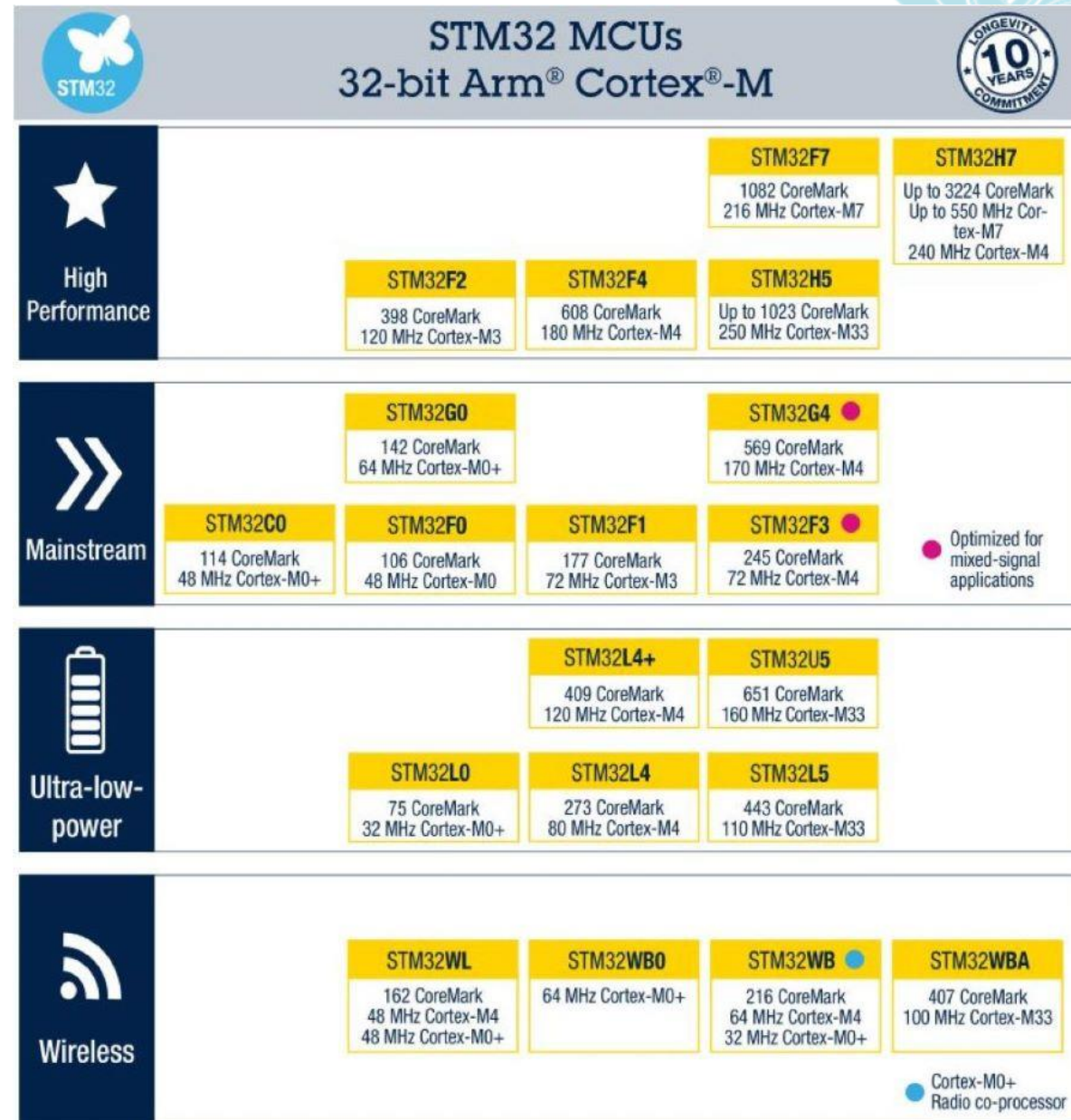
Build up a picture of what the MCU needs to do





Choose a device, thinking about how we should configure it



Pick a family...

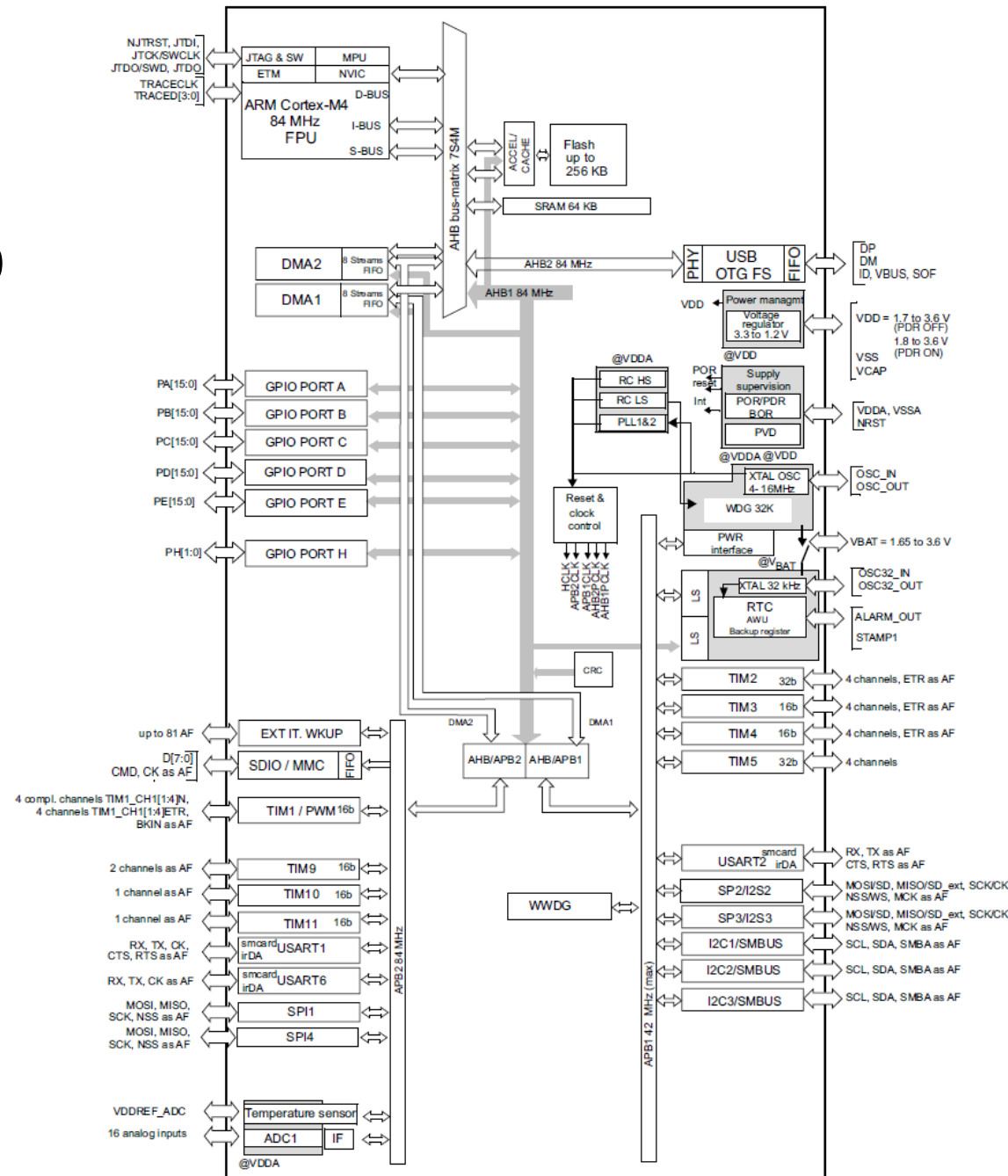


Pick a device...

<div>  <div> STM32F4 MCU Series 32-bit Arm® Cortex®-M4 – Up to 180 MHz </div>  </div>														
Product line	F _{CPU} (MHz)	Flash (KB)	RAM (KB)	Ethernet I/F IEEE 1588	2x CAN	Camera I/F	SDRAM I/F	Dual Quad-SPI	SAI	SPDIF RX	Chrom-ART Graphic Accelerator™	TFT LCD Controller	MIPIDSI	
Advanced lines														
STM32F469 ²	180	512 K to 2056 K	384	•	•	•	•	•	•		•	•	•	
STM32F429 ²	180	512 K to 2056 K	256	•	•	•	•		•		•	•		
STM32F427 ²	180	1024 K to 2056 K	256	•	•	•	•		•		•			
Foundation lines														
STM32F446	180	256 K to 512 K	128		•	•	•	•	•	•				
STM32F407 ²	168	512 K to 1024 K	192	•	•	•								
STM32F405 ²	168	512 K to 1024 K	192		•									
Product line	F _{CPU} (MHz)	Flash (KB)	RAM (KB)	RUN current (µA/MHz)	STOP current (µA)	Small package (mm)	FSMC (NOR/PSRAM/LCD) support	QSPI	DFSDM	DAC	TRNG	DMA Batch Acquisition mode	USB 2.0 OTG FS	
Access lines														
STM32F401	84	128 K to 512 K	up to 96	Down to 128	Down to 10	Down to 3x3							•	
STM32F410	100	64 K to 128 K	32	Down to 89	Down to 6	Down to 2.553x 2.579				•	•	BAM	-	
STM32F411	100	256 K to 512 K	128	Down to 100	Down to 12	Down to 3.034x 3.22						BAM	•	
STM32F412	100	512 K to 1024 K	256	Down to 112	Down to 18	Down to 3.653x 3.651	•	•	•		•	BAM	•+LPM ¹	
STM32F413 ²	100	1024 K to 1536 K	320	Down to 115	Down to 18	Down to 3.951x 4.039	•	•	•	•	•	BAM	•+LPM ¹	

- ART Accelerator™
- SDIO
- USART, SPI, PC
- PS + audio PLL
- 16 and 32-bit timers
- 12-bit ADC (0.41 µs)
- True Random Number Generator
- Batch Acquisition Mode
- Low voltage 1.7 to 3.6 V
- Temperature: -40 °C to 125 °C

...and decide
how to set it up



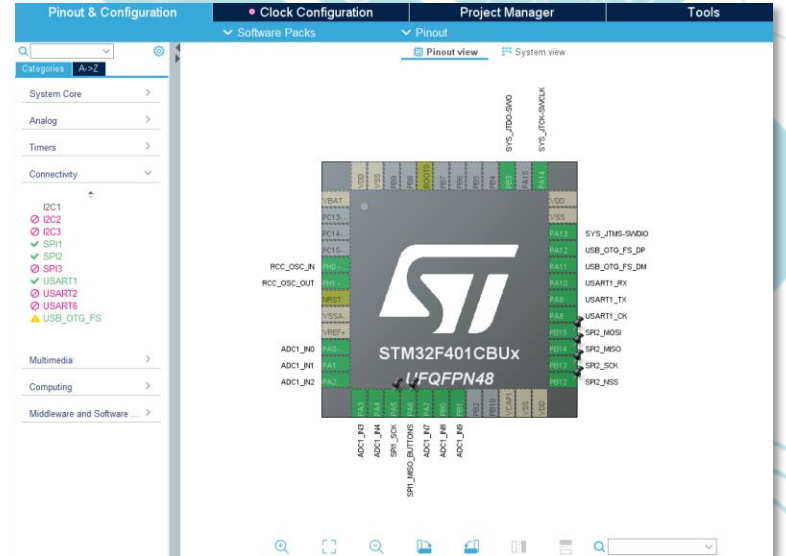
GPIO	W/CE	LOP1	LOP2	UPRG	after reset ⁽¹⁾	Pin	IO	N		
13	E4	17	26	L3	PA3	I/O	FT	-	USART2_RX, TIM2_CH4, TIM5_CH4, TIM9_CH2, EVENTOUT	ADC1_IN3
-	-	18	27	-	VSS	S	-	-	-	-
-	-	19	28	-	VDD	S	-	-	-	-
-	-	-	-	E3	BYPASS_REG	I	FT	-	-	-
14	G6	20	29	M3	PA4	I/O	FT	-	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN4
15	F5	21	30	K4	PA5	I/O	FT	-	SPI1_SCK, TIM2_CH1/TIM2_ETR, EVENTOUT	ADC1_IN5
16	F4	22	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM1_BKIN, TIM3_CH1, EVENTOUT	ADC1_IN6
17	F3	23	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM1_CH1N, TIM3_CH2, EVENTOUT	ADC1_IN7
-	-	24	33	K5	PC4	I/O	FT	-	EVENTOUT	ADC1_IN14
-	-	25	34	L5	PC5	I/O	FT	-	EVENTOUT	ADC1_IN15
18	G5	26	35	M5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, EVENTOUT	ADC1_IN8
19	G4	27	36	M6	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, EVENTOUT	ADC1_IN9
20	G3	28	37	L6	PB2	I/O	FT	-	EVENTOUT	BOOT1
-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, EVENTOUT	-
-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, EVENTOUT	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, EVENTOUT	-



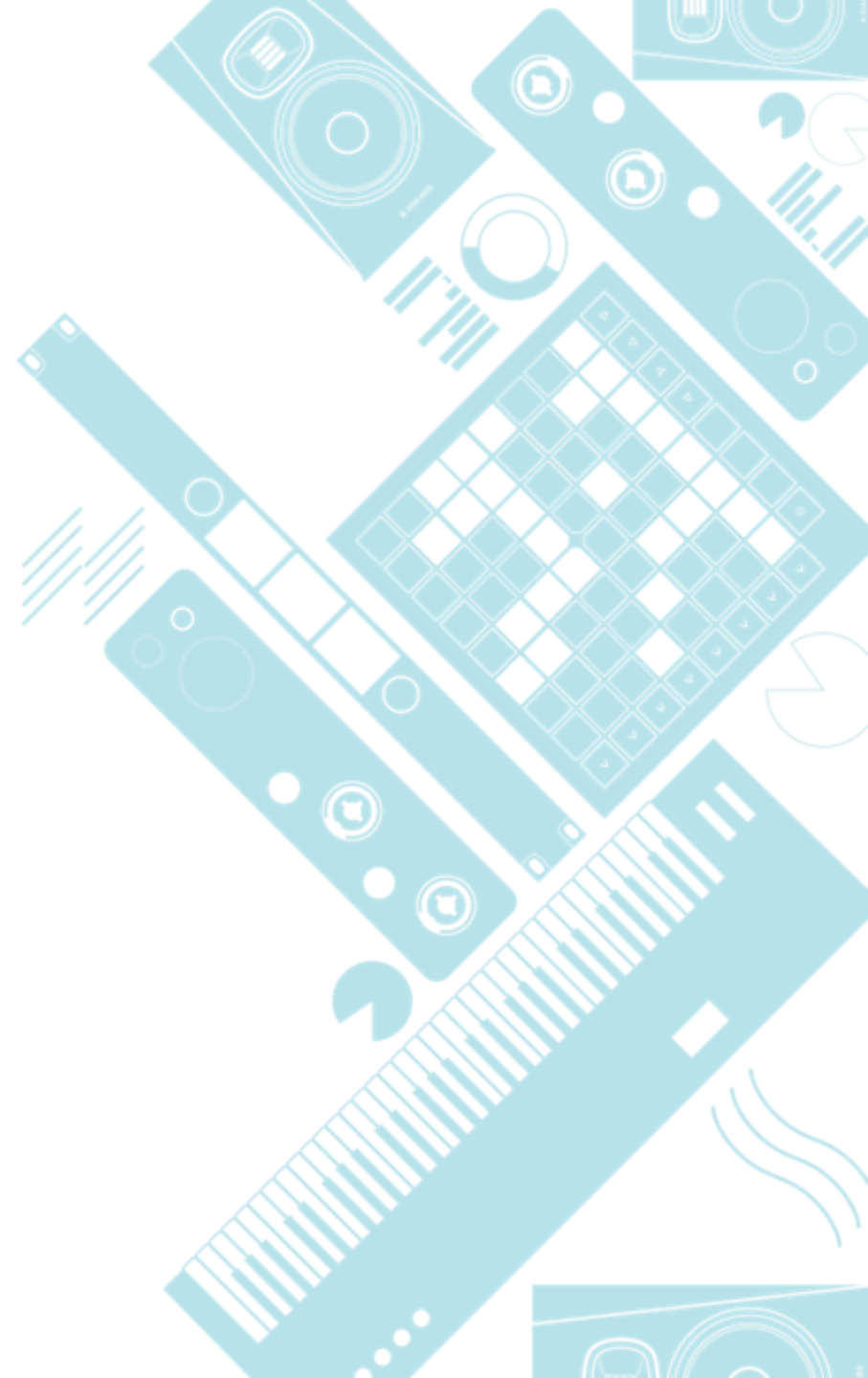
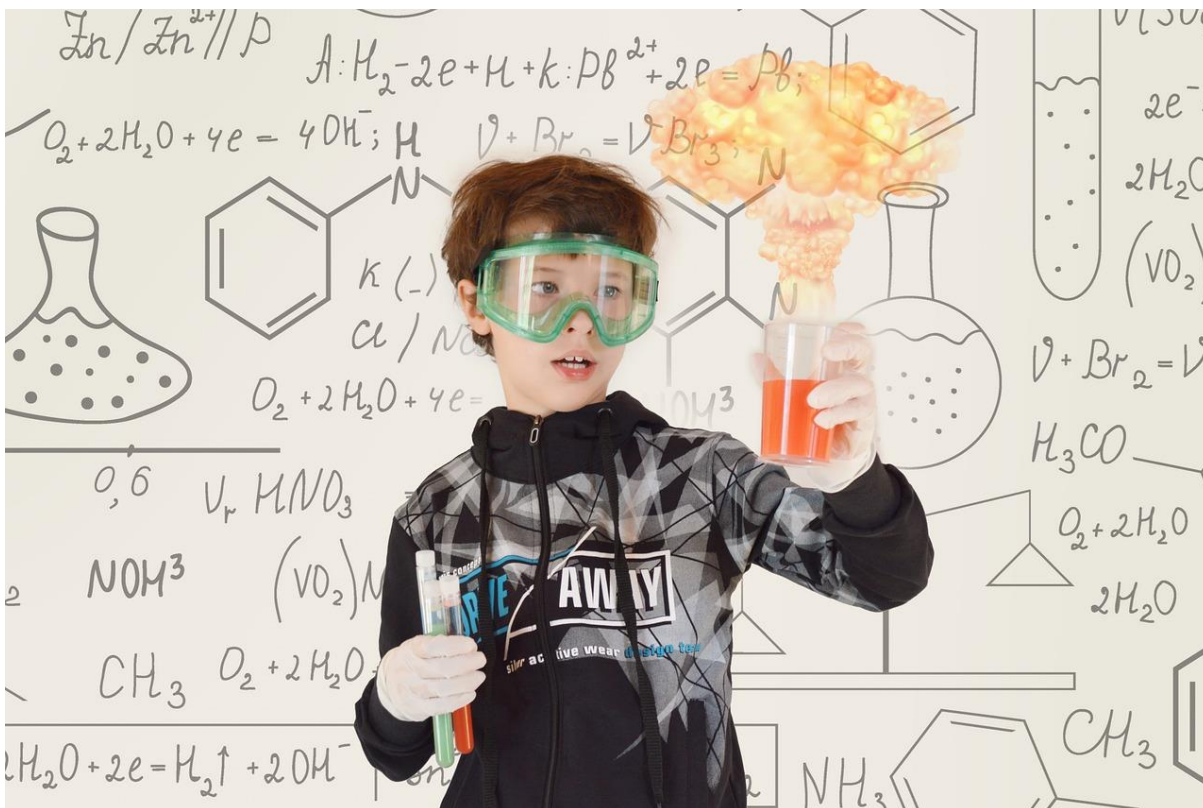
Tile 0 Audio										
I/O	1b	4b	8b	16b	Link	Link	16b	8b	4b	1b
XDD00	A[0]									
XDD01	B[0]									
XDD02	A[0]	A[0]	A[0]							
XDD03	A[1]	A[1]	A[1]							
XDD04	B[0]	A[2]	A[2]		BT0					
XDD05	B[1]	A[3]	A[3]		BT1					
XDD06	B[2]	A[4]	A[4]		BT2					
XDD07	B[3]	A[5]	A[5]							
XDD08	A[2]	A[6]	A[6]							
XDD09	A[3]	A[7]	A[7]							
XDD10	C[0]									
XDD11	D[0]									
XDD12	E[0]									
XDD13	F[0]									
XDD14	C[0]	B[0]	A[8]							
XDD15	C[1]	B[1]	A[9]							
XDD16	D[0]	B[2]	A[10]	L4[4]		L7[4]				
XDD17	D[1]	B[3]	A[11]	L4[3]		L7[3]				
XDD18	D[2]	B[4]	A[12]	L4[2]		L7[2]				
XDD19	D[3]	B[5]	A[13]	L4[1]		L7[1]				
XDD20	C[2]	B[6]	A[14]							
XDD21	C[3]	B[7]	A[15]							
XDD43	L0[1]	B[15]	D[7]							
XDD42	L0[0]	B[14]	D[6]							
XDD41	L0[0]	B[13]	D[5]							
XDD40	L0[1]	B[12]	D[4]							
XDD39		B[11]	D[3]							
XDD38		B[10]	D[2]							
XDD37		B[9]	D[1]							
XDD36		B[8]	D[0]							
XDD35										
XDD34										
XDD33										
XDD32										
XDD31										
XDD30										
XDD29										
XDD28										
XDD27										
XDD26										
XDD25										
XDD24										
XDD23										
XDD22										



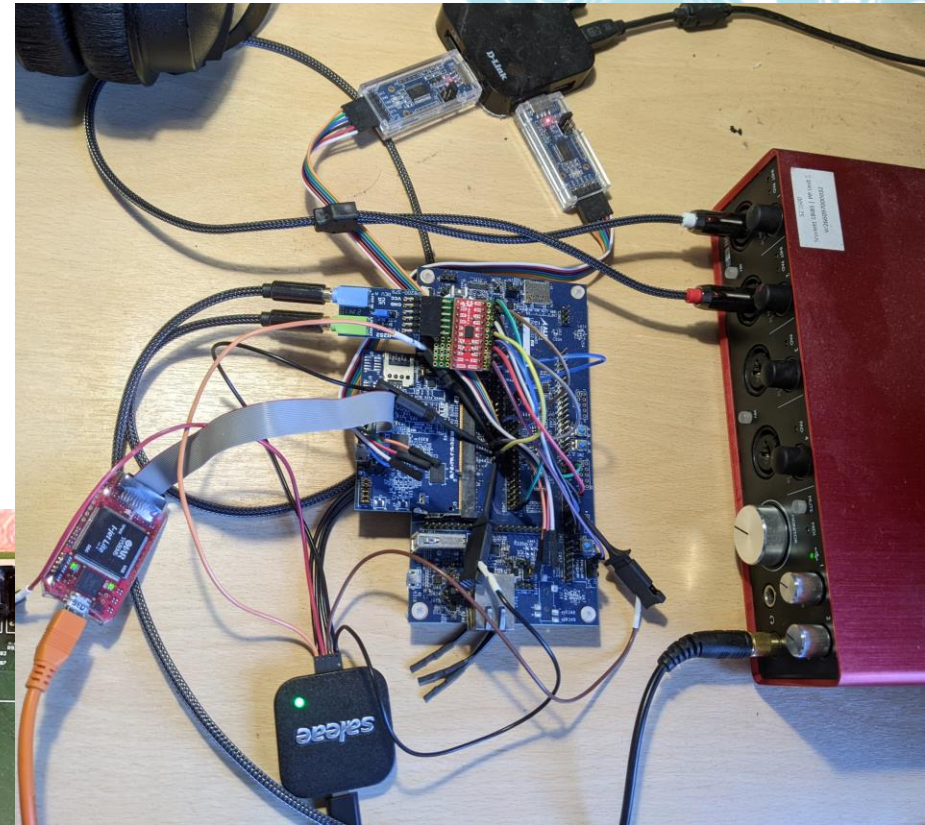
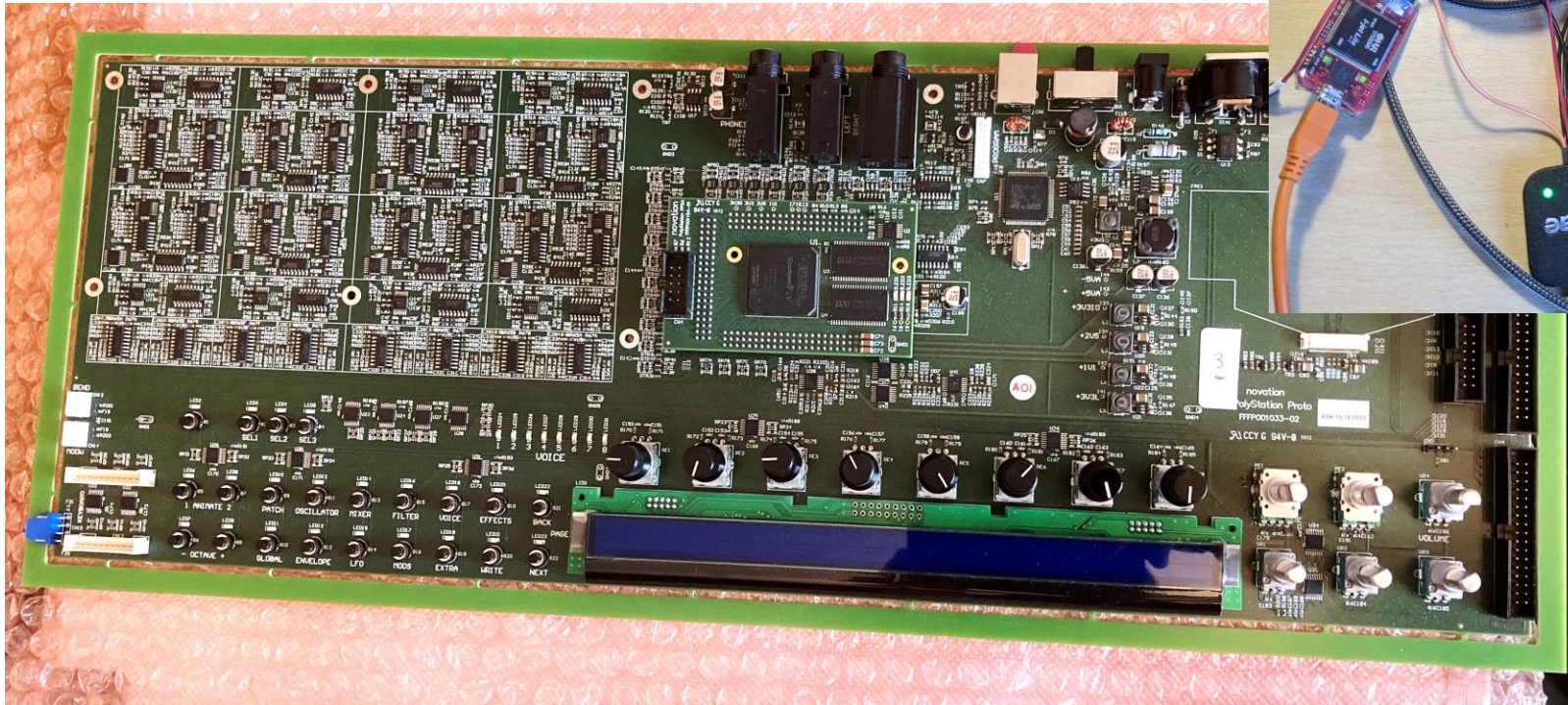
Port	AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF1
	SYS_AF	TIM1/TIM2	TIM3/TIM4/TIM5	TIM6/TIM7/TIM10/TIM11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4	SPI2/I2S2/SPI3/I2S3	SPI3/I2S3/USART4/USART2	USART6	I2C2/I2C3	OTG1_FS		SDIO	
PB0	-	TIM1_CH2N	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	-	-	-	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PB3	JTDO-SWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK/I2S3_CK	-	-	I2C2_SDA	-	-	-	-
PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	I2C3_SDA	-	-	-	-
PB5	-	-	TIM3_CH2	-	-	I2C1_SMB	SPI1_MOSI	SPI3_MISO/I2S3_SD	-	-	-	-	-	-
PB6	-	-	TIM4_CH1	-	-	I2C1_SCL	-	USART1_TX	-	-	-	-	-	-
PB7	-	-	TIM4_CH2	-	-	I2C1_SDA	-	USART1_RX	-	-	-	-	-	-
PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	-	-	-	SDIO_D4	-
PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	SDIO_D5	-
PB10	-	TIM2_CH3	-	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-
PB11	-	TIM2_CH4	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	-
PB12	-	TIM1_BKIN	-	-	-	I2C2_SMB	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-
PB13	-	TIM1_CH1N	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-
PB14	-	TIM1_CH2N	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	-



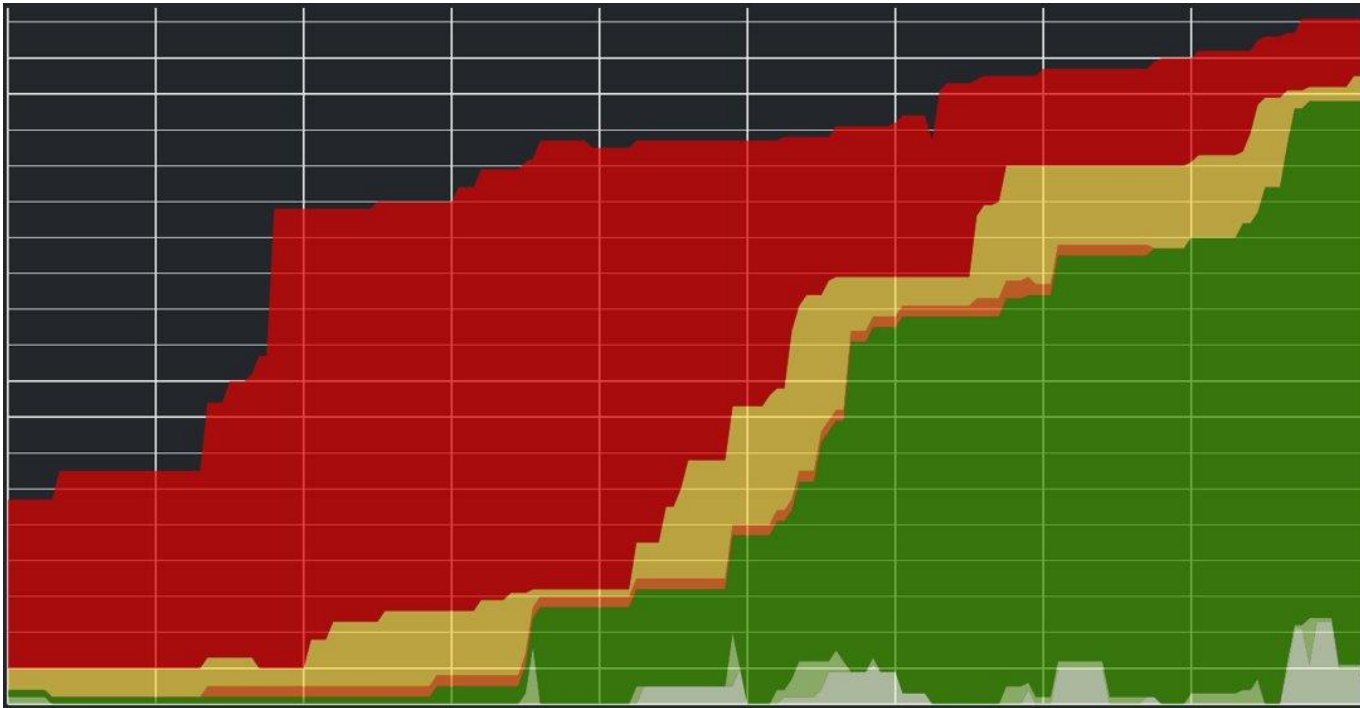
What could possibly go wrong?



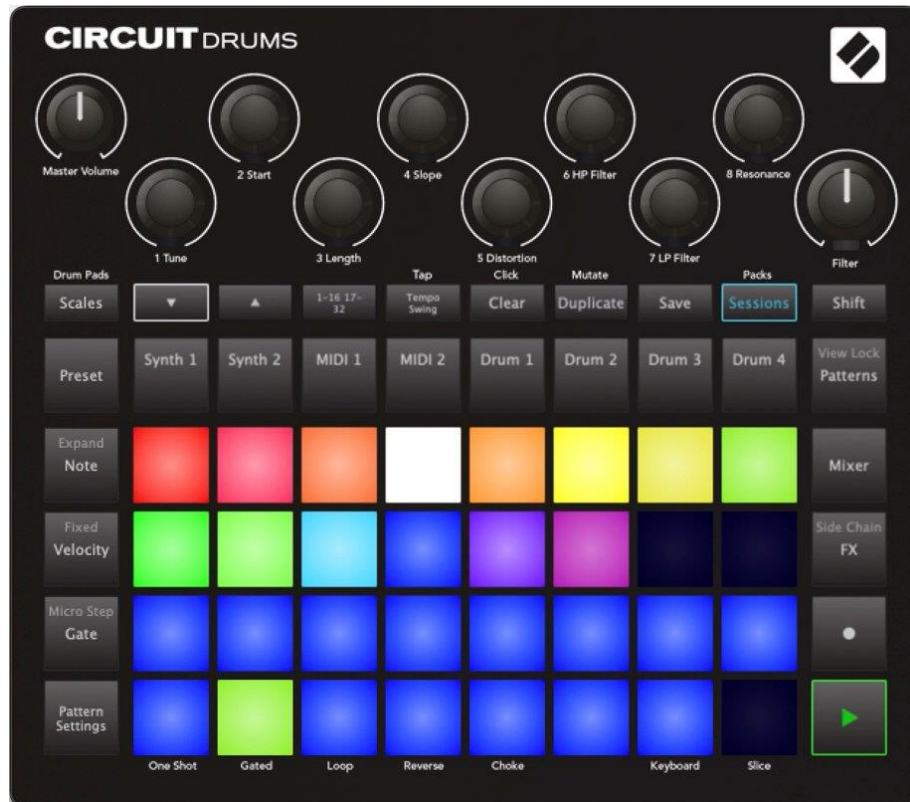
*Just enough hardware
to get started*



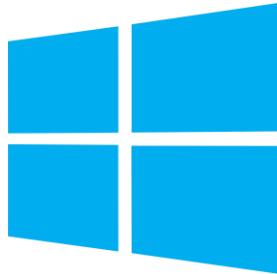
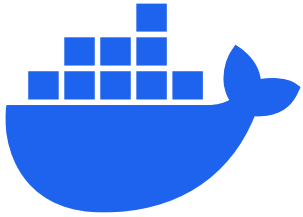
**Firmware engineers
join
multi-disciplinary teams...**



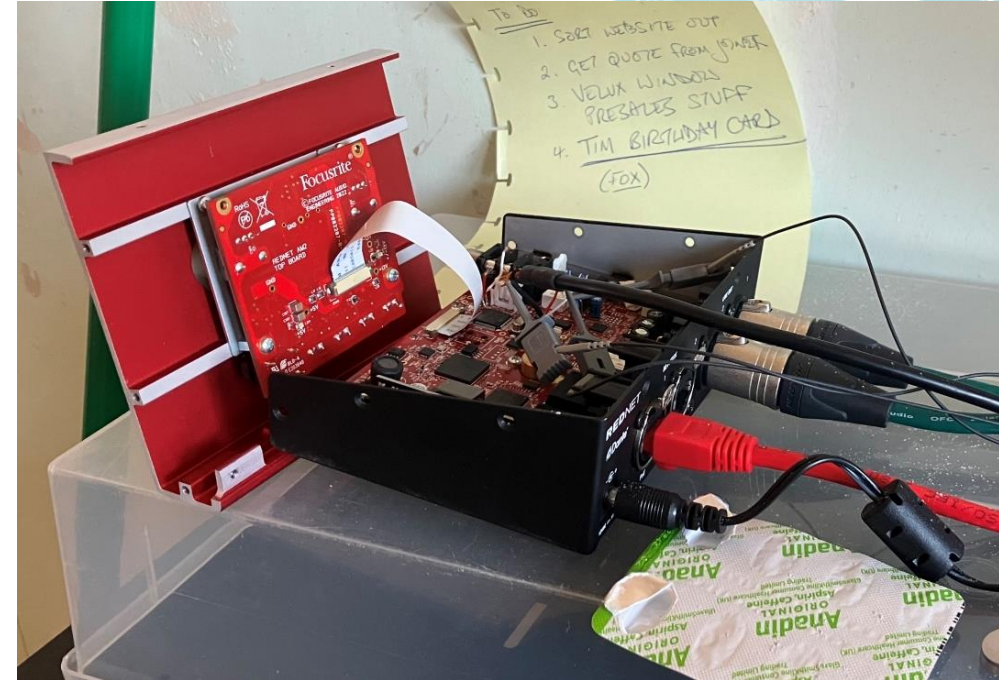
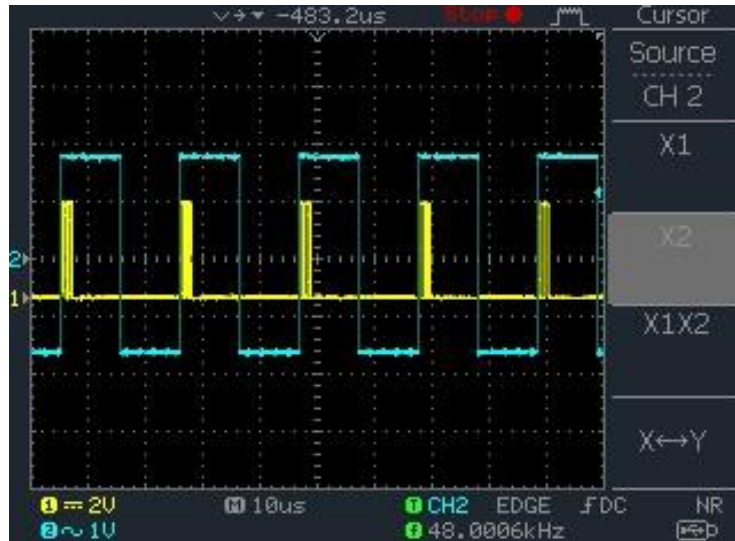
**..but must also couple tightly to
software & hardware development**



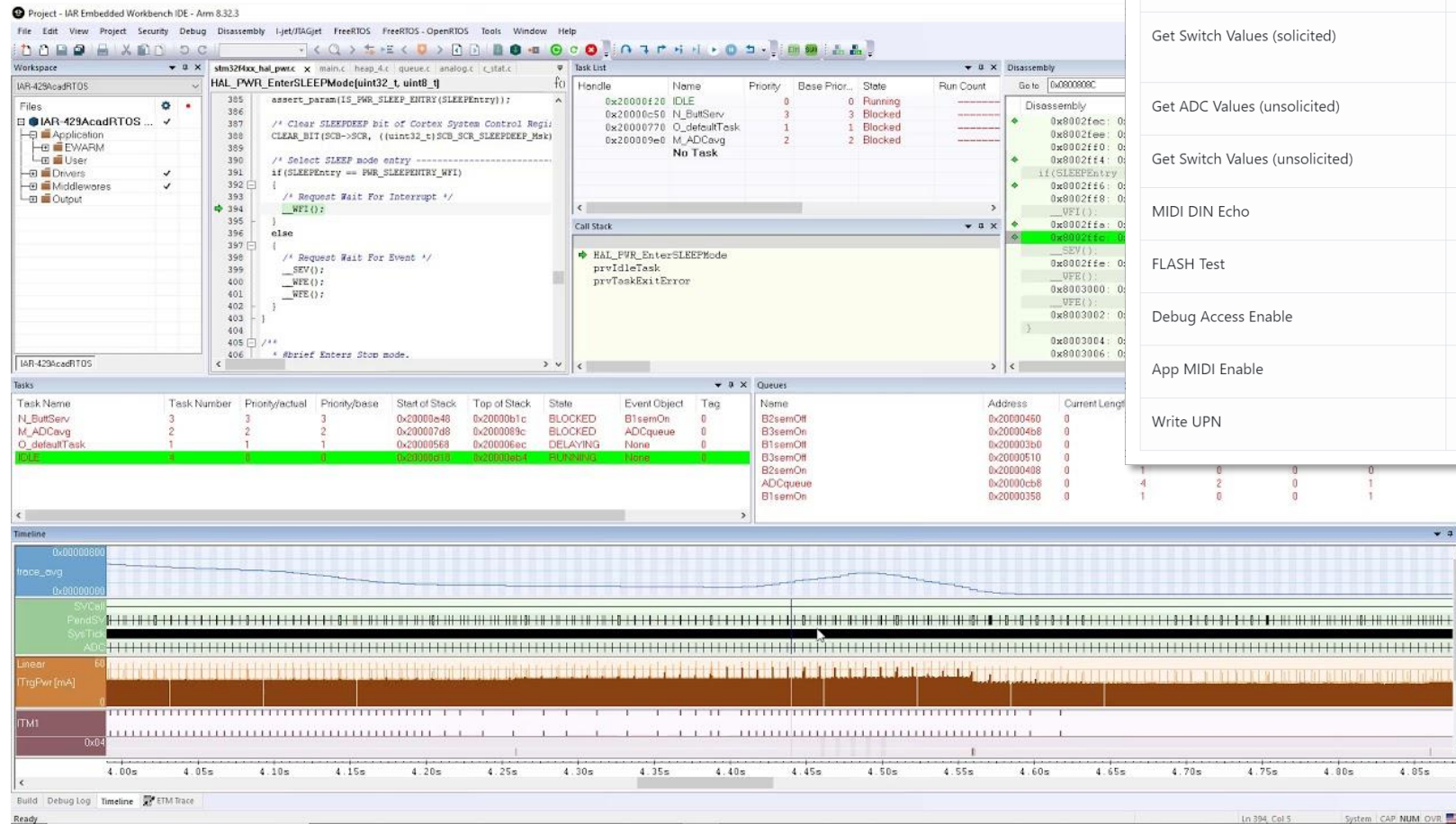
Debugging together – choose tools that keep the barrier to entry low



Finding out what's going on inside

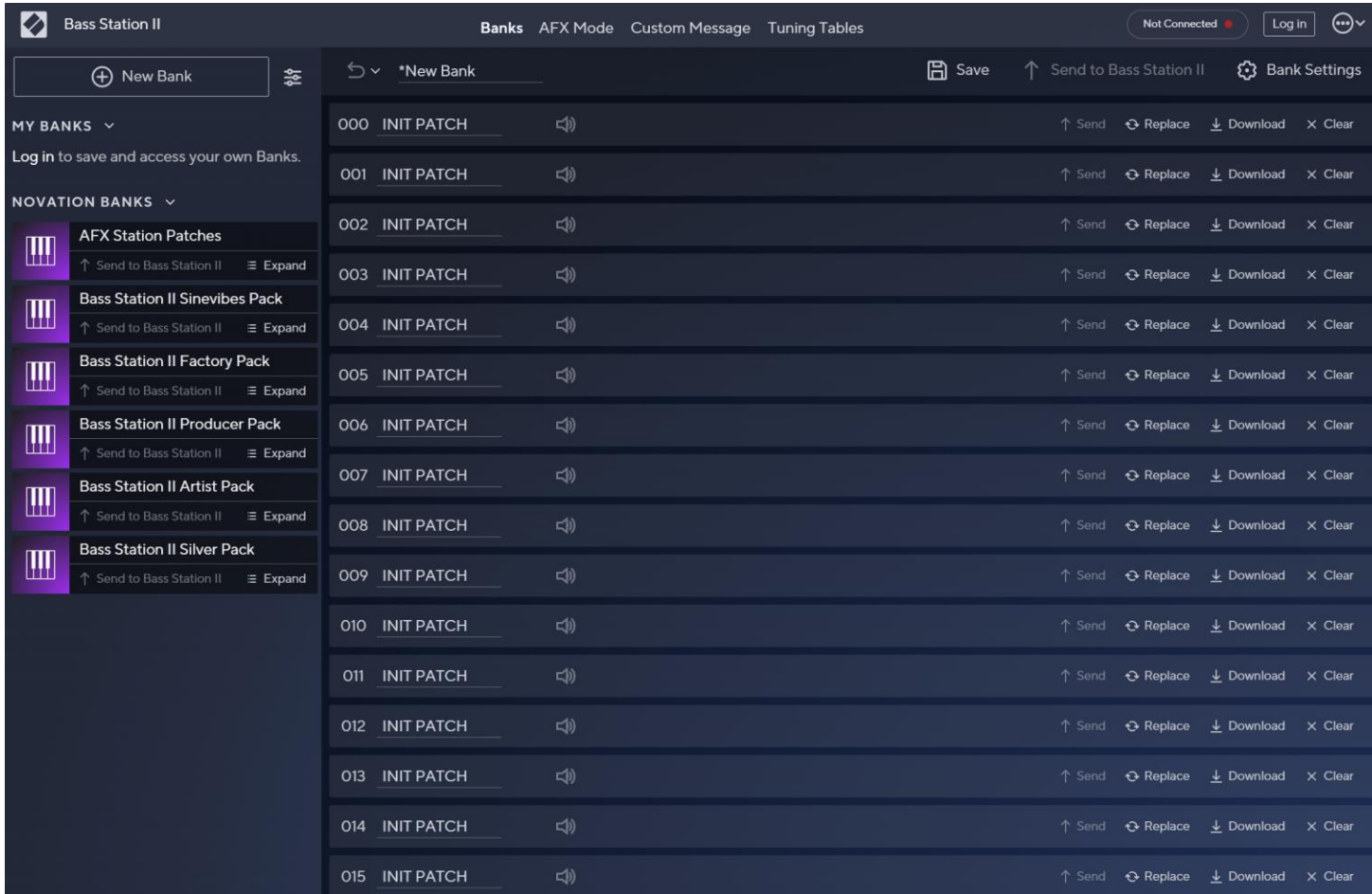


Finding out what's going on inside



Set all RGB LED White		F0 00 20 29 02 0C 70 03 F7	Send
Set all RGB LED Red		F0 00 20 29 02 0C 70 04 F7	Send
Set all RGB LED Green		F0 00 20 29 02 0C 70 05 F7	Send
Set all RGB LED Blue		F0 00 20 29 02 0C 70 06 F7	Send
Get ADC Values (solicited)	0	F0 00 20 29 02 0C 70 10 00 F7	Send
Get Switch Values (solicited)	0	F0 00 20 29 02 0C 70 11 00 00 F7	Send
Get ADC Values (unsolicited)	Enable	F0 00 20 29 02 0C 70 12 01 F7	Send
Get Switch Values (unsolicited)	Enable	F0 00 20 29 02 0C 70 13 01 F7	Send
MIDI DIN Echo	Enable	F0 00 20 29 02 0C 70 30 01 F7	Send
FLASH Test		F0 00 20 29 02 0C 70 40 F7	Send
Debug Access Enable	Enable	F0 00 20 29 02 0C 70 60 01 F7	Send
App MIDI Enable	Enable	F0 00 20 29 02 0C 70 61 01 F7	Send
Write UPN	SN:	F0 00 20 29 02 0C 70 6C F7	Send

Implement Reliable Field Update



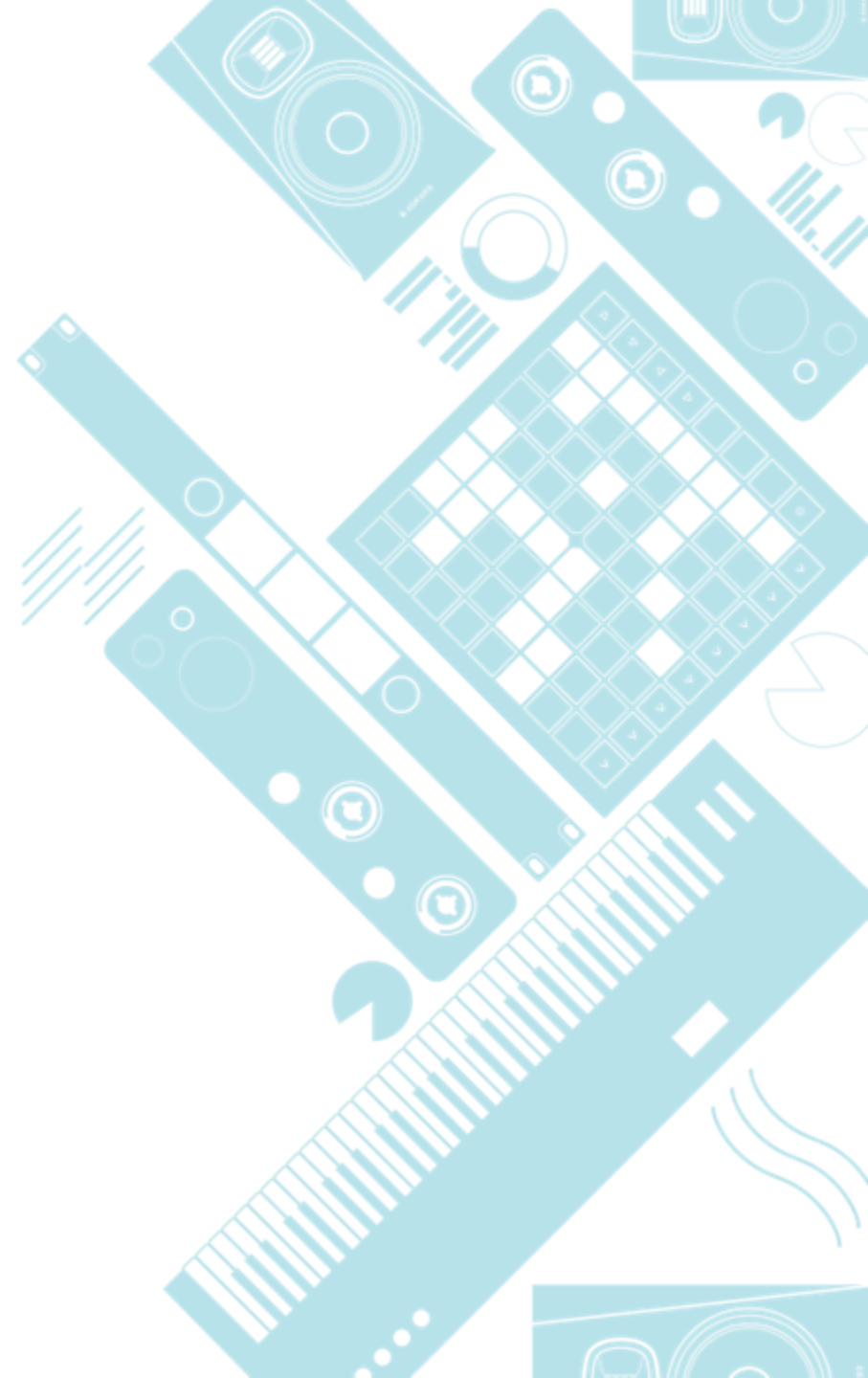
The screenshot displays the Bass Station II web interface. The top navigation bar includes tabs for Banks, AFX Mode, Custom Message, and Tuning Tables. A status bar on the right shows 'Not Connected' and a 'Log in' button. The main content area is divided into a left sidebar and a central table.

Left Sidebar:

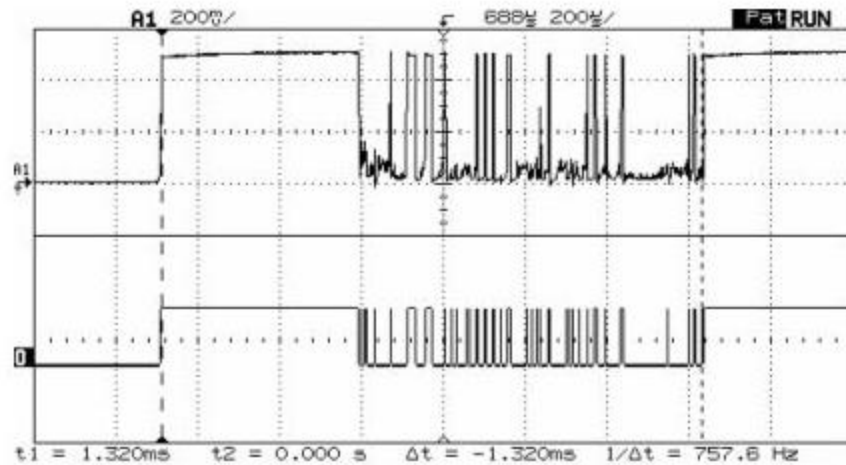
- MY BANKS** (dropdown): Includes a 'Log in to save and access your own Banks.' link.
- NOVATION BANKS** (dropdown): Lists several preset banks, each with a 'Send to Bass Station II' and 'Expand' option:
 - AFX Station Patches
 - Bass Station II Sinevibes Pack
 - Bass Station II Factory Pack
 - Bass Station II Producer Pack
 - Bass Station II Artist Pack
 - Bass Station II Silver Pack

Central Table:

*New Bank		Save	Send to Bass Station II	Bank Settings	
000	INIT PATCH	Send	Replace	Download	Clear
001	INIT PATCH	Send	Replace	Download	Clear
002	INIT PATCH	Send	Replace	Download	Clear
003	INIT PATCH	Send	Replace	Download	Clear
004	INIT PATCH	Send	Replace	Download	Clear
005	INIT PATCH	Send	Replace	Download	Clear
006	INIT PATCH	Send	Replace	Download	Clear
007	INIT PATCH	Send	Replace	Download	Clear
008	INIT PATCH	Send	Replace	Download	Clear
009	INIT PATCH	Send	Replace	Download	Clear
010	INIT PATCH	Send	Replace	Download	Clear
011	INIT PATCH	Send	Replace	Download	Clear
012	INIT PATCH	Send	Replace	Download	Clear
013	INIT PATCH	Send	Replace	Download	Clear
014	INIT PATCH	Send	Replace	Download	Clear
015	INIT PATCH	Send	Replace	Download	Clear



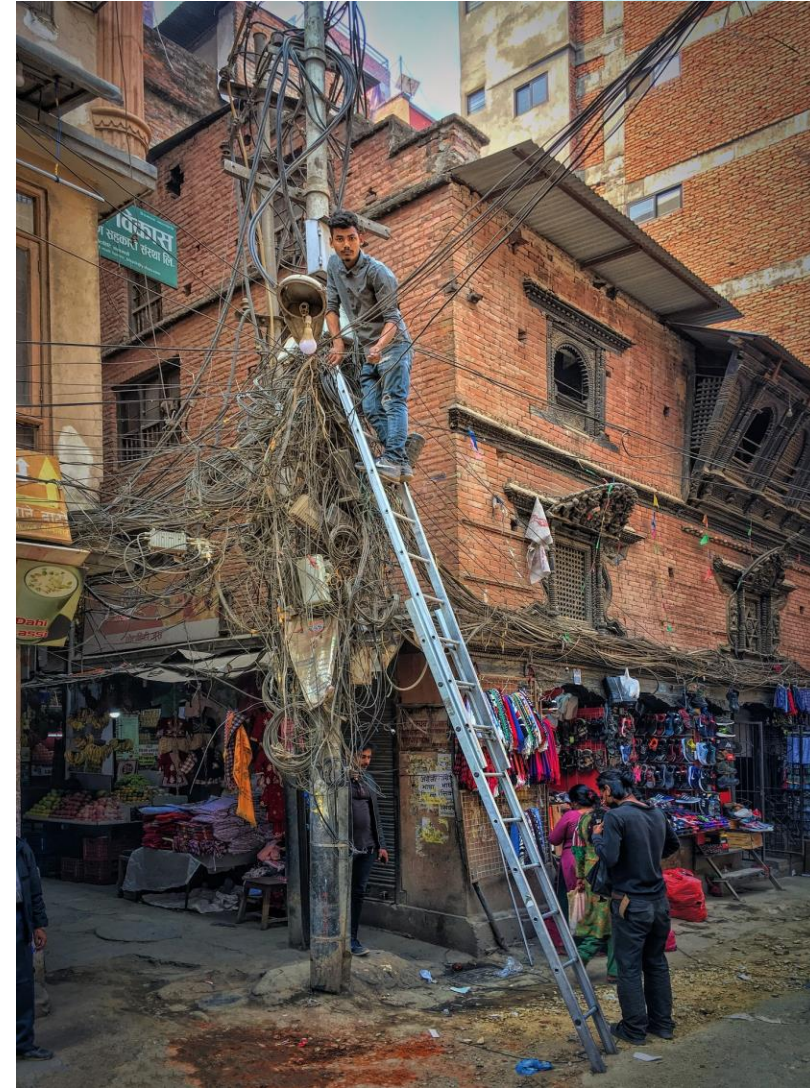
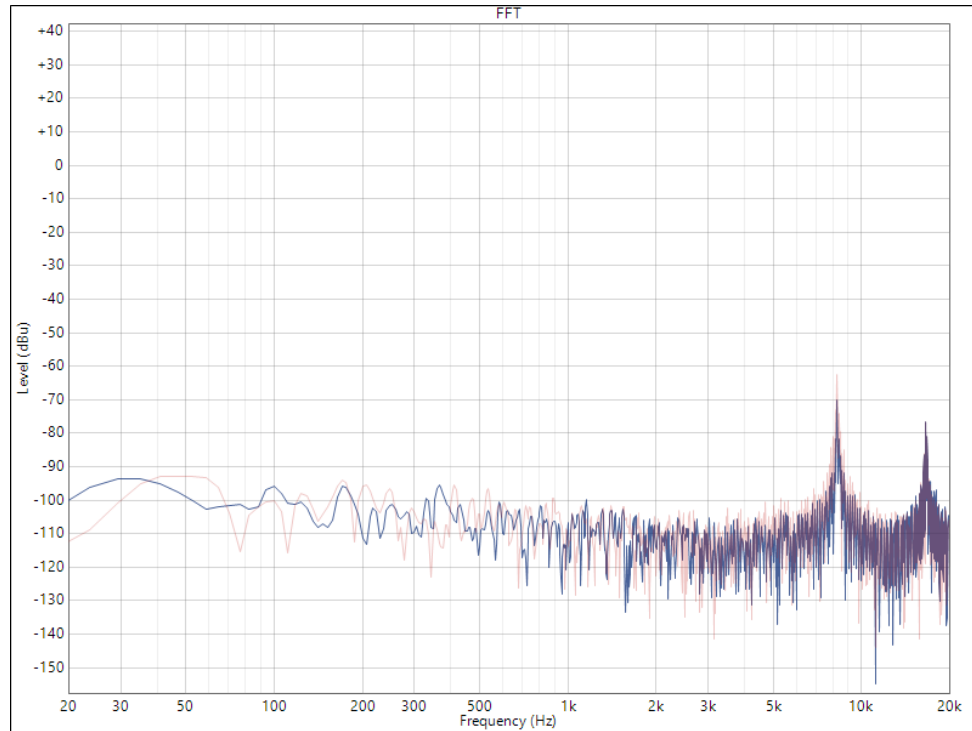
The real world looks a bit funny



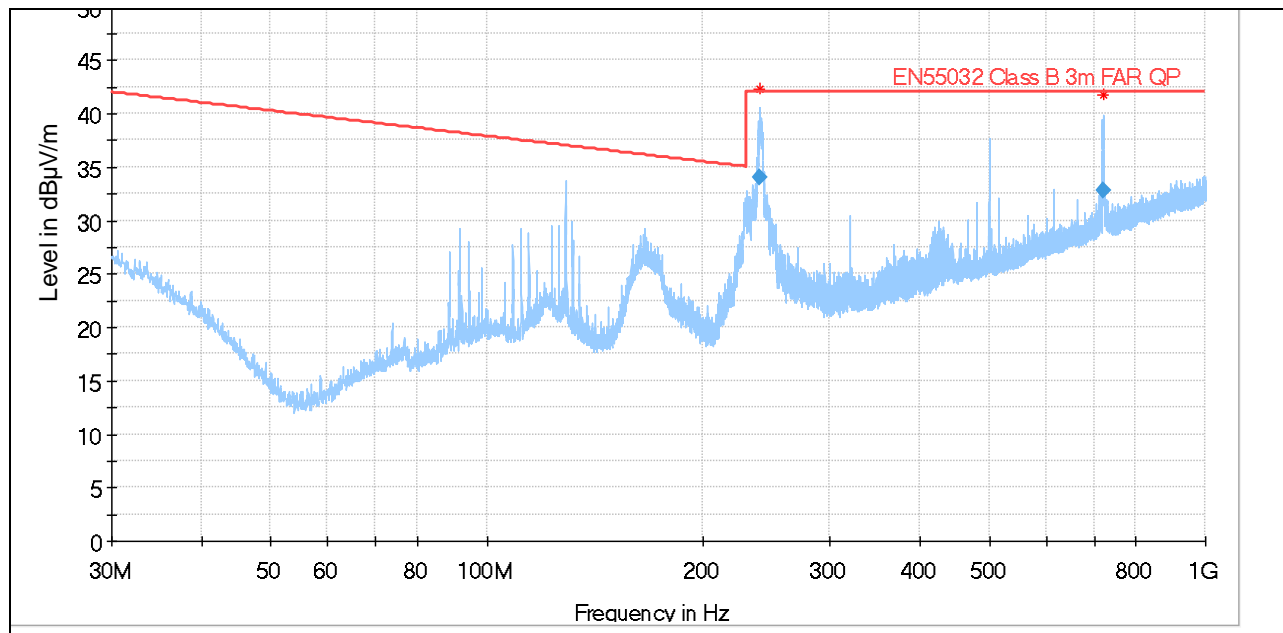
↑
From Jack Ganssle's blog – worth checking out!



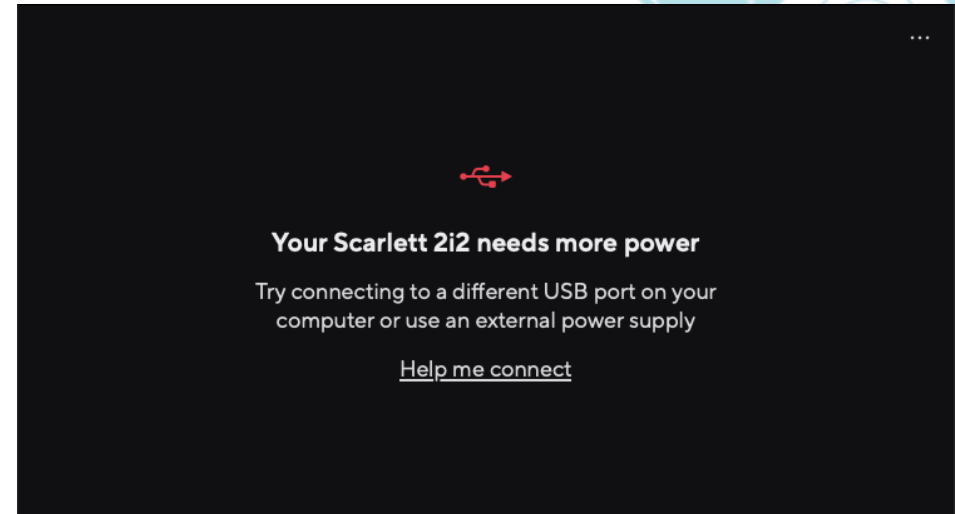
**Sometimes *we* cause
the problems for
ourselves**



Playing nicely with others



Standards help, but the goal is a good user experience



Embedded Software Development

A wild ride!

Focusrite Group

Focusrite

novation

Focusrite PRO

Ampify Music

Oberheim

Sonnox

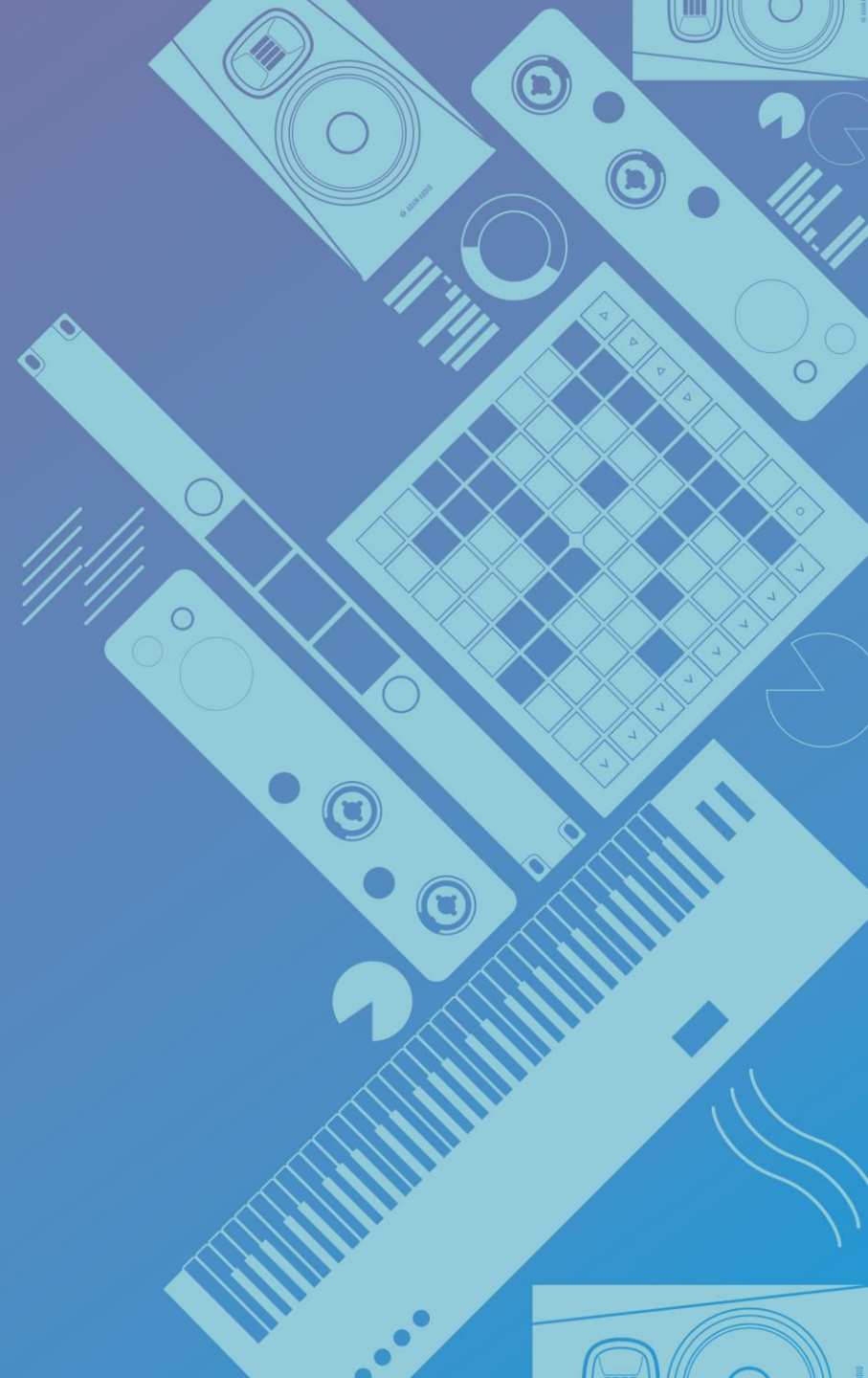
ADAM AUDIO

MARTIN AUDIO

Optimal Audio

SEQUENTIAL

LINEA
RESEARCH



We're Hiring!

Focusrite Group

