802.11b/g/n Single-Chip Wi-Fi Micro Controller

M88WI6800-K

Data Sheet

Revision Number: 1.0
Revision Date: August 15, 2017

Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH MONTAGE PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN MONTAGE'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, MONTAGE ASSUMES NO LIABILITY WHATSOEVER, AND MONTAGE DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF MONTAGE PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Montage may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Montage reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Other names and brands may be claimed as the property of others.

Do not disclose or distribute to any third party without written permission of Montage.

Preface

This data sheet is the primary reference for the 802.11b/g/n Single-Chip Wi-Fi Micro Controller - M88WI6800-K. It includes complete pin information, functional description, register description and electrical specifications for engineers who may evaluate or use the device.

Conventions

The following conventions are used in this data sheet for easy and effective explanation.

- Cross-references are highlighted in blue for your attention. You can click on them to jump to the target pages.
- Number representation
  - A hexadecimal number is represented by xxxxH or n'hxxxx (h/H: hexadecimal; n: number of bits).
  - A binary number is represented by xxxxB or n'bxxxx (b/B: binary; n: the number of bits). Sometimes the binary number with only one bit is also represented by '0' or '1'.
  - Other numbers should be considered as decimal numbers unless otherwise stated.

Terms and Abbreviations

Term	Definition	Term	Definition
ADC	Analog to Digital Converter	PHY	Physical layer device
AGC	Automatic Gain Control	QoS	Quality of Service
AMPDU	Aggregated MAC Protocol Data Unit	RF	Radio Frequency
AP	Access Point	SDR	Single Data Rate
BBP	Baseband Processor	SNAP	Subnetwork Access Protocol
BOM	Bill of Material	SPI	Serial Programming Interface
DDR	Dual Data Rate	TR	Transmit / Receive (T/R)
LAN	Local Area Network	UART	Universal Asynchronous Receiver/Transmitter
LLC	Logical Link Control	UDP	User Datagram Protocol
MAC	Media Access Controller	WAPI	WLAN Authentication and Privacy Infrastructure
MIC	Message Integrity Check	WEP	Wireless Encryption Protocol
MSDU	MAC Service Data Unit	WLAN	Wireless Local Area Network
NAT	Network Address Translation	WMM	Wi-Fi Multimedia
NVRAM	Non-Volatile Random Access Memory	WMM-PS	WMM-Power Save
OS	Operating System	WPA	Wi-Fi Protected Access
PA	Power Amplifier	WPS	Wi-Fi Protected Setup

Revision History

Revision Number	Revision Date	Changes	
		Page Number	Description
1.0	August 15, 2017	-	Modify pin out for production test.
0.1	Nov. 17, 2016	-	Change Part Number from ***M88WI8000*** to ***M88WI6800-K.***
0.0	July 15, 2016	-	Initial Release

Table of Contents

List of Tables

List of Figures

802.11b/g/n Single-Chip Wi-Fi Micro Controller
M88WI6800-K

Features

Wi-Fi:

- Compatible with IEEE 802.11 b/g/n standards
  - 802.11b: 1, 2, 5.5, 11Mbps;
  - 802.11g: 6, 9, 12, 24, 36, 48, 54Mbps;
  - 802.11n: Support PHY rate up to 150Mbps.
- Support 1T1R, 20MHz/40MHz bandwidth operation
- Integrated MAC/BB/RF/PA, TR switch & Balun
- Integrated Auto Calibration
- Integrated high-efficiency DC-DC converter
- Integrated OTP NVRAM for adapter information
- Support TCP/IP Transparent Transmission
- Support Soft-AP, Station & AP/Station modes; QoS-WMM, WMM-PS; Wi-Fi Direct
- Support TCP/IP Transparent Transmission
- Security support for 64/128 WEP, WPA, WPA2, WAPI, TKIP
- Support multiple BSSID
- Support protocols offload

Micro Processor:

- 32-bit micro processor with over 200MIPS
- User programmable memory larger than 100 kBytes
- 32 kHz watchdog timer

Peripheral Interfaces:

- 17 usable GPIOs with interrupt support
- 4 hardware PWM drivers with 8-bit duty cycle resolution
- 2 12-bit AD converters
- Multiplexed UART ports
- Multiplexed SPI Flash interface
- AT command can be supported by UART

Package:

- 6x6mm QFN48

Applications

- Internet of Things
- Industrial control
- Home automation
- Smart plug
- Lighting / Metering
- Network consumer devices

General Description

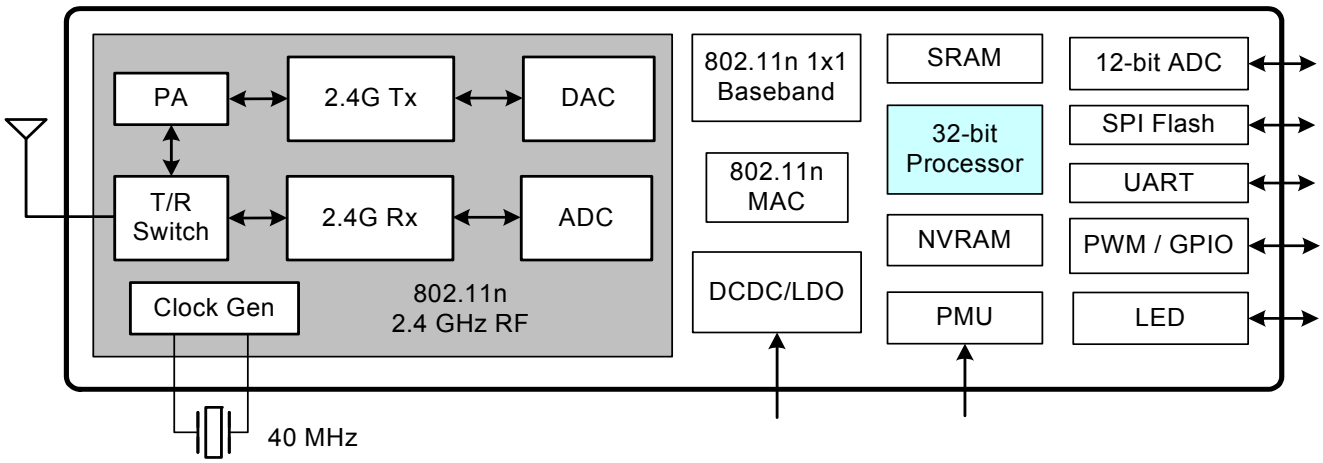
M88WI6800-K is a single-chip Wi-Fi micro controller with SPI Flash / UART interface. The chip fully complies with IEEE 802.11b/g/n 1T1R 2.4 GHz standards.

M88WI6800-K integrates a 32-bit micro processor, a 802.11n MAC, a baseband processor and a 2.4 GHz RF transceiver including power amplifier, low noise amplifier and RF T/R switch into a single die. Robust RF calibration algorithms, such as IQ-imbalance correction, Tx LO leakage removal and Rx DC offset cancellation, are built-in to alleviate the radio front-end impairments in RF/Analog circuits. The baseband processor, designed with adaptive channel estimation, enhanced boundary detector and soft-decision Viterbi decoder, is capable of providing mitigation even in severe multi-path environments. The 32-bit processor core with over 200MIPS and over 100 kByte programmable memory is embedded with TCP/IP protocol stack. In addition, the chip comes with 32 kHz low-speed clock timers, 2 12-bit ADCs with voltage range of 0 V - 3.3 V, 4 channel hardware PWM drivers with tunable frequency range and maximum 17 GPIOs with interrupt control. It contains also a power management unit and a high-efficiency DC-DC converter for cost effective system implementation.

M88WI6800-K is available in 6x6mm QFN48 package. It is an ideal solution for network enabled applications, such as Internet of Things, with few external circuit components and minimized PCB size. The networking system built with the chip can operate in Station mode, Soft-AP mode or AP/Station mode.

Functional Block Diagram

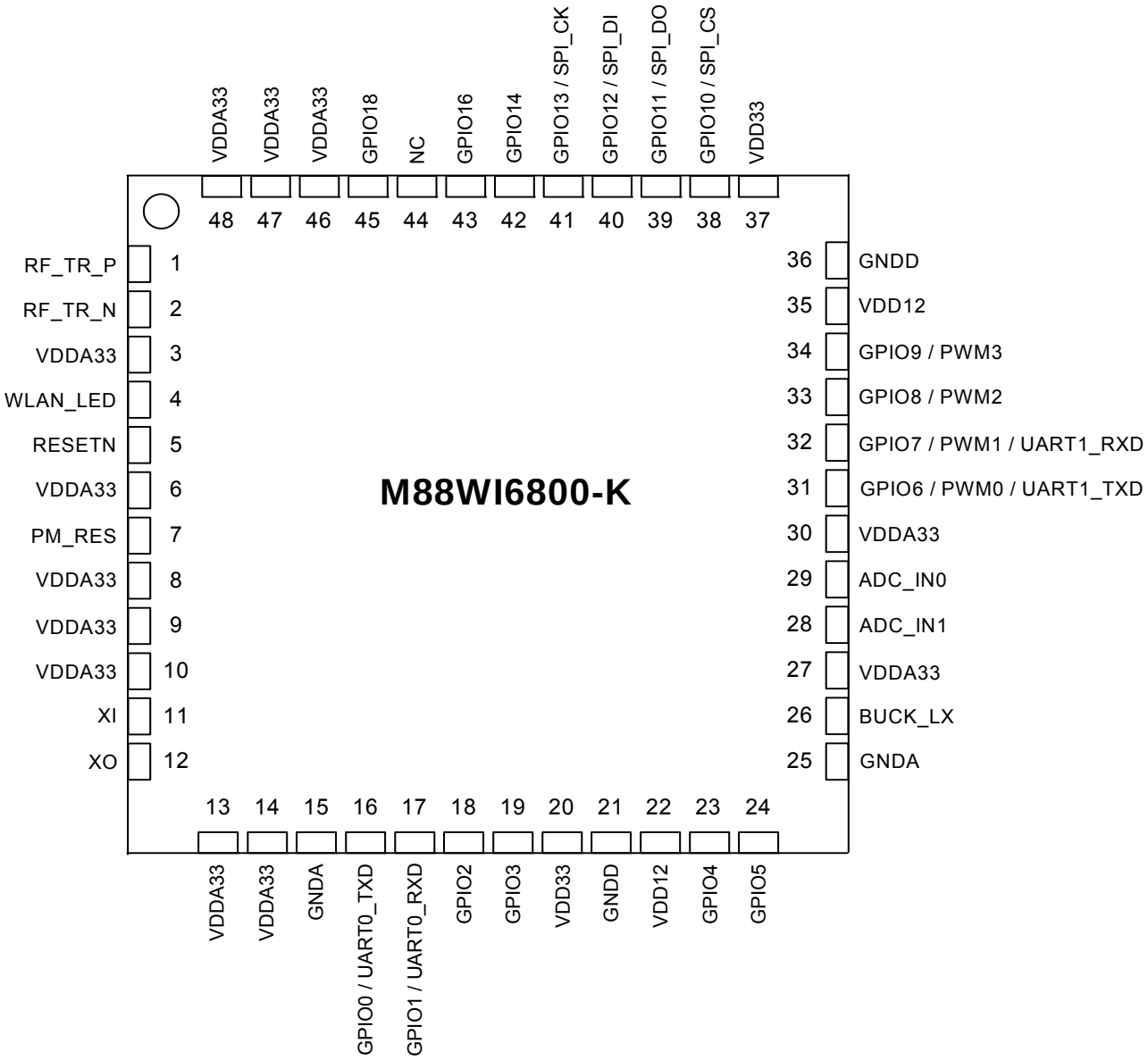
Figure 1. Functional Block Diagram for M88WI6800-K



1 Pin Information

1.1 Pin Assignment

Figure 2. QFN48 Pin Assignment



1.2 Pin List

Table 1. Signals By Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	RF_TR_P	13	VDDA33	25	GNDA	37	VDD33
2	RF_TR_N	14	VDDA33	26	BUCK_LX	38	GPIO10 / SPI_CS
3	VDDA33	15	GNDA	27	VDDA33	39	GPIO11 / SPI_DO
4	WLAN_LED	16	GPIO0 / UART0_TXD	28	ADC_IN1	40	GPIO12 / SPI_DI
5	RESETN	17	GPIO1 / UART0_RXD	29	ADC_IN0	41	GPIO13 / SPI_CK
6	VDDA33	18	GPIO2	30	VDDA33	42	GPIO14
7	PM_RES	19	GPIO3	31	GPIO6 / PWM0 / UART1_TXD	43	GPIO16
8	VDDA33	20	VDD33	32	GPIO7 / PWM1 / UART1_RXD	44	NC
9	VDDA33	21	GNDD	33	GPIO8 / PWM2	45	GPIO18
10	VDDA33	22	VDD12	34	GPIO9 / PWM3	46	VDDA33
11	XI	23	GPIO4	35	VDD12	47	VDDA33
12	XO	24	GPIO5	36	GNDD	48	VDDA33

1.3 Pin Description

Table 2. Pin Description (Sheet 1 of 2)

Pin Name	Pin No.	Type[1]	Description
RF Transceiver Interface			
RF_TR_P	1	RF	Differential RF input/output (plus), or Single-ended RF input/output.
RF_TR_N	2	RF	Differential RF input/output (minus), or GNDA for Single-ended mode.
DCDC Converter Interface			
BUCK_LX	26	AO	Analog output of DCDC converter.
ADC Input Interface			
ADC_IN1	28	AI	Analog input 1 of ADC.
ADC_IN0	29	AI	Analog input 0 of ADC.
GPIOs			
GPIO[3:0]	19,18,17,16	I/O	General purpose input/output pins.
GPIO[5:4]	24,23	I/O	General purpose input/output pins.
GPIO[9:6]	34,33,32,31	I/O	General purpose input/output pins.
GPIO10	38	I/O	General purpose input/output pin. This is also a Boot-strap pin which should be pulled **High**.
GPIO11	39	I/O	General purpose input/output pin. This is also a Boot-strap pin which should be pulled **Low**.
GPIO12	40	I/O	General purpose input/output pin.
GPIO13	41	I/O	General purpose input/output pin. This is also a Boot-strap pin which should be pulled **Low**.
GPIO18, GPIO16, GPIO14	45,43,42	I/O	General purpose input/output pins.
Multiplexed UART Interfaces			
UART0_RXD	17	I	UART receive pin. This pin is multiplexed with GPIO1.
UART0_TXD	16	O	UART transmit pin. This pin is multiplexed with GPIO0.
UART1_RXD	32	I	UART receive pin. This pin is multiplexed with GPIO7. It shall be connected to an external pulled-up resistor of 10 kΩ.
UART1_TXD	31	O	UART transmit pin. This pin is multiplexed with GPIO6.
Multiplexed PWM Drivers			
PWM[3:0]	34,33,32,31	O	PWM driver outputs. These pins are multiplexed with GPIO[9:6].

Table 2. Pin Description (Sheet 2 of 2)

Pin Name	Pin No.	Type[1]	Description
Multiplexed SPI Flash Interface			
SPI_CS	38	O	SPI flash device selection signal output. This pin is multiplexed with GPIO10.
SPI_DO	39	O	SPI flash data output line. This pin is multiplexed with GPIO11.
SPI_DI	40	I	SPI flash data input line. This pin is multiplexed with GPIO12.
SPI_CK	41	O	SPI flash clock output. This pin is multiplexed with GPIO13.
LED Driver			
WLAN_LED	4	I/O	WLAN activity LED driver. The WLAN LED blinks when there is traffic on the port. This is also a Boot-strap pin which should be pulled **Low**.
XTAL, System Control & Miscellaneous			
XI	11	AI	40 MHz quartz crystal input, or 40 MHz reference clock input with XO pin left floating.
XO	12	AO	40 MHz quartz crystal output.
RESETN	5	I	External chip reset. Active Low. The pin shall be connected to an external pulled-up resistor of 10 kΩ. When asserted as low for over 10 ms, the chip will be reset.
PM_RES	7	AIO	Reference resistor. A 1.2 kΩ resistor in 1% is required to be tied to ground.
Power & Ground			
VDD33	20,37	Power	3.3 V power supply for digital I/O pads.
VDD12	22,35	Power	1.2 V power supply for digital core.
VDDA33	3,6,8,9,10,13,14, 27,30,46,47,48	Power	3.3 V power supply for analog part.
GNDD	21,36	Ground	Digital ground.
GNDA	15,25	Ground	Analog ground.
Others			
NC	44	-	No connection.

1. In the Type column: “I” stands for Digital Input; “O” for Digital Output; “I/O” for Digital Input/Output; “AI” for Analog Input; “AO” for Analog Output; “AIO” for Analog Input/Output.

2 Function Description

M88WI6800-K is a single-chip Wi-Fi micro controller with SPI Flash and UART interfaces. It fully complies with IEEE 802.11b/g/n 1T1R 2.4 GHz standards. It is designed in high integration, which contains Power Management Unit (PMU), T/R switch, RF Balun, PA, etc. in an QFN48 package.

The chip can operate in Station, Soft-AP or AP/Station mode with 2 ADC inputs, 4 hardware PWM drivers and max. 17 GPIOs for various networking application scenarios, such as Internet of Things (LoT), industrial control, home automation, etc.

This chapter introduces the function of the main modules and peripheral interfaces of the chip.

2.1 System Clock Generation

The chip is designed with two sets of clock systems:

1. A PLL based clock generation system to generate clocks for different modules.
2. An Always On oscillator (AON_OSC) module to generate 32 kHz clock for PMU (Power Management Unit) and Always On modules.

The PLL clock generation system requires a reference clock of 40 MHz +/-20ppm which can be provided in two ways:

- Connect an external quartz crystal between XI pin and XO pin, or;
- Connect an external 40 MHz clock source to the pin XI with the pin XO left floating.

2.2 Power Management

For power saving purpose, the chip integrates a Power Management Unit (PMU) to manage the power supplies on different power domains according to the system operating modes. The main features of PMU are shown as followings:

- Use crystal oscillator clock (40 MHz) in Standby mode.
- Use AON_OSC (32 kHz) in Sleep mode.
- The AON_OSC is asked to do calibration once before entering Sleep mode.
- In charge of waking up the DCDC converter
- In charge of waking up the system
- Autonomy wake-up and programmable wakeup cycle
- Detection of external wake-up events

2.2.1 Low Power Modes

The PMU supports several low power modes & operation states to minimize the power consumption of the chip without compromising any system functionality. The states of PMU are readable by register PMU_SM[4:0] (b4~0, 000C_0850H). The operation details are defined as below:

- **PowerUp state:**
  - When VDD_3P3V is valid, PMU turns to PowerUp state.
  - At PowerUp state, all boot-strap states are latched into the corresponding registers.
  - The chip decides the operation modes at PowerUp state.
  - The chip loads SPI flash code into SRAM if the boot-strap register bit is set.

- **Standby Mode**: In this mode:
  - All power modules are enabled.
  - All clock modules are enabled.
  - All necessary clocks are enabled.
  - The chip is running at full-speed clock rate.
  - The mode is the default state after power-up.
  - The PMU operates with 40 MHz crystal.
  - CPU only runs in this mode.
- **Power Down (PD) Mode**: In this mode:
  - All power modules and functional blocks are disabled.
  - The chip goes to Sleep mode when it leaves from Power Down mode.
- **Sleep Mode**: In this mode:
  - The chip enters Sleep mode when the corresponding register bit SLP_ON_REG (b5, 000C_0850H) is set. Users can read the status at this bit of register PMU_CTRL_REG (000C_0850H).
  - The chip keeps the minimum power consumption for automatic wakeup.
  - The following functions are still enabled and the functions other than those mentioned below are turned off.
    - POR
    - PMU (Power Management Unit)
    - AON_LDO
    - AON_OSC
    - Memory content retain
  - PMU operates with 32 kHz AON_OSC.
  - PMU supports the programmable sleep timer.
  - The sleep timer starts at Sleep mode.
  - PMU wakes up the system when the sleep timer times up.
  - The chip exits from Sleep mode when the sleep timer times up or a wakeup event is detected.
  - The chip enters Sleep mode when the sleep event is set in bit 5 of register PMU_CTRL_REG (000C_0850H).

2.2.2 Wakeup

The chip can exit from Sleep mode automatically once either of the following events happens. All wakeup events are latched into the wakeup status register sets and these events could wake up the system if the corresponding interrupt bit is enabled. Please refer to the register PMU_INT_REG (000C_0864H) for more information.

- Sleep Timer Wakeup
- GPIO (GPIO4 Transition) Wakeup

- **Sleep Timer Wakeup**

Sleep Timer Wakeup provides the system a cycling wakeup mechanism. S/W uses the function to wake up the chip periodically by checking the Wi-Fi beacon packets or the status of peripheral devices. S/W will continue sleep status if no service is detected. The register SLP_TME_CTRL_REG (000C_0869H) is used to control the function.

- **GPIO4 Wakeup**

An embedded host can use GPIO4 to wake up the chip from Sleep mode. The host should send 10 clock cycles to indicate the wakeup request. It sends the wakeup request to PMU when it detects the event, and then PMU starts the wakeup procedure.

2.2.3 Timers

There are 3 types of timer in the chip:

- 24-bit Sleep Timer in unit of 32 kHz
- 24-bit RTC Timer in unit of 32 kHz
- 24-bit WatchDog Timer in unit of 32 kHz

- **Sleep Timer**

Users can set the register SLP_TMR_SETTING[23:0] (b23~0, 000C_0868H) to decide the expected sleep time. Sleep Timer starts down counting when the corresponding bit SLP_TMR_EN (b24, 000C_0868H) is set and the chip is operating in Sleep mode. The sleep timer can be reloaded with the bit SLP_TMR_SETTING automatically when it counts down to zero. The timer counts at the clock frequency of 32 kHz. This means that the maximum sleep time is 524 seconds. The register SLP_TMR_CTRL_REG (000C_0868H) can be read for the operation.

- **RTC Timer**

RTC timer is used as a real time clock for S/W to get the real clock in chip. The timer counts up every cycle at 32 kHz rate. And it is reset when the timer expires or the register bit RTC_CLK_CLR (b26, 000C_086CH) is set to 1. Please refer to RTC_CLK_REG (000C_086CH) for the register operation.

- **Watchdog Timer**

By default, Watchdog Timer is enabled and the timer setting is 4E2000H which indicates 10 seconds. The timer counts every cycle at 32 kHz rate. S/W must write to SLP_WDOG_TMR[23:0] (b23~0, 000C_0870H) to reload the timer value before expiration. The chip is reset with all registers and boot-strap status returned to default when the timer expires. Sleep Timer should be set to wake up the chip before Watchdog Timer expiration. Please refer to WDOG_TMR_CTRL_REG (000C_0870H) for the register setting in detail.

2.3 Reset

The chip supports 3 types of hardware reset.

- POR (Power On Reset)
- Watchdog Timer Reset (Refer to Section 2.2.3, "Timers")
- External RESETN triggered reset

2.3.1 Power On Reset

A POR (Power On Reset) circuit is built in the chip, which resets all circuits at the power-up duration. The power supply of POR is derived from VDDA33 (3.3 V) for MADC. POR is successful when VDDA33_MADC drops down to a valid low level (< 0.2 V). In addition, the digital H/W reset circuit extends the reset pulse until the PLL is stable and I/O input level is valid.

2.3.2 External RESETN Triggered Reset

The device has a dedicated pin, RESETN, for receiving reset signal from an external chip. Pin RESETN is low active and it shall be connected to an external pulled-up resistor of 10 kΩ. Under all operating conditions, when this pin asserted as low for over 10 ms, the chip will be reset.

2.4 CPU Core

The chip employs a 32-bit RISC processor as CPU Core. The 32-bit processor core comes with over 200MIPS and over 100 KByte SRAM. The core has an AHB system bus interface and dedicated buses for the on-chip instruction and data memories. It includes 16 general purpose registers (GPRs), a tick-timer (TTimer), a programmable interrupt controller (PIC) and an advanced power management unit (PMU).

The main features of the high-performance CPU core are shown as below:

- 32-bit RISC @ 150 MHz
- 5-stage pipe line
- Up to 1.727 DMIPS/MHz
- Variable length (16/24/32/48 bits) instruction encoding
- Super dense instruction set, single-cycle instruction execution on most instructions
- 16 Configurable general purpose registers (GPRs)

2.5 RF Transceiver Interface

The RF transceiver in the chip mainly consists of a 2.4 GHz receiver (Rx) path, a 2.4 GHz transmitter (Tx) path and a frequency synthesizer for channel LO frequency generation, and broadband ADC's & DAC's. With the on-chip Balun and TR switch, the Rx path and Tx path are combined in a single RF port for simple RF matching and minimal BOM cost. RF signal is received or transmitted via RF_TR_P & RF_TR_N pins in differential mode or via RF_TR_P pin in single ended mode. As per 802.11 b/g/n standards, the RF transceiver supports the following channel frequencies in 2.4 - 2.5 GHz band:

Table 3. Supported Channel Frequencies

Channel No.	Frequency (MHz)	Channel No.	Frequency (MHz)
1	2412	8	2447
2	2417	9	2452
3	2422	10	2457
4	2427	11	2462
5	2432	12	2467
6	2437	13	2472
7	2442	14	2484

The Rx path receives RF signals, down-converts the RF signals to I/Q baseband signals and then digitizes the baseband signals in the broadband ADC's to interface to the digital baseband processor, where sampling clocks of the ADC's are generated in the PLL based clock generation system. Low noise amplifier, IQ down-conversion mixers, channel select filters and programmable gain amplifiers are implemented in the Rx path with necessary automatic gain control (AGC). The Rx path meets all the requirements of sensitivity, SNDR, adjacent channel interference rejection and dynamic range.

In the Tx path, digital baseband signals are converted into IQ analog baseband signals in the broadband DAC's, up-conversion mixers convert the analog baseband signals to RF signals at 2.4 - 2.5 GHz. Fully integrated power amplifier provides the required output power at RF port. The Tx path fulfills stringent EVM's, spectrum masks and spurious emissions at 11b/g/n modes.

The frequency synthesizer is based on advanced PLL architecture with on-chip LC voltage-controlled oscillator (VCO) and 40 MHz crystal oscillator for reference frequency. All channel LO frequencies, as listed in Table 3, are generated after self-calibration for low phase noise and optimal Rx & Tx operations.

In addition, to alleviate impairments in RF & analog circuits, programmable calibration paths and algorithms are built-in in the RF transceiver and digital baseband processor, for IQ imbalance correction for both Rx and Tx paths, LO leakage removal for Tx path, and DC offset cancellation.

2.6 802.11n MAC & Baseband

The major function of 802.11n MAC is to meet the high throughput requirement under the constraint of the 802.11e QoS specifications. The MAC also supports 802.11i for security and 802.11n for enhanced MAC protocol efficiency. Packet aggregation, such as A-MPDU, is employed to enhance the MAC protocol efficiency greatly. The MAC consists of Low MAC (LMAC) and Upper MAC (UMAC). LMAC provides a bridge function between UMAC and Base Band (BB). UMAC transfers 802.11n frame data between Packet buffer pool in SRAM and LMAC, and performs frame queue control according to software commands.

The BB processor is a 1T1R capable baseband that implements OFDM with 1 transmit and 1 receive paths. It is compatible with the IEEE 802.11n specification. The highly integrated demodulator supports IEEE 802.11b/g/n data rates and can process the modulation and coding schemes (MCS) from 0 to 7 along with 32 in 802.11g/n. The BB processor is built with an enhanced boundary detector, an adaptive channel estimation equalizer and a soft-decision Viterbi decoder, to alleviate severe multi-path effects and mutual interference when receiving multiple streams.

2.7 SPI Flash Interface

The chip can connect to an external serial flash or other possible SPI slaves through the SPI flash interface. The SPI flash interface is multiplexed with GPIO pins. When the SPI flash interface is enabled, the chip works in SPI host mode by default.

2.8 UART Interface

The UART interface provides a flexible and low speed communication channel between wireless media and other control units such as a micro-controller. The UART interface supports baud rate ranging from 2400 bps to 115200 bps.

2.9 LED Driver

The chip supports LED indication for the RF transceiver port. When there is traffic on the port, WLAN LED will blink.

2.10 PWM Output

The chip also provides four channels of PWM outputs to drive fancy LEDs. The pins PWM[3:0] are multiplexed with GPIOs.

The PWM outputs can be enabled via the corresponding register bit (PWM0~3_EN). The PWM's cycle period and duty cycle are also programmable via registers PWM1_REG (000C_0010H) & PWM2_REG (000C_0014H). Please refer to below for details.

1. Set the PWM generation mode (auto mode or non-auto mode) in the corresponding register bit CH0~3_AUTO_MODE.
2. Set the maximum prescalar value in register PRESCALAR_MAX[7:0].
   Prescalar pulse period = system clock cycle * PRESCALAR_MAX[7:0]
3. Set the register CH0~3_SWEEP_FREQ[2:0] to chose the sweep period and decide the tick time and PWM cycle time.
   – For auto mode: Tick time = Prescalar pulse period

For non-auto mode: Tick time = Prescalar pulse period * Tick_max
Where, Tick_max depends on CH0~3_SWEEP_FREQ[2:0].

- PWM cycle time = Tick time * 32
  PWM cycle time = Tick time * 32

4. For non-auto mode, the PWM duty cycle is set in registers CH0~3_DUTY_CYCLE[4:0].
   For auto mode, the PWM duty cycle is controlled by registers CH0~3_SWEEP_FREQ[2:0]

3 Register Information

3.1 Register Attribute

Table 4. Register Attribute

Register Attribute	Description
R or RO	Read-only register: Register bits are read-only and cannot be altered by software or any reset operation. Writes to these bits are ignored.
RW	Read-Write register: Register bits are read-write and may be either set or cleared by software to the desired state.
W or WO	Write-only register. It is not physically implemented register. Rather, it is an address at which registers can be written.
RWC	Register bits are read-write and can be cleared by software writing '1' to these bits.

3.2 Register Map

Table 5. Register Map (Sheet 1 of 4)

Address (Hex)	Register Name	Width /Bits	Register Description
PWM Registers			
000C_0010H	PWM1_REG (PWM1 Control Register)	32	Page 50
000C_0014H	PWM2_REG (PWM2 Control Register)	32	Page 51
PMU Registers			
000C_0804H	GPIO_FUN_EN (GPIO Enable Bits)	32	Page 17
000C_0808H	GPIO_ODS_REG (GPIO Output Data Set Register)	32	Page 17
000C_080CH	GPIO_ODC_REG (GPIO Output Data Clear Register)	32	Page 17
000C_0810H	GPIO_OEN_REG (GPIO Output Enable Register)	32	Page 17
000C_0814H	GPIO_ID_REG (GPIO Input Data Register)	32	Page 18
000C_0818H	GPIO_OD_REG (GPIO Output Data Register)	32	Page 18
000C_081CH	GPIO_TMR_CTRL_REG (GPIO Common Control Register)	32	Page 18
000C_0820H	GPIO_IE_CTRL_REG (GPIO Input Enable Control Register)	32	Page 19
000C_0824H	GPIO_DRV_BIT0_REG (GPIO Bit0 of Drive Strength Register)	32	Page 19
000C_0828H	GPIO_DRV_BIT1_REG (GPIO Bit1 of Drive Strength Register)	32	Page 19
000C_082CH	GPIO_SMTEN_CTRL_REG (GPIO Schmitt Control Register)	32	Page 19
000C_0830H	PIO_RPU (GPIO Pull-up Control Register)	32	Page 20
000C_0834H	PKG_MODE_CTRL_REG (Package Mode Control Register)	32	Page 20
000C_0838H	RESERVED	32	Page 21
000C_0850H	PMU_CTRL_REG (PMU Control Register)	32	Page 21
000C_0854H	SLP_PD_CTRL_REG (Sleep Power Down Control Register)	32	Page 21
000C_0858H	SLP_CLK_CTRL_REG (Sleep Clock Control Register)	32	Page 23
000C_085CH	STDBY_PD_CTRL_REG (Standby Power Down Control Register)	32	Page 25

Table 5. Register Map (Sheet 2 of 4)

Address (Hex)	Register Name	Width /Bits	Register Description
000C_0860H	STDBY_CLK_CTRL_REG (Standby Clock Control Register)	32	Page 26
000C_0864H	PMU_INT_REG (PMU Interrupt Register)	32	Page 28
000C_0868H	SLP_TMR_CTRL_REG (Sleep Timer Control Register)	32	Page 28
000C_086CH	RT_CLK_REG (Real Time Clock Control Register)	32	Page 28
000C_0870H	WDOG_TMR_CTRL_REG (Watchdog Timer Control Register)	32	Page 29
000C_0878H	SLP_ISO_CTRL (Sleep Isolation Control Register)	32	Page 29
000C_0880H	GPIO_INT_RISING_REG	32	Page 30
000C_0884H	GPIO_INT_FALLING_REG	32	Page 30
000C_0888H	GPIO_INT_HIGH_REG	32	Page 30
000C_088CH	GPIO_INT_LOW_REG	32	Page 31
000C_0890H	GPIO_INT_MASK_REG	32	Page 31
000C_0894H	GPIO_INT_STS_REG	32	Page 31
000C_089CH	RESERVED	32	Page 31
000C_08A0H	RESERVED	32	Page 32
000C_08A4H	PWRUP_WAIT_XTAL	32	Page 32
000C_08A8H	PWRUP_WAIT_BUCK	32	Page 32
000C_08ACH	PWRUP_WAIT_PLL	32	Page 32
000C_08B0H	WAKEUP_WAIT_XTAL	32	Page 32
000C_08B4H	WAKEUP_WAIT_BUCK	32	Page 33
000C_08B8H	WAKEUP_WAIT_PLL	32	Page 33
000C_08BCH	SLP_CLK2ISO_DLY	32	Page 33
000C_08C0H	SLP_ISO2PDN_DLY	32	Page 33
000C_08C4H	WAKEUP_PDN2ISO_DLY	32	Page 34
000C_08C8H	RF_REG_CTRL	32	Page 34
000C_08CCH	RF_WT_RCOV_TIME	32	Page 34
000C_08D0H	RF_CTRL_REG	32	Page 35
PLL Registers			
000C_0A00H	PLL_CTRL1_REG	32	Page 35
000C_0A04H	PLL_CTRL2_REG	32	Page 36
000C_0A08H	CLKGEN_RSVD_REG	32	Page 36
000C_0A0CH	CLKGEN_CTRL_REG	32	Page 36
000C_0A10H	ADC_CTRL_REG	32	Page 37
000C_0A14H	CPU_CLK_CTRL_REG	32	Page 38
000C_0A18H	AXI_CLK_CTRL_REG	32	Page 39
000C_0A1CH	WIFI_CLK_CTRL_REG	32	Page 40
000C_0A20H	WIFI_DAC_SETTING	32	Page 41
000C_0A24H	WIFI_ADC_SETTING	32	Page 41

Table 5. Register Map (Sheet 3 of 4)

Address (Hex)	Register Name	Width /Bits	Register Description
000C_0A34H	ATE_ADC_CTRL_REG	32	Page 42
000C_0A38H	ATE_DAC_CTRL_REG	32	Page 43
MADC Control Registers			
000C_0C00H	MADC_CTRL0_REG	32	Page 43
000C_0C08H	MADC_DATA_REG	32	Page 44
000C_0C1CH	MADC_IQ_SM_REG	32	Page 44
000C_0C20H	DCC_REG	32	Page 44
000C_0C24H	SDMI_REG	32	Page 45
000C_0C28H	SDMQ_REG	32	Page 45
Timer Registers			
000C_2000H	TIMER1_L (Timer1 Counter Register)	32	Page 45
000C_2004H	TIMER1_H (Timer 1 Cycle Time Setting Register)	32	Page 45
000C_2008H	TIMER1_PRESCALER (Timer 1 Prescaler Register)	32	Page 46
000C_200CH	TIMER1_CTRL	32	Page 46
000C_2010H	TIMER1_STATUS	32	Page 46
000C_2014H	TIMER2_L	32	Page 46
000C_2018H	TIMER2_H	32	Page 47
000C_201CH	TIMER2_PRESCALAR	32	Page 47
000C_2020H	TIMER2_CTRL	32	Page 47
000C_2024H	TIMER2_STATUS	32	Page 47
UART Registers			
000C_1000H	UART1_STATUS	32	Page 48
000C_1004H	UART1_CTRL	32	Page 48
000C_3000H	UART2_STATUS	32	Page 49
000C_3004H	UART2_CTRL	32	Page 49
SPI Flash Registers			
000C_4000H	SPI_REG0 (SPI Command Register)	32	Page 52
000C_4004H	SPI_REG1 (SPI Address Register)	32	Page 52
000C_4008H	SPI_REG2 (SPI Write Data Register)	32	Page 53
000C_400CH	SPI_REG3 (SPI Read Data Register)	32	Page 53
CPU DMA Registers			
000F_4000H	CPU_DMA_CHANNEL0_CMD (Command, Length and Status of DMA Channel 0)	32	Page 53
000F_4004H	CPU_DMA_CHANNEL0_SRC_ADDR (DMA Source Address - Channel 0)	32	Page 54
000F_4008H	CPU_DMA_CHANNEL0_DST_ADDR (DMA Destination Address - Channel 0)	32	Page 54

Table 5. Register Map (Sheet 4 of 4)

Address (Hex)	Register Name	Width /Bits	Register Description
000F_4010H	CPU_DMA_CHANNEL1_CMD (Command, Length and Status of DMA Channel 1)	32	Page 55
000F_4014H	CPU_DMA_CHANNEL1_SRC_ADDR (DMA Source Address - Channel 1)	32	Page 55
000F_4018H	CPU_DMA_CHANNEL1_DST_ADDR (DMA Destination Address - Channel 1)	32	Page 55
000F_4020H	CPU_DMA_CHANNEL2_CMD (Command, Length and Status of DMA Channel 2)	32	Page 56
000F_4024H	CPU_DMA_CHANNEL2_SRC_ADDR (DMA Source Address - Channel 2)	32	Page 56
000F_4028H	CPU_DMA_CHANNEL2_DST_ADDR (DMA Destination Address - Channel 2)	32	Page 56
000F_4030H	CPU_DMA_CHANNEL3_CMD (Command, Length and Status of DMA Channel 3)	32	Page 57
000F_4034H	CPU_DMA_CHANNEL3_SRC_ADDR (DMA Source Address - Channel 3)	32	Page 57
000F_4038H	CPU_DMA_CHANNEL3_DST_ADDR (DMA Destination Address - Channel 3)	32	Page 57
000F_403CH	CPU_DMA_INT_STA_MASK (DMA Interrupt Status and Mask)	32	Page 58
000F_4040H	CPU_DMA_BOOST_SET (DMA Boost Setting Register)	32	Page 60
000F_4044H	CPU_AXI_ERR_ADDR (AXI Bus Error Address)	32	Page 61
000F_4048H	CPU_AXI_ERR_INFO (AXI Bus Error Information)	32	Page 62

3.3 Register Description

3.3.1 PMU Registers

GPIO_FUN_EN (GPIO Enable Bits)

Address: 000C_0804H Default: 003F0000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_FUN_EN_REG[18:0]	RW	The bits enable the GPIO function for each I/O respectively.

GPIO_ODS_REG (GPIO Output Data Set Register)

Address: 000C_0808H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_ODS_REG[18:0]	RWC	GPIO output data setting (to 1). Write '1' to set the corresponding GPIO bit. These bits are self-cleared after being written.

GPIO_ODC_REG (GPIO Output Data Clear Register)

Address: 000C_080CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_ODC_REG[18:0]	RWC	GPIO output data clearing bits (cleared to 0). Write '1' to clear the corresponding GPIO output data bit. These bits are self-cleared.

GPIO_OEN_REG (GPIO Output Enable Register)

Address: 000C_0810H Default: 003FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_OEN_REG[18:0]	RW	These bits are used to configure the corresponding GPIO pin as input/output port. 0: GPIO is set as output; 1: GPIO is set as input.

GPIO_ID_REG (GPIO Input Data Register)

Address: 000C_0814H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_ID_REG[18:0]	R	GPIO input value. The bits indicate the value input from the corresponding GPIO.

GPIO_OD_REG (GPIO Output Data Register)

Address: 000C_0818H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_OD_REG[18:0]	RW	GPIO output data register. S/W can write data onto GPIOs through these register bits. These register bits are updated when AHB writing onto the register is detected.

GPIO_TMR_CTRL_REG (GPIO Common Control Register)

Address: 000C_081CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:22	RESERVED	RW	Reserved
21:1	GPIO_TMR_SEL_REG[20:0]	RW	Selection of GPIO for timer interrupt input. 00000: GPIO0 00001: GPIO1 00010: GPIO2 ..... 10010: GPIO18 Others: Reserved
0	GPIO_TMR_EN	RW	The bit enables the selected GPIO as a Timer Clock Source. 0: Disabled; 1: Enabled.

GPIO_IE_CTRL_REG (GPIO Input Enable Control Register)

Address: 000C_0820H Default: 003FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved
18:0	GPIO_IE[18:0]	RW	GPIO input enable. 0: Input direction is disabled; 1: Input direction is enabled.

GPIO_DRV_BIT0_REG (GPIO Bit0 of Drive Strength Register)

Address: 000C_0824H Default: E000003FH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_DRV_BIT0[18:0]	RW	GPIO[18:0] drive strength control bits.

GPIO_DRV_BIT1_REG (GPIO Bit1 of Drive Strength Register)

Address: 000C_0828H Default: E003FFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_DRV_BIT1[18:0]	RW	GPIO[18:0] drive strength control bits. When GPIO_DRV_BIT1 & GPIO_DRV_BIT0 = : 00: 8 mA 01: 12 mA 10: 16 mA (Default) 11: 20 mA

GPIO_SMTEN_CTRL_REG (GPIO Schmitt Control Register)

Address: 000C_082CH Default: E0000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_SMTEN[18:0]	RW	Schmitt enable bits. The register does not effect GPIO0 ~ GPIO5. 0: Disabled. 1: Enabled.

PIO_RPU (GPIO Pull-up Control Register)

Address: 000C_0830H
Default: 0003FFFFH

Bit No.	Bit Name	Attribute	Description
31:19	RESERVED	RW	Reserved.
18:0	GPIO_RPU[18:0]	RW	Pull-up enable bits. The register does not effect GPIO0 ~ GPIO5. 0: Enabled; 1: Disabled.

PKG_MODE_CTRL_REG (Package Mode Control Register)

Address: 000C_0834H
Default: 00000C00H

Bit No.	Bit Name	Attribute	Description
31:24	RESERVED	RW	Reserved.
23	RESERVED	RW	The bit should be set to 0.
22:20	TEST_REG[2:0]	RW	Test mode setting.
19:16	RESERVED	RW	Reserved.
15	UART2_EN1	RW	UART1 enable 1. 0: UART port is disabled. 1: UART port is enabled. When enabled, PWM2 acts as UART_TXD (output) and PWM3 acts as UART_RXD (input).
14	UART2_EN0	RW	UART1 port enable 0. 0: UART port is disabled. 1: UART port is enabled. When enabled, PWM0 acts as UART_TXD (output) and PWM1 acts as UART_RXD (input).
13	RESERVED	RW	The bit should be set to 0.
12	RESERVED	RW	Reserved.
11	I2C_IF_EN	RW	I2C interface enable. The interface is multiplexed with GPIO pins. It can be enabled only when the bit is set.
10	JTAG_IF_EN	RW	JTAG interface enable. The interface is multiplexed with GPIO pins. It can be enabled only when the bit is set.
9	RESERVED	RW	Reserved.

Address: 000C_0834H Default: 00000C00H			
Bit No.	**Bit Name**	**Attribute**	**Description**
8	FLASH_HW_LOAD_EN	RW	Defines the status of boot-strap of GPIO11 for HW_LOAD_EN. 0: Disable SPI Flash H/W loading. 1: Enable SPI Flash H/W loading.
4	STATION_MODE	RW	The status of boot-strap of GPIO10 for NIC or Station mode operation. 0: NIC Mode 1: Station Mode
3	HOST_IF	RW	Host interface selection. The register latches the value of pin GPIO13. **Host I/F GPIO13** UART 0
2:0	RESERVED	RW	Reserved.

RESERVED

Address: 000C_0838H Default: 0000000FH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	RESERVED	RW	Reserved.

PMU_CTRL_REG (PMU Control Register)

Address: 000C_0850H Default: 00000002H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:6	RESERVED	RW	Reserved.
5	SLP_ON_REG	RWC	Sleep mode on. The bit is Self-Cleared. Write ‘1’ to command PMU entering Sleep Mode
4:0	PMU_SM[4:0]	R	The status of PMU state machine

SLP_PD_CTRL_REG (Sleep Power Down Control Register)

Address: 000C_0854H Default: 00019F81H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:18	RESERVED	RW	Reserved.

Address: 000C_0854H Default: 00019F81H			
Bit No.	**Bit Name**	**Attribute**	**Description**
17	SLP_QMEM0_PD	RW	QMEM0 power down control. 0: Power on; 1: Power down.
16	SLP_QMEM1_PD	RW	QMEM1 power down control. 0: Power on; 1: Power down.
15	SLP_QMEM2_PD	RW	QMEM2 power down control. 0: Power on; 1: Power down.
14:13	RESERVED	RW	Reserved.
12	SLP_RF_PD	RW	RF power down control. 0: Power on. 1: Power down.
11	SLP_MADC_PD	RW	Monitor ADC power down control. Determines the MADC function is turned on or off. 0: Power on. 1: Power down.
10	SLP_WIFI_DAC_PD	RW	Wi-Fi DAC power down control. 0: Power on. 1: Power down.
9	SLP_WIFI_ADC_PD	RW	Wi-Fi ADC power down control. 0: Power on. 1: Power down.
8	SLP_PLL_PD	RW	PLL power down control. 0: Power on. 1: Power down.
7	SLP_XTAL_PD	RW	Crystal power down control. 0: Power on. 1: Power down.
6	SLP_AON_OSC_PD	RW	AON oscillator power down control. 0: Power on. 1: Power down.
5:3	RESERVED	RW	Reserved.

Address: 000C_0854H Default: 00019F81H			
Bit No.	**Bit Name**	**Attribute**	**Description**
2	SLP_BUCK_EN	RW	Sleep DCDC converter enable. Enable DCDC converter in Sleep Mode. 1: Enable. 0: Disable.
1	SLP_AON_LDO_PD	RW	AON LDO power down control. 0: Power on. 1: Power down.
0	SLP_BUCK_PD	RW	DCDC converter power down control. 0: Power on; 1: Power down.

SLP_CLK_CTRL_REG (Sleep Clock Control Register)

Address: 000C_0858H Default: 04000C02H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:27	RESERVED	RW	Reserved.
26	SLP_USE_AON_OSC	RW	Determines whether PMU uses AON OSC in Sleep mode. 0: PMU operates with 40 MHz crystal clock. 1: PMU operates with AON OSC.
25	SLP_40M_CLK_ON	RW	The register bit is used to enable the 40 MHz reference clock. It controls the 40 MHz reference clocks of clock generator. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
24	RESERVED	RW	Reserved.
23	SLP_SPI_DAC_CLK_INV	RW	The register is used to invert DAC_CLKO which is derived from ana_top_with_IO. The register should be implemented in PMU Register Set. 0: No change. 1: Clock inverted.
22	SLP_SPI_ADC_CLK_INV	RW	The register is used to invert ADC_CLKO which is derived from ana_top_with_IO. The register should be implemented in PMU Register Set. 0: No change. 1: Clock inverted.

Address: 000C_0858H Default: 04000C02H			
Bit No.	**Bit Name**	**Attribute**	**Description**
21	SLP_BBP_11N_ON	RW	The register is used to enable Wi-Fi MAC clock source. It controls the BBP (baseband processor) clocks of clock generator. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
20	SLP_WIFI_MAC_ON	RW	The register is used to enable Wi-Fi MAC clock source. It controls the Wi-Fi clocks of clock generator. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
19	SLP_WIFI_SEC_CLK_ON	RW	The register is used to enable Wi-Fi MAC Security clock source. It controls PLL clock WIFI_MAC_SEC_CLKO of ana_top_with_IO. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
18	SLP_PLL_160M_CLK_ON	RW	The register is used to enable 160 MHz clock source. It controls PLL clock 160M_CLKO of ana_top_with_IO. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
17	SLP_AXI_CLK_ON	RW	The register is used to enable AXI Bus clock. It controls PLL clock AXI_CLKO of ana_top_with_IO. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
16	SLP_CPU_CLK_ON	RW	The register is used to enable CPU clock. It controls PLL clock CPU_CLKO of ana_top_with_IO. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
15:10	RESERVED	RW	Reserved.
9	SLP_BBP11N_RSTN_REG	RW	The register bit is used to reset BBP 11N function. 0: Reset. 1: Do not reset the function.

Address: 000C_0858H Default: 04000C02H			
Bit No.	**Bit Name**	**Attribute**	**Description**
8	SLP_WIFI_MAC_RSTN_REG	RW	The register bit is used to reset WIFI_MAC Bridge function. 0: Reset. 1: Do not reset the function.
7:2	RESERVED	RW	Reserved.
1	SLP_CPU_MEM_RSTN_REG	RW/HS	The register bit is used to reset CPU_MEM function. The bit is Self-Cleared after it is set to 0. 0: Reset. 1: Do not reset the function.
0	RESERVED	RW	Reserved.

STDBY_PD_CTRL_REG (Standby Power Down Control Register)

Address: 000C_085CH Default: 00001000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:13	RESERVED	RW	Reserved.
12	STDBY_RF_PD	RW	RF TX Power Down control. 0: Power on. 1: Power down.
11	STDBY_MADC_PD	RW	Monitor ADC Power Down control. 0: Power on. 1: Power down.
10	STDBY_WIFI_DAC_PD	RW	Wi-Fi DAC Power Down control. 0: Power on. 1: Power down.
9	STDBY_WIFI_ADC_PD	RW	Wi-Fi ADC Power Down control. 0: Power on. 1: Power down.
8	STDBY_PLL_PD	RW	PLL Power Down control in Standby mode. 0: Power on. 1: Power down.
7	RF_TEST_XTAL_PD	RW	XTAL Power Down control in RF test mode. 1: Power down. 0: Power on.
6	STDBY_AON_OSC_PD	RW	AON oscillator Power Down control. 0: Power on. 1: Power down.

Address: 000C_085CH Default: 00001000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
5:3	RESERVED	RW	Reserved.
2	BOOT_SLEEPING	RW	BOOT_SLEEPING Default value is 0. 0: Boot from Normal mode. 1: Boot from Sleeping mode.
1	STDBY_AON_LDO_PD	RW	AON LDO Power Down control. 0: Power on. 1: Power down.
0	RESERVED	RW	Reserved.

STDBY_CLK_CTRL_REG (Standby Clock Control Register)

Address: 000C_0860H Default: 0B3F0F02H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:27	RESERVED	RW	Reserved.
26	STDBY_USE_AON_OSC	RW	PMU uses AON OSC in Standby mode. 0: PMU operates with 40 MHz crystal clock; 1: PMU operates with AON OSC.
25	STDBY_40M_CLK_ON	RW	The register bit is used to enable 40 MHz reference clock. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
24	RESERVED	RW	Reserved.
23	STDBY_SPI_DAC_CLK_INV	RW	The register is used to invert DAC_CLKO. The register should be implemented in PMU Register Set. 0: No change. 1: Clock inverted.
22	STDBY_SPI_ADC_CLK_INV	RW	The register bit is used to invert ADC_CLKO. The register should be implemented in PMU Register Set. 0: No change. 1: Clock inverted.
21	STDBY_BBP_11N_ON	RW	The register bit is used to enable Wi-Fi MAC clock source. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.

Address: 000C_0860H Default: 0B3F0F02H			
Bit No.	**Bit Name**	**Attribute**	**Description**
20	STDBY_WIFI_MAC_ON	RW	The register bit is used to enable Wi-Fi MAC clock source. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
19	STDBY_WIFI_SEC_CLK_ON	RW	The register bit is used to enable Wi-Fi MAC Security clock source. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
18	STDBY_PLL_160M_CLK_ON	RW	The register bit is used to enable 160 MHz clock source. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
17	STDBY_AXI_CLK_ON	RW	The register bit is used to enable AXI Bus clock. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
16	STDBY_CPU_CLK_ON	RW	The register bit is used to enable CPU clock. The register should be implemented in PMU Register Set. 0: Disable clock. 1: Enable clock.
15:10	RESERVED	RW	Reserved.
9	STDBY_BBP11N_RSTN_REG	RW	The register bit is used to reset BBP 11N function. 0: Reset. 1: Do not reset the function.
8	STDBY_WIFI_MAC_RSTN_REG	RW	The register bit is used to reset WIFI_MAC Bridge function. 0: Reset. 1: Do not reset the function.
7:2	RESERVED	RW	Reserved.
1	STDBY_CPU_MEM_RSTN_REG	RW/HS	The register bit is used to reset CPU_MEM function. The bit is Self-Set after it is set to 0. 0: Reset. 1: Do not reset the function.
0	RESERVED	RW	Reserved.

PMU_INT_REG (PMU Interrupt Register)

Address: 000C_0864H Default: 00002A80H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:4	RESERVED	RW	Reserved.
3	SLP_TMR_WAKE_STATUS	RWC	Sleep timer wakeup status Writing '1' clears the bit. 0: No sleep timer wakeup event. 1: Sleep timer wakeup is detected.
2:1	RESERVED	RW	Reserved.
0	SLP_TMR_WAKE_INT_DIS	RW	Sleep timer wakeup interrupt disable. 0: Enable. 1: Disable.

SLP_TMR_CTRL_REG (Sleep Timer Control Register)

Address: 000C_0868H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:25	RESERVED	RW	Reserved.
24	SLP_TMR_EN	RW	Sleep timer enable. Set '1' to enable the timer. Set '0' to disable the timer.
23:0	SLP_TMR_SETTING[23:0]	RW	Sleep timer counter value. Unit: 32 kHz The register reflects the current value of the down counting counter and can be reloaded when writing new value to this register. SLP_TMR_WAKE_STATUS is set when the timer counts down to 0.

RT_CLK_REG (Real Time Clock Control Register)

Address: 000C_086CH Default: 01000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:27	RESERVED	RW	Reserved.
26	RTC_CLK_CLR	RW	RTC clock clear Set '1' to clear RTC. The bit is Self-Cleared.
25	RESERVED	RW	Reserved.

Address: 000C_086CH Default: 01000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
24	RTC_CLK_EN	RW	RTC clock enable.
23:0	RTC_CLK[23:0]	R	RTC clock

WDOG_TMR_CTRL_REG (Watchdog Timer Control Register)

Address: 000C_0870H Default: 0104E200H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:26	RESERVED	RW	Reserved.
25	SLP_WDOG_TMR_INT	RWC	Sleep watchdog timer interrupt Writing ‘1’ clears the interrupt.
24	SLP_WDOG_TMR_EN	RW	Sleep watchdog timer enable Set ‘1’ to enable the timer. Set ‘0’ to disable the timer.
23:0	SLP_WDOG_TMR[23:0]	RW	Sleep watchdog timer counter value Unit: 32 kHz The register reflects the current value of the down counting counter and can be reloaded when a new value is written to this register.

SLP_ISO_CTRL (Sleep Isolation Control Register)

Address: 000C_0878H Default: 0000007FH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:4	RESERVED	RW	Reserved.
3	SLP_ISO_QMEM2	RW	Isolates the signals due to QMEM2 power switch off. 0: Isolation off. 1: Isolation on.
2	SLP_ISO_QMEM1	RW	Isolates the signals due to QMEM1 power switch off. 0: Isolation off. 1: Isolation on.
1	SLP_ISO_QMEM0	RW	Isolates the signals due to QMEM0 power switch off. 0: Isolation off. 1: Isolation on.

Address: 000C_0878H Default: 0000007FH			
Bit No.	**Bit Name**	**Attribute**	**Description**
0	SLP_ISO_BUCK	RW	Isolates the signals due to DCDC converter power switch off. 0: Isolation off. 1: Isolation on.

GPIO_INT_RISING_REG

Address: 000C_0880H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_RISING_REG[18:0]	RW	These bits are used to enable the rising edge mode of GPIO INT. 0: Rising edge interrupt is disabled. 1: Rising edge interrupt is enabled.

GPIO_INT_FALLING_REG

Address: 000C_0884H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_FALLING_REG[18:0]	RW	These bits are used to enable the falling edge mode for GPIO INT. 0: Falling edge interrupt is disabled. 1: Falling edge interrupt is enabled.

GPIO_INT_HIGH_REG

Address: 000C_0888H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_HIGH_REG[18:0]	RW	These bits are used to enable the high-level mode of GPIO INT. 0: High-level interrupt is disabled. 1: High-level interrupt is enabled.

GPIO_INT_LOW_REG

Address: 000C_088CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_LOW_REG[18:0]	RW	These bits are used to enable the low-level mode for GPIO INT. 0: Low-level interrupt is disabled. 1: Low-level interrupt is enabled.

GPIO_INT_MASK_REG

Address: 000C_0890H Default: 001FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_MASK_REG[18:0]	RW	GPIO interrupt mask register bits.

GPIO_INT_STS_REG

Address: 000C_0894H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:19	RESERVED	RW	Reserved.
18:0	GPIO_INT_STS_REG[18:0]	RW	GPIO interrupt status register bits. Write ‘1’ to clear these bits. Note: GPIO Status is logic ‘OR’ with 4 types of Interrupt. We enable only one interrupt type if one type of interrupt is needed.

RESERVED

Address: 000C_089CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	RESERVED	RW	The register must be set to 0.

RESERVED

Address: 000C_08A0H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	RESERVED	RW	The register must be set to 0.

PWRUP_WAIT_XTAL

Address: 000C_08A4H Default: 0000EA60H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	PWRUP_WAIT_XTAL[19:0]	RW	Power up waiting crystal oscillator settling time. Maximum is 26.214 ms. Unit: 40 MHz

PWRUP_WAIT_BUCK

Address: 000C_08A8H Default: 00007D00H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	PWRUP_WAIT_BUCK[19:0]	RW	Power up waiting DCDC converter settling time (800 us). Unit: 40 MHz

PWRUP_WAIT_PLL

Address: 000C_08ACH Default: 00030D40H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	PWRUP_WAIT_PLL[19:0]	RW	Power up waiting PLL settling tiem (5 ms). Unit: 40 MHz

WAKEUP_WAIT_XTAL

Address: 000C_08B0H Default: 00000038H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.

Address: 000C_08B0H Default: 00000038H			
Bit No.	**Bit Name**	**Attribute**	**Description**
15:0	WAKEUP_WAIT_XTAL[15:0]	RW	Wakeup waiting crystal oscillator (XTAL) settling time (1.5 ms). Unit: 32 kHz

WAKEUP_WAIT_BUCK

Address: 000C_08B4H Default: 00000018H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.
15:0	WAKEUP_WAIT_BUCK[15:0]	RW	Wakeup waiting DCDC converter settling time (800 us). Unit: 32 kHz

WAKEUP_WAIT_PLL

Address: 000C_08B8H Default: 000000B8H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.
15:0	WAKEUP_WAIT_PLL[15:0]	RW	Wakeup waiting PLL settling time (5 ms). Unit: 32 kHz

SLP_CLK2ISO_DLY

Address: 000C_08BCH Default: 00000003H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.
15:0	SLP_CLK2ISO_DLY[15:0]	RW	Clock Off to Isolation On delay time (125 us). Unit: 32 kHz

SLP_ISO2PDN_DLY

Address: 000C_08C0H Default: 00000003H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.

Address: 000C_08C0H Default: 00000003H			
Bit No.	**Bit Name**	**Attribute**	**Description**
15:0	SLP_ISO2PDN_DLY[15:0]	RW	Isolation On to Power Down delay time (125 us). Unit: 32 kHz

WAKEUP_PDN2ISO_DLY

Address: 000C_08C4H Default: 00000003H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	RESERVED	RW	Reserved.
15:0	WAKEUP_PDN2ISO_DLY[15:0]	RW	Wakeup delay time from Power Down to Isolation Off (125 us). Unit: 32 kHz

RF_REG_CTRL

Address: 000C_08C8H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:4	RESERVED	RW	Reserved.
3	RF_PA_ON_REG	RW	RF PA_ON is controlled by the register bit when the bit RF_REG_CTRL_EN is set.
2	RF_RX_ON_REG	RW	RF RX_ON is controlled by the register bit when the bit RF_REG_CTRL_EN is set.
1	RF_TX_ON_REG	RW	RF TX_ON is controlled by the register bit when the bit RF_REG_CTRL_EN is set.
0	RF_REG_CTRL_EN	RW	The bit determines whether RF TX_ON, RXON and PA_ON are controlled by the register bits mentioned above.

RF_WT_RCOV_TIME

Address: 000C_08CCH Default: 00009C40H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:21	RESERVED	RW	Reserved.
19:0	RF_WT_RCOV_TIME[19:0]	RW	Reserved.

RF_CTRL_REG

Address: 000C_08D0H Default: 00000001H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:1	RESERVED	RW	Reserved.
0	RF_AC_RSTN	RW	RF_AC reset control. 0: Reset. 1: Do not perform reset.

3.3.2 PLL Registers

PLL_CTRL1_REG

Address: 000C_0A00H Default: 00002082H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:17	RESERVED	RW	Reserved.
16:9	PLL_FBDIV[7:0]	RW	PLL feedback divider control. 00000000: div 2^5 01000000: div 96 11111111: div 2^8-1 div<7>&div<6> = 0 divn = 2^5+div<0>*2^0+div<1>*2^1+.. div<7> & div<6> = 1 divn = div<0>*2^0 +d iv<1>*2^1+..
8:6	PLL_ICP[2:0]	RW	Charge-pump current control. 000: 10u 001: 20u 010: 30u 011: 40u 100: 50u 101: 60u 110: 70u
5	PLL_PFD_DLY	RW	PFD dead zone pulse control. 0: 130ps 1: 230ps
4:0	PLL_REF_DIV[4:0]	RW	PLL reference clock divider. 00000: div 2 (20M refclk). 00010: div 4 (40M refclk).

PLL_CTRL2_REG

Address: 000C_0A04H Default: 000017F1H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:15	RESERVED	RW	Reserved.
14	PLL_PD	RW	PLL power down signal. 0: Power up. 1: Power down.
13	PLL_RST_SOFT	RW	PLL re-calibration control: 0->1->0: Re-calibration
12	PLL_CAL_EN	RW	PLL calibration block enable. 0: Disable calibration 1: Enable calibration
11:10	PLL_CAL_EXT[1:0]	RW	External KVCO control.
9:8	PLL_CAL_TIME[1:0]	RW	PLL calibration timing control: 00: 7*64 clk cycle 01:15*64 calclk cycle 10: 31*64 calclk cycle 11: 63*64 calclk cycle
7:4	PLL_CAL_DIV[3:0]	RW	PLL calibration clock divider. divn = 1~15
3:2	PLL_CPVR_SEL[1:0]	RW	PLL charge pump reference selection.
1:0	PLL_VCO_SEL[1:0]	RW	PLL VCO CAP selection.

CLKGEN_RSVD_REG

Address: 000C_0A08H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	CLKGEN_RSVD_REG[31:0]	RW	Reserved.

CLKGEN_CTRL_REG

Address: 000C_0A0CH Default: 00000010H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:8	RESERVED	RW	Reserved.
7	CLKGEN_ATP_EN	RW	Clkgen analog test point enable. 0: Disabled. 1: Enabled.

Address: 000C_0A0CH Default: 00000010H			
Bit No.	**Bit Name**	**Attribute**	**Description**
6:5	CLKGEN_ATP_SEL	RW	Clkgen analog test point selection. 00: vref_b_test 01: vref_t_test 10: vddvco_test 11: vcon_test
4:3	CLKGEN_TEST_DIV[1:0]	RW	Test clock divider. 00: div1 01: div2 10: div4 11: div8
2:0	CLKGEN_TEST_SEL[2:0]	RW	Test clock selection. 000: Disabled 100: 0 101: 0 110: 0 111: cpu_clk_tst

ADC_CTRL_REG

Address: 000C_0A10H Default: 00026063H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:18	RESERVED	RW	Reserved.
17	MADC_CLK_EN	RW	MADC clock enable. 0: Disabled. 1: Enabled.
16	MADCCLK_NOGATE	RW	MADC clock gating control after configuration update. 0: Gating. 1: No gating.
15	MADCCLK_UPDATE	RW	Update MADC clock register setting. Setting process: 1. Change SEC clock divider setting 2. Write the update register bit from 0->1 3. Clock is valid after 5 cycles. No glitch during transition.
14:7	MADC_PREDIV[7:0]	RW	MADC clock frequency pre-divider control.

Address: 000C_0A10H Default: 00026063H			
Bit No.	**Bit Name**	**Attribute**	**Description**
6:4	MADC_POSTDIV[2:0]	RW	MADC clock frequency post-divider control. 000: div 2 001/100: div 4 010: div 6 011/100: div 8 101: div 16 110: div 24 111: div 32
3	DAC_DIVSEL160M_80M	RW	Wi-Fi DAC divider selection. 0: Output 160M DAC clock. 1: Ouput 80M DAC clock.
2	ADC_DIVSEL_480M	RW	ADC input clock setting. 0: 480M ADC input clock. 1: 240M ADC input clock.
1	ADC_CLK_EN	RW	ADC clock enable. 0: Disable. 1: Enable.
0	DAC_CLK_EN	RW	DAC clock enable. 0: Disabled. 1: Enabled.

CPU_CLK_CTRL_REG

Address: 000C_0A14H Default: 00002604H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:14	RESERVED	RW	Reserved.
13	CPU_CLK_EN	RW	CPU clock enable. 0: Disable. 1: Enable.
12	CPUCLK_NOGATE	RW	CPU clock gating control after configure update. 0: Gating. 1: No gating.

Address: 000C_0A14H Default: 00002604H			
Bit No.	**Bit Name**	**Attribute**	**Description**
11	CPUCLK_UPDATE	RW	Update CPU clock register setting. Update process: 1. Change CPU clock divider setting 2. Write the update register bit from 0->1 3. Clock is valid after 5 cycles. No glitch during transition.
10:3	CPUCLK_PREDIV[7:0]	RW	CPU clock frequency pre-divider control.
2:0	CPUCLK_POSTDIV[2:0]	RW	CPU clock frequency post-divider control. 000: div 1 001/100: div 2 010: div 3 011/100: div 4 101: div 8 110: div 12 111: div 16

AXI_CLK_CTRL_REG

Address: 000C_0A18H Default: 00002582H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:14	RESERVED	RW	Reserved.
13	AXI_CLK_EN	RW	AXI clock enable. 0: Disabled. 1: Enabled.
12	AXICLK_NOGATE	RW	AXI clock gating control after configuration update. 0: Gating. 1: No gating.
11	AXICLK_UPDATE	RW	Update AXI clock register setting Setting process: 1. Change AXI clock divider setting; 2. Write the update register bit from 0->1; 3. Clock is valid after 5 cycles. No glitch during transition.
10:3	AXI_PREDIV[7:0]	RW	AXI clock frequency pre-divider control.

Address: 000C_0A18H Default: 00002582H			
Bit No.	**Bit Name**	**Attribute**	**Description**
2:0	AXI_POSTDIV[2:0]	RW	AXI clock frequency post-divider control. 000: div 1 001/100: div 2 010: div 3 011/100: div 4 101: div 8 110: div 12 111: div 16

WIFI_CLK_CTRL_REG

Address: 000C_0A1CH Default: 00001803H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31	WIFI_DAC_SLP_REG_CTRL	RW	A ‘1’ in this bit means that Wi-Fi DAC sleep is controlled by the bit WIFI_DAC_SLP.
30	WIFI_DAC_SLP	RW	Wi-Fi DAC Sleep mode control. 0: Standby status. 1: Sleep status.
29	WIFI_ADC_SLP_REG_CTRL	RW	A ‘1’ in this bit means that Wi-Fi ADC sleep is controlled by the bit WIFI_ADC_SLP.
28	WIFI_ADC_SLP	RW	Wi-Fi ADC Sleep mode control. 0: Standby status. 1: Sleep status.
27:15	RESERVED	RW	Reserved.
14	SECCLK_NOGATE	RW	SEC clock gating control after configuration update. 0: Gating. 1: No gating.
13	SECCLK_UPDATE	RW	Update SEC clock register setting Update process: 1. Change SEC clock divider setting; 2. Write update register from 0->1; 3. Clock is valid after 5 cycles. No glitch during transition
12:5	SEC_PREDIV[7:0]	RW	SEC clock frequency pre-divider control.

Address: 000C_0A1CH Default: 00001803H			
Bit No.	**Bit Name**	**Attribute**	**Description**
4:2	SEC_POSTDIV[2:0]	RW	SEC clock frequency post-divider control. 000: div 1 001/100: div 2 010: div 3 011/100: div 4 101: div 8 110: div 12 111: div 16
1	WIFI_CLK_EN	RW	Wi-Fi clock enable. 0: Disabled. 1: Enabled.
0	SEC_CLK_EN	RW	SEC clock enable. 0: Disabled. 1: Enabled.

WIFI_DAC_SETTING

Address: 000C_0A20H Default: 00000064H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:9	RESERVED	RW	Reserved.
8	CLK_POLARITY_DAC	RW	Clock polarity control (1.2V logic). Default value is 0.
7:6	CV_DAC[1:0]	RW	Bias voltage control (1.2V logic). Default value is 01B.
5:3	CI_I_DAC[2:0]	RW	Bias current control for I channel (1.2V logic). Default value is 100B.
2:0	CI_Q_DAC[2:0]	RW	Bias current control for Q channel (1.2V logic). Default value is 100B.

WIFI_ADC_SETTING

Address: 000C_0A24H Default: 00000091H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:21	ADC_SW_REG_31_21[10:0]	RW	Reserved.
20	ADC_SW_REG_20	RW	Enable 120MSPS mode (1.2V logic). Default value is 0.
19	ADC_SW_REG_19	RW	Select comparator fixed clock mode (1.2V logic). Default value is 0.

Address: 000C_0A24H Default: 00000091H			
Bit No.	**Bit Name**	**Attribute**	**Description**
18	ADC_SW_REG_18	RW	Disable reset phase before sampling phase (1.2V logic). Default value is 0.
17	ADC_SW_REG_17	RW	Reserved.
16	ADC_SW_REG_16	RW	Reserved.
15	ADC_SW_REG_15	RW	Power down Q-channel ADC (1.2V logic). Default value is 0.
14	ADC_SW_REG_14	RW	Power down I-channel ADC (1.2V logic). Default value is 0.
13:12	ADC_SW_REG_13_12[1:0]	RW	Control the data clock delay (1.2V logic). Default value is 00B.
11	ADC_SW_REG_11	RW	Invert the data clock phase (1.2V logic). Default value is 0.
10	ADC_SW_REG_10	RW	Bypass the coarse ADC output (1.2V logic). Default value is 0.
9:8	ADC_SW_REG_9_8[1:0]	RW	Control delay time between flash sub-ADC and SAR sub-ADC.
7:5	ADC_SW_REG_7_5[2:0]	RW	Control the internal voltage reference level (1.2V logic). Default value is 100. Vref=0.5+0.2*b2+0.1*b1+0.05*b0
4:2	ADC_SW_REG_4_2[2:0]	RW	Control the internal common-mode level (1.2V logic). Default value is 100. Vcm=0.7+0.2*b2+0.1*b1+0.05*b0
1	ADC_SW_REG_1	RW	Enable internal common-mode level bias for analog input (1.2V logic). Default value is 0.
0	ADC_SW_REG_0	RW	Enable clock input (1.2V logic). Default value is 1.

ATE_ADC_CTRL_REG

Address: 000C_0A34H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:29	RESERVED	RW	Reserved.
28:16	ADC_BUF_LENGTH[12:0]	RW	ADC buffer length. Unit: Word
15:4	RESERVED	RW	Reserved.
3	MADC_I_WR	RW	MADC I channel write selection. 0: Write channel Q. 1: Write channel I.
2	ADC_CONSECUTIVE_READ	RW	ADC consecutive read mode selection. 0: Not consecutive. 1: Consecutive.

Address: 000C_0A34H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
1	ADC_I_READ	RW	ADC channel I read selection. 0: Read channel Q. 1: Read channel I.
0	ADC_EN	RW	ADC test enable. 0: Disable. 1: Enable.

ATE_DAC_CTRL_REG

Address: 000C_0A38H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:29	RESERVED	RW	Reserved.
28:16	DAC_BUF_LENGTH[12:0]	RW	DAC buffer length. Unit: Word
15:2	RESERVED	RW	Reserved.
1	DAC_CONSECUTIVE_READ	RW	DAC consecutive read mode selection. 0: Not consecutive 1: Consecutive
0	DAC_EN	RW	DAC test enable. 0: Disable. 1: Enable.

3.3.3 MADC Control Registers

MADC_CTRL0_REG

Address: 000C_0C00H Default: 00000004H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:4	RESERVED	RW	Reserved.
3	MADC_START	RWC	The bit is used to start to latch MADC data into the corresponding registers. The bit is Self-Cleared.
2	MADC_RSTN	RW	MADC reset bit. 0: Reset. 1: Do not perform reset.

Address: 000C_0C00H Default: 00000004H			
Bit No.	**Bit Name**	**Attribute**	**Description**
1	SDMQ_PD	RW	MADCQ Power Down control. 0: Power on. 1: Power down.
0	SDMI_PD	RW	MADCI Power Down control. 0: Power on. 1: Power down.

MADC_DATA_REG

Address: 000C_0C08H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:28	RESERVED	RW	Reserved.
27:16	MADCQ[11:0]	RW	MADC channel Q data The data is valid when MADC_START returns to 0 after MADC_START is set to 1.
15:12	RESERVED	RW	Reserved.
11:0	MADCI[11:0]	RW	MADC channel I data The data is valid when MADC_START returns to 0 after MADC_START is set to 1.

MADC_IQ_SM_REG

Address: 000C_0C1CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:21	RESERVED	RW	Reserved.
20:16	SETQ_SM[4:0]	R	Reads from MADC_SETQ_SM.
15:5	RESERVED	RW	Reserved.
4:0	SETI_SM[4:0]	R	Reads from MADC_SETI_SM.

DCC_REG

Address: 000C_0C20H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31	RESERVED	RW	Reserved.
30:16	DCCQ[14:0]	R	Latched by MADC_START.

Address: 000C_0C20H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
15	RESERVED	RW	Reserved.
14:0	DCCI[14:0]	R	Latched by MADC_START.

SDMI_REG

Address: 000C_0C24H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	SDMI_REG[14:0]	RW	Reserved.
15	RESERVED	RW	Reserved.
14:0	SDMI_DCC0[14:0]	RW	Reserved.

SDMQ_REG

Address: 000C_0C28H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	SDMI_REG[14:0]	RW	Reserved.
15	RESERVED	RW	Reserved.
14:0	SDMI_DCC0[14:0]	RW	Reserved.

3.3.4 Timer Registers

TIMER1_L (Timer1 Counter Register)

Address: 000C_2000H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	TIM1_L[31:0]	RW	Timer 1 counts up to TIMER1_H, then resets to 0.

TIMER1_H (Timer 1 Cycle Time Setting Register)

Address: 000C_2004H Default: 000FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	TIM1_H[31:0]	RW	Timer 1 cycle time setting.

TIMER1_PRESCALER (Timer 1 Prescaler Registers)

Address: 000C_2008H
Default: 000FFFFFH

Bit No.	Bit Name	Attribute	Description
31:20	RESERVED	RW	Reserved.
19:0	TIM1_PRESCALAR[19:0]	RW	Timer 1 pre-scalar register.

TIMER1_CTRL

Address: 000C_200CH
Default: 00000000H

Bit No.	Bit Name	Attribute	Description
31:3	RESERVED	RW	Reserved.
2	TIMER_EN	RW	Timer 1 enable. 0: Disabled. 1: Enabled.
1	INT_EN	RW	Interrupt enable. 0: Disabled. 1: Enabled.
0	AUTO_RESTART	RW	0: Timer 1 stops when Timer 1 expires. 1: Timer 1 restarts automactically when Timer 1 expires.

TIMER1_STATUS

Address: 000C_2010H
Default: 00000000H

Bit No.	Bit Name	Attribute	Description
31:1	RESERVED	RW	Reserved.
0	INT_SR	RW	Timer 1 interrupt status. Write ‘1’ to clear the interrupt status bit. 0: Timer 1 interrupt de-assertion; 1: Timer 1 interrupt assertion.

TIMER2_L

Address: 000C_2014H
Default: 00000000H

Bit No.	Bit Name	Attribute	Description
31:20	RESERVED	RW	Reserved.
19:0	TIM2_L[19:0]	RW	Timer 2 counts up to TIM2_H, then resets to 0.

TIMER2_H

Address: 000C_2018H Default: 000FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	TIM2_H[19:0]	RW	Timer 2 cycle time setting.

TIMER2_PRESCALAR

Address: 000C_201CH Default: 000FFFFFH			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	TIM2_PRESCALAR[19:0]	RW	Timer 2 prescalar register.

TIMER2_CTRL

Address: 000C_2020H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:3	RESERVED	RW	Reserved.
2	TIMER_EN	RW	Timer 2 enable. 0: Disabled. 1: Enabled.
1	INT_EN	RW	Interrupt enable. 0: Disabled. 1: Enabled.
0	AUTO_RESTART	RW	0: Timer 2 stops when Timer 2 expires. 1: Timer 2 restarts automatically when Timer 2 expires.

TIMER2_STATUS

Address: 000C_2024H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:1	RESERVED	RW	Reserved.
0	INT_SR	RW	Timer 2 interrupt status. Write 1 to clear the status bit. 0: Timer 2 interrupt de-assertion. 1: Timer 2 interrupt assertion.

3.3.5 UART Registers

UART1_STATUS (For UART0 Interface)

Address: 000C_1000H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	UART_DATA_PORT[7:0]	RW	Data port of UART0 interface. Write to this data port for TX and read from this port for RX.
23	UART_RX_DATA_RDY	R	A '1' in this bit means the RX data is ready for being read.
22:0	RESERVED	RW	Reserved.

UART1_CTRL (For UART0 Interface)

Address: 000C_1004H Default: 90001070H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	BAUD_RATE_CNT[15:0]	RW	Baud rate counter for UART0 interface: 9600bps: Baud rate = A2CH (2604) 115200bps: Baud rate = D9H (217)
15	TX_INT_EN	RW	TX interrupt enable. 0: Disable. 1: Enable.
14	RX_INT_EN	RW	RX interrupt enable. 0: Disable. 1: Enable.
13	PARITY_EN	RW	Parity bit enable 0: Disable; 1: Enable.
12	PAROTY_MODE	RW	0: Odd parity; 1: Even parity.
11	STOP_BIT	RW	0: 1 stop bit. 1: 2 stop bits
10	LOOPBACK	RW	1: Internal loop back enabled.
9	RX_PARITY	RW	Current RX byte parity.
8	PARITY_ERR	RW	Parity error.
7	FRAME_ERR	RW	Framing error.

Address: 000C_1004H Default: 90001070H			
Bit No.	**Bit Name**	**Attribute**	**Description**
6:4	INT_RX_THR[2:0]	RW	Defines the threshold for the number of bytes to generate the interrupt. RX will generate an interrupt when the number of RX data bytes are greater than the Rx threshold, or there are RX data and time out is detected.
3	RESERVED	-	Reserved.
2	TX_BUF_EMPTY	R	1: TX buffer is empty.
1	RX_BUF_RDY	R	1: RX buffer is ready to be read.
0	TX_DATA_SENDING	R	TX data is on going.

UART2_STATUS (For UART1 Interface)

Address: 000C_3000H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	UART_DATA_PORT[7:0]	RW	Data port of UART1 interface. Write to this data port for TX, and read from this port for RX.
23	UART_RX_DATA_RDY	R	RX data is ready for being read.
22:0	RESERVED	RW	Reserved.

UART2_CTRL (For UART1 Interface)

Address: 000C_3004H Default: 90001070H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:16	BAUD_RATE_CNT[15:0]	RW	Baud rate counter for UART1 interface: 9600bps: Baud rate = A2CH (2604) 115200bps” Baud rate = D9H (217)
15	TX_INT_EN	RW	TX interrupt enable. 1: Enable
14	RX_INT_EN	RW	RX interrupt enable. 1: Enable
13	PARITY_EN	RW	Parity bit enable. 1: Enable
12	PAROTY_MODE	RW	0: Odd parity 1: Even parity
11	STOP_BIT	RW	0: 1 stop bit 1: 2 stop bits

Address: 000C_3004H Default: 90001070H			
Bit No.	**Bit Name**	**Attribute**	**Description**
10	LOOPBACK	RW	1: Internal loop back enabled
9	RX_PARITY	RW	Current RX byte parity
8	PARITY_ERR	RW	Parity error
7	FRAME_ERR	RW	Framing error
6:4	INT_RX_THR[2:0]	RW	Defines the threshold for the number of bytes to generate the interrupt. RX will generate an interrupt when the number of RX data bytes is greater than the Rx threshold, or there are RX data and time out is detected.
3	RESERVED	-	Reserved.
2	TX_BUF_EMPTY	R	1: TX buffer is empty.
1	RX_BUF_RDY	R	1: RX buffer is ready for being read.
0	TX_DATA_SENDING	R	TX data is on going.

3.3.6 PWM Registers

PWM1_REG (PWM1 Control Register)

Address: 000C_0010H Default: 06000000H			
Note: CH0 for GPIO6; CH1 for GPIO7.			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:30	RESERVED	RW	Reserved.
29:22	PRESCALAR_MAX[7:0]	RW	PWM pre-scalar max. setting
21	CH1_POLARITY	RW	PWM polarity
20	CH0_POLARITY	RW	PWM polarity
19:17	CH1_SWEEP_FREQ[2:0]	RW	PWM sweep frequency
16:14	CH0_SWEEP_FREQ[2:0]	RW	PWM sweep frequency
13:9	CH1_DUTY_CYCLE[4:0]	RW	PWM duty cycle
8:4	CH0_DUTY_CYCLE[4:0]	RW	PWM duty cycle
3	CH1_AUTO_MODE	RW	Auto mode enable. 0: Non-auto mode. 1: Auto mode.
2	CH0_AUTO_MODE	RW	Auto mode 0: Non-auto mode. 1: Auto mode.

Address: 000C_0010H Default: 06000000H			
Note: CH0 for GPIO6; CH1 for GPIO7.			
Bit No.	**Bit Name**	**Attribute**	**Description**
1	CH1_EN	RW	PWM1 enable 0: Disable 1: Enable
0	CH0_EN	RW	PWM0 enable 0: Disable 1: Enable

PWM2_REG (PWM2 Control Register)

Address: 000C_0014H Default: 06000000H			
Note: CH2 for GPIO8; CH3 for GPIO9.			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:30	RESERVED	RW	Reserved.
29:22	PRESCALAR_MAX[7:0]	RW	PWM pre-scalar max. setting
21	CH3_POLARITY	RW	PWM polarity
20	CH2_POLARITY	RW	PWM polarity
19:17	CH3_SWEEP_FREQ[2:0]	RW	PWM sweep frequency
16:14	CH2_SWEEP_FREQ[2:0]	RW	PWM sweep frequency
13:9	CH3_DUTY_CYCLE[4:0]	RW	PWM duty cycle
8:4	CH2_DUTY_CYCLE[4:0]	RW	PWM duty cycle
3	CH3_AUTO_MODE	RW	Auto mode enable. 0: Non-auto mode. 1: Auto mode.
2	CH2_AUTO_MODE	RW	Auto mode enable. 0: Non-auto mode. 1: Auto mode.
1	CH3_EN	RW	PWM3 enable 0: Disable. 1: Enable.
0	CH2_EN	RW	PWM2 enable. 0: Disable. 1: Enable.

3.3.7 SPI Flash Registers

SPI_REG0 (SPI Command Register)

Address: 000C_4000H Default: 00FF1900H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	SFCMD[7:0]	RW	Command issue to SPI flash.
23:20	SFHIGH[3:0]	RW	SPI flash clock high cycles, in unit of hclk.
19:16	SFLOW[3:0]	RW	SPI flash clock low cycles, in unit of hclk.
15:13	RESERVED	RW	Reserved.
12:8	NONACT[4:0]	RW	sfcsn_o must idle for more than NONACT clock period before next activation.
7	RD_TRIG	RW	Trigger transaction for customer command 1: The SPI flash transaction is issued when reading from the SPI read data register. The bit should not be set with WR_TRIG.
6	WR_TRIG	RW	Trigger transaction for customer command 1: The SPI flash transaction is issued when writing to the SPI write command register. The bit should not be set with RD_TRIG.
5:4	DUMMY_CNT[1:0]	RW	Dummy cycle for customer command DUMMY_CNT[1:0] should subtract 1 when ADDR_NEED is not set.
3	ADDR_NEED	RW	1: Send the address for customer command.
2:0	DATA_CNT[2:0]	RW	The number of the data bytes that need to be read or written. The maximum number is 4 for 32-bit AHB bus.

SPI_REG1 (SPI Address Register)

Address: 000C_4004H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	RESERVED	-	Reserved.
23:0	SFADDR[23:0]	RW	Address information used in SPI flash transaction

SPI_REG2 (SPI Write Data Register)

Address: 000C_4008H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	SFWDATA[31:0]	RW	Write data used in SPI flash transaction to this register.

SPI_REG3 (SPI Read Data Register)

Address: 000C_400CH Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	SFRDATA[31:0]	RV	Read the data result in SPI flash transaction from this register.

3.3.8 CPU DMA Registers

CPU_DMA_CHANNEL0_CMD (Command, Length and Status of DMA Channel 0)

Address: 000F_4000H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:17	RESERVED	RW	Reserved
16	DMA_START_0	RW	DMA start command for DMA channel 0. Write 1's to issue a DMA transfer command. The bit is cleared by hardware when DMA transfer is completed or aborted. 0: DMA idle 1: DMA busy

Address: 000F_4000H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
15:0	DMA_LEN_0[15:0]	RW	DMA start command for DMA channel 0. Write 1's to issue a DMA transfer command. The field is cleared by hardware when DMA transfer is completed or aborted. 0: DMA idle 1: DMA busy DMA transfer length for DMA channel 0 0000H: 65536 byte 0001H: 1 bytes 0002H: 2 bytes 0003H: 3 bytes … FFFFH: 65535 bytes

CPU_DMA_CHANNEL0_SRC_ADDR (DMA Source Address - Channel 0)

Address: 000F_4004H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	RESERVED	RW	Reserved.
23:0	DMA_SRC_ADDR_0[23:0]	RW	Source address of DMA channel 0. When SRC_FROM_FLAS_0 is 0's, it indicates the address of external Flash. When SRC_FROM_FLAS_0 is 1's, it indicates the address of internal memory (internal SRAM or CPU memory)

CPU_DMA_CHANNEL0_DST_ADDR (DMA Destination Address - Channel 0)

Address: 000F_4008H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	DMA_DST_ADDR_0[19:0]	RW	Destination address of DMA channel 0.

CPU_DMA_CHANNEL1_CMD (Command, Length and Status of DMA Channel 1)

Address: 000F_4010H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:17	RESERVED	RW	Reserved.
16	DMA_START_1	RW	DMA start command for DMA channel 1. Write 1's to issue a DMA transfer command Cleared by hardwire when DMA transfer is finished or aborted. 0: DMA idle 1: DMA busy
15:0	DMA_LEN_1[15:0]	RW	DMA transfer length for DMA channel 1. 0000H: 65536 byte 0001H: 1 bytes 0002H: 2 bytes 0003H: 3 bytes … FFFFH: 65535 bytes

CPU_DMA_CHANNEL1_SRC_ADDR (DMA Source Address - Channel 1)

Address: 000F_4014H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	RESERVED	RW	Reserved.
23:0	DMA_SRC_ADDR_1[23:0]	RW	Source address of DMA channel 1. When SRC_FROM_FLAS_1 is 0's, it indicates the address of external Flash. When SRC_FROM_FLAS_1 is 1's, it indicates the address of internal memory (internal SRAM or CPU memory)

CPU_DMA_CHANNEL1_DST_ADDR (DMA Destination Address - Channel 1)

Address: 000F_4018H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	RW	Reserved.
19:0	DMA_DST_ADDR_1[19:0]	RW	Destination address of DMA channel 1.

CPU_DMA_CHANNEL2_CMD (Command, Length and Status of DMA Channel 2)

Address: 000F_4020H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:17	RESERVED	RW	Reserved.
16	DMA_START_2	RW	DMA start command for DMA channel 2. Write 1's to issue a DMA transfer command. The bit is cleared by hardware when DMA transfer is completed or aborted. 0: DMA idle 1: DMA busy
15:0	DMA_LEN_2[15:0]	RW	DMA transfer length for DMA channel 2. 0000H: 65536 byte 0001H: 1 bytes 0002H: 2 bytes 0003H: 3 bytes … FFFFH: 65535 bytes

CPU_DMA_CHANNEL2_SRC_ADDR (DMA Source Address - Channel 2)

Address: 000F_4024H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	RESERVED	-	Reserved.
23:0	DMA_SRC_ADDR_2[23:0]	RW	Source address of DMA channel 2. When SRC_FROM_FLAS_2 is 0's, it indicates the address of external Flash. When SRC_FROM_FLAS_2 is 1's, it indicates the address of internal memory (internal SRAM or CPU memory).

CPU_DMA_CHANNEL2_DST_ADDR (DMA Destination Address - Channel 2)

Address: 000F_4028H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	-	Reserved.
19:0	DMA_DST_ADDR_2[19:0]	RW	Destination address of DMA channel 2.

CPU_DMA_CHANNEL3_CMD (Command, Length and Status of DMA Channel 3)

Address: 000F_4030H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:17	RESERVED	RV	Reserved.
16	DMA_START_3	RW	DMA start command for DMA channel 3. Write 1's to issue a DMA transfer command The bit is cleared by hardware when DMA transfer is completed or aborted. 0: DMA idle 1: DMA busy
15:0	DMA_LEN_3[15:0]	RW	DMA transfer length for DMA channel 3. 0000H: 65536 byte 0001H: 1 bytes 0002H: 2 bytes 0003H: 3 bytes … FFFFH: 65535 bytes

CPU_DMA_CHANNEL3_SRC_ADDR (DMA Source Address - Channel 3)

Address: 000F_4034H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:24	RESERVED	-	Reserved.
23:0	DMA_SRC_ADDR_3[23:0]	RW	Source address of DMA channel 3. When SRC_FROM_FLAS_3 is 0's, it indicates the address of external Flash. When SRC_FROM_FLAS_3 is 1's, it indicates the address of internal memory (internal SRAM or CPU memory)

CPU_DMA_CHANNEL3_DST_ADDR (DMA Destination Address - Channel 3)

Address: 000F_4038H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:20	RESERVED	-	Reserved.
19:0	DMA_DST_ADDR_3[19:0]	RW	Destination address of DMA channel 3.

CPU_DMA_INT_STA_MASK (DMA Interrupt Status and Mask)

Address: 000F_403CH
Default: 0002FF00H

Bit No.	Bit Name	Attribute	Description
31:18	RESERVED	RW	Reserved (Dummy cell reserved).
17	AXI_BUS_ERROR_IMSK	RW	AXI Bus Error interrupt mask. 0: Unmask 1: Mask
16	AXI_BUS_ERROR	RWC	AXI Bus Error detection flag. Set by H/W detects AXI Bus Error events, and clear by writing 1's to this bit. AXI Bus Error detection flag. Set by H/W detects AXI Bus Error events, and clear by writing 1's to this bit. 0: No AXI Bus Error 1: AXI Bus Error detected
15	DMA_FAIL_IMSK_3	RW	DMA_FAIL_3 interrupt mask 0: Unmask 1: Mask
14	DMA_FAIL_IMSK_2	RW	DMA_FAIL_2 interrupt mask 0: Unmask 1: Mask
13	DMA_FAIL_IMSK_1	RW	DMA_FAIL_1 interrupt mask 0: Unmask 1: Mask
12	DMA_FAIL_IMSK_0	RW	DMA_FAIL_0 interrupt mask 0: Unmask 1: Mask
11	DMA_FINISH_IMSK_3	RW	DMA_FINISH_3 interrupt mask 0: Unmask 1: Mask
10	DMA_FINISH_IMSK_2	RW	DMA_FINISH_2 interrupt mask 0: Unmask 1: Mask
9	DMA_FINISH_IMSK_1	RW	DMA_FINISH_1 interrupt mask 0: Unmask 1: Mask
8	DMA_FINISH_IMSK_0	RW	DMA_FINISH_0 interrupt mask 0: Unmask 1: Mask

Address: 000F_403CH
Default: 0002FF00H

Bit No.	Bit Name	Attribute	Description
7	DMA_FAIL_3	RWC	DMA failure flag for DMA channel 3 Set by hardware when detecting that the DMA channel 3 command is an exception event. The bit is cleared by writing 1's to it. 0: DMA does not fail; 1: DMA transfer fails.
6	DMA_FAIL_2	RWC	DMA failure flag for DMA channel 2 Set by hardware when detecting that the DMA channel 2 command is an exception event. The bit is cleared by writing 1's to it. 0: DMA does not fail; 1: DMA transfer fails.
5	DMA_FAIL_1	RWC	DMA fail flag for DMA channel 1 Set by hardware when detecting that the DMA channel 1 command is an exception event. The bit is cleared by writing 1's to it. 0: DMA does not fail; 1: DMA transfer fails.
4	DMA_FAIL_0	RWC	DMA fail flag for DMA channel 0 Set by hardware when detecting that the DMA channel 0 command is an exception event. The bit is cleared by writing 1's to it. 1: DMA transfer fails; 0: DMA does not fail.
3	DMA_FINISH_3	RWC	DMA channel 3 finish flag. Set by hardware and cleared by writing 1's to the bit. This is an interrupt source. 0: Not finished yet 1: Finished
2	DMA_FINISH_2	RWC	DMA channel 2 finish flag. Set by hardware and cleared by writing 1's to this bit. This is an interrupt source. 0: Not finished yet 1: Finished

Address: 000F_403CH Default: 0002FF00H			
Bit No.	**Bit Name**	**Attribute**	**Description**
1	DMA_FINISH_1	RWC	DMA channel 1 finish flag. Set by hardware and cleared by writing 1's to the bit. This is an interrupt source. 0: Not finished yet 1: Finished
0	DMA_FINISH_0	RWC	DMA channel 0 finish flag. Set by hardware and cleared by writing 1's to the bit. This is an interrupt source. 0: Not finished yet 1: Finished

CPU_DMA_BOOST_SET (DMA Boost Setting Register)

Address: 000F_4040H Default: 00000200H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:10	RESERVED	-	Reserved.
9	ROM_INSERT_WAIT	RW	CPU ROM insert wait state 0: ROM accessing has no wait cycle, i.e. one cycle to access ROM. 1: ROM accessing has 1 wait cycle, i.e. two cycles to access ROM.
8:7	SRC_FLASH_DMA_SEL[1:0]	RW	Source from Flash DMA channel selector. When SRC_FROM_FLASH is set, it is used for selecting one of DMA channel to perform move data from external flash.
6	SRC_FROM_FLASH	RW	DMA channel 0 source from external flash. 0: Source from internal memory 1: Source from flash Only one DMA channel can be selected to move data from external flash. SRC_FLASH_DMA_SEL[2:0] is used for selecting the DMA channel used to move data from external flash.

Address: 000F_4040H Default: 00000200H			
Bit No.	**Bit Name**	**Attribute**	**Description**
5:4	SM2_DMA_BOOST[1:0]	RW	System SRAM2 DMA boost setting. This is a configuration register for boosting the access of DMA and AXI slave to local memories. The accessing order is as shown below. 00: CPU code, CPU data, DMA/AXIS,… 01: CPU code, CPU data, DMA/AXIS, DMA/AXIS 10: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS 11: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS, DMA/AXIS
3:2	SM1_DMA_BOOST[1:0]	RW	System SRAM 1 DMA boost setting. This is a configuration register for boosting the access of DMA and AXI slave to local memories. The accessing order is as shown below. 00: CPU code, CPU data, DMA/AXIS,… 01: CPU code, CPU data, DMA/AXIS, DMA/AXIS 10: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS 11: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS, DMA/AXIS
1:0	LM_DMA_BOOST[1:0]	RW	Local memory DMA boost setting. This is a configuration register for boosting the access of DMA and AXI slave to local memories. The accessing order is as shown below. 00: CPU code, CPU data, DMA/AXIS,… 01: CPU code, CPU data, DMA/AXIS, DMA/AXIS 10: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS 11: CPU code, CPU data, DMA/AXIS, DMA/AXIS, DMA/AXIS, DMA/AXIS

CPU_AXI_ERR_ADDR (AXI Bus Error Address)

Address: 000F_4044H Default: 00000000H			
Bit No.	**Bit Name**	**Attribute**	**Description**
31:0	AXI_ERR_ADDR[31:0]	RO	Address of AXI Bus Error. When detecting an AXI bus error, H/W records the address of memory accessing which causes the AXI Bus Error.

CPU_AXI_ERR_INFO (AXI Bus Error Information)

Address: 000F_4048H
Default: 00000000H

Bit No.	Bit Name	Attribute	Description
31:6	RESERVED	-	Reserved.
5	AXI_ERR_RW	RO	Read or write command of AXI Bus Error event. When detecting AXI Bus Error, H/W records the AXI bus command type. 0: Read 1: Write
4:2	AXI_ERR_MST[2:0]	RO	Master of AXI Bus Error event. When detecting AXI Bus Error, H/W records the master that the AXI bus command is issued from. 000: Reserved 001: Reserved 010: WIFI I1 011: WIFI I2 100: WIFI I3 101: WIFI I4 110: WIFI I5
1:0	AXI_ERR_DEV[1:0]	RO	Device of AXI Bus Error event. When detecting AXI Bus Error, H/W records the device that AXI bus command is issued to. 00: CPU memory or reserved region 01: System SRAM 1 10: System SRAM 2

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings[1]

Symbol	Parameter	Rating		Unit
		Min.	Max.	
VDDA33	3.3V Power Supply for Analog	-0.3	3.6	V
VDD33	3.3V Power Supply for Digital I/Os	-0.3	3.6	V
VDD12	1.2V Power Supply for Digital Core	-0.3	1.5	V
V_{IN}	Voltage on Input Pins	-0.5	VDD33+0.5	V
T_{STG}	Storage Temperature	-40	+125	°C
V_{ESD}	ESD Protection (HBM)	-	TBD	V

1. Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to conditions beyond the absolute maximum ratings may affect the life and reliability of the device.

4.2 Recommended Operating Conditions

Table 7. Recommended Operating Conditions[1]

Symbol	Parameters	Min.	Typ.	Max.	Unit
VDDA33	Analog Part Supply Voltage	2.97	3.3	3.6	V
VDD33	Digital Part DC Supply Voltage for Digital I/O	2.97	3.3	3.6	V
VDD12	Digital Part DC Supply Voltage for Digital Core	1.14	1.2	1.26	V
T_A	Operating Ambient Temperature	-10	-	70	°C

1. Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.

4.3 DC Electrical Characteristics

Table 8. DC Electrical Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage (for LVTTL)	-0.28		0.6	V
V_{IH}	High Level Input Voltage (for LVTTL)	2.0		3.6	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage (for LVTTL)	0.68		1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage (for LVTTL)	1.36		1.7	V
V_{OL}	Low Level Output Voltage (|OL| = 1.6~14mA)	-0.28		0.4	V
V_{OH}	High Level Output Voltage (|OH| = 1.6~14mA)	2.4		VDD33+0.33	V

4.4 Current Consumption

Table 9. Current Consumption

Symbol	Condition	Min.	Typ.	Max.	Unit
I_{total}	Sleep mode		TBD		mA
	Rx Active, HT40, MCS7		TBD		mA
	RX Power saving, DTIM=1		TBD		mA
	RX Listen		TBD		mA
	TX HT40, MCS7 @13dBm		TBD		mA
	TX CCK, 11Mbps @19dBm		TBD		mA

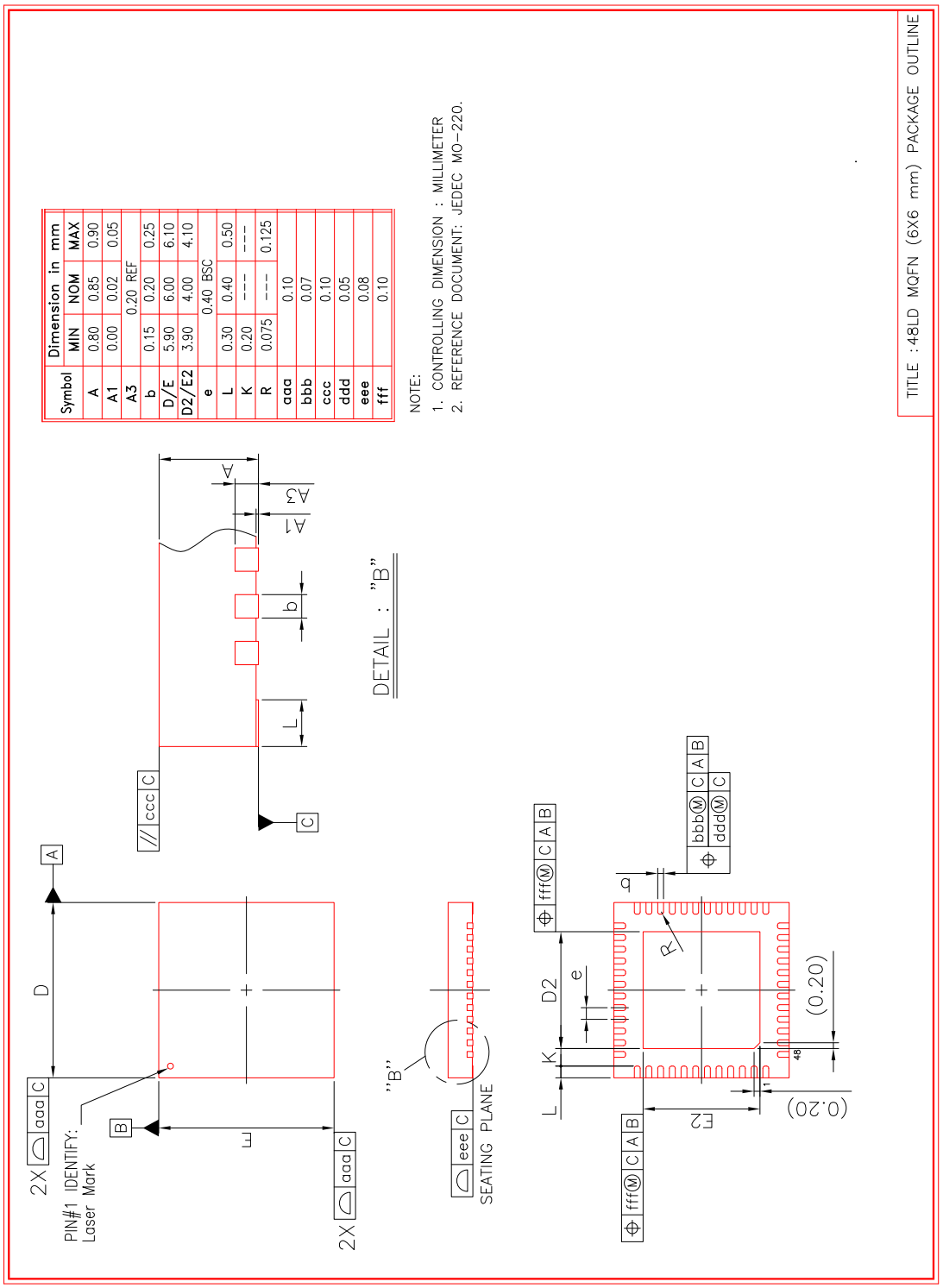
4.5 mADC Performance

Table 10. mADC Performance

Symbol	Condition	Min.	Typ.	Max.	Unit
N	Resolution	-	12	-	Bit
BW	Input Signal Bandwidth	-	100	-	kHz
V_{PP}	Input Swing.	-	-	3.3	V
V_{IN}	Input Voltage.	-	-	3.3	V
R_{IN}	Input Impedance: Unselected channel Selected channel	-	10k	-	Ohm
DNL	Differential Non-linearity without dithering and averaging	-	-	±2	LSB
INL	Integral Non-linearity without dithering and averaging	-	-	±4	LSB
SNR	Signal to Noise Ratio	-	69	-	dB

5 Mechanical Package Data

Figure 3. QFN48 Package Outline



Contact Information

Montage Technology (Shanghai) Co., Ltd.

Address: 6/F, Block A, Technology Building, 900 Yishan Road, Shanghai 200233, China
Phone: +86-21-6128-5678
Fax: +86-21-5426-3132
E-mail: infosh@montage-tech.com
Website: www.montage-tech.com

Montage Technology, Inc.

Address: 101 Metro Drive, Suite 500, San Jose, CA 95110, USA
Phone: +1-408-982-2788
Fax: +1-408-982-2789
E-mail: infosv@montage-tech.com
Website: www.montage-tech.com

Montage Sales Contact in Korea

Address: Suite 604, 6th Fl., B-dong, Woolim Lions Valley 5 Cha, Galmachi-ro 302, Jungwon-gu, Seongnam-si, Gyeonggi-do, 462-739 Korea
Phone: +82-70-8247-4520
E-mail: infosk@montage-tech.com
Website: www.montage-tech.com