Modeling the Impact of a Non-Ohmic Contact on the Delay of Complementary OTFT Inverters

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***Abstract*—To be commercially successful, printed organic electronics need to include minimal signal processing abilities. Rudimentary intelligence relies on sufficiently fast digital circuits based on thin-film transistors (TFTs). A key material parameter for high-frequency operation is the charge carrier mobility. However, organic semiconductors frequently already surpass the mobility of amorphous silicon. Thus, development efforts recently shifted towards the reduction of the contact resistance to further increase the operating frequency. Contact resistance values for organic TFTs are orders of magnitude higher than for silicon technologies and critically limit the TFT current drive. Probably even more important, the charge injection across an organic metal-to-semiconductor interface shows a non-ohmic bias dependence. In the present work, we estimate the deteriorative effect of non-ohmic contacts on the delay of complementary inverters at a given current drive. Moreover, we advocate the use of table circuit models in the absence of physical compact models and related extraction strategies for bias-dependent contact resistances.**

***Index Terms*—Printed electronics, OTFT, table model, complementary inverter.**

I. Introduction

Printed organic electronics (POE) is considered a key technology for enabling the Internet of Things [1], [2]. To live up to the high expectations, POE needs to fulfill its promise to deliver anywhere and on demand low-cost and green electronic circuits on mechanically flexible substrates. However, the challenges are formidable. State-of-the-art circuits fabricated with fully additive processes still show very poor performance. Printed digital circuits are slow, require large supply voltages and suffer from substantial performance variations. For example, the five-stage ring oscillator (RO) described in [3] operates at a frequency of $f_{\mathrm{osc}} = 134\,\mathrm{Hz}$ and a supply voltage of $V_{\mathrm{sup}} = 100\,\mathrm{V}$. The maximum inverter gain across all stages of the RO varies by nearly 10%, a consequence of printing all transistor parts, i.e., the gate, source and drain contacts with a channel length of $L_{\mathrm{ch}} = 70\,\mu\mathrm{m}$ as well as the gate dielectric.

An important performance deteriorator is the contact resistance of the metal-to-semiconductor interface [4]–[6]. Over the past decade the contact resistance r_{c} has been improved and the lowest achievable values dropped by four orders of magnitude to tens of $\Omega\,\mathrm{cm}$ (resistance normalized by multiplying by the contact width). Nevertheless, r_{c} remains at least hundred times larger than typical values for advanced silicon based technologies. A low r_{c} and short L_{ch} are required to reach GHz operating frequencies [7]. Recently, a record $f_{\mathrm{osc}} = 329\,\mathrm{kHz}$ has been reported for an eleven-stage RO powered by $V_{\mathrm{sup}} = 3.7\,\mathrm{V}$ and fabricated on a flexible substrate [8]. The employed unipolar transistor technology relies on high temperature processes and defined the source and drain contacts with $L_{\mathrm{ch}} = 1\,\mu\mathrm{m}$ via metal vapor deposition through a silicon stencil mask and the dielectric via plasma oxidation of the gate metal.

In the presence of a contact resistance, an abruptly rising transistor current is impeded since r_{c} limits the increase of the internal drain-source voltage, which can be modeled as reduction of the effective mobility [7]. The non-linear impact ceases in saturation when the transistor operates as constant current source. Therefore, a sufficient high r_{c} results in an S-shape of the transistor's output current-voltage curve in the so-called linear regime [4]. An additional nonlinearity is introduced if r_{c} decreases with an increased voltage drop across the source-to-semiconductor interface. Such a dependence can arise from the charge injection across a Schottky barrier via thermionic emission or tunneling [9]. At a given gate bias the interfacial field will increase with the drain voltage. A pronounced nonlinear output curve at low drain bias is, thus, often taken as an indicator of a non-ohmic contact resistance.

Although r_{c} has been significantly improved, true ohmic charge injection may be never achieved for organic thin-film transistor (OTFT) technologies. In the present work we therefore simulate the impact of an S-shaped output curve on the rise (fall) time of a complementary inverter based on hypothetical symmetric n- and p-type OTFTs, which is a basic building block of ROs and other digital circuits. We hereby touch also on an additional challenge of the POE supply chain, the availability of process development kits (PDKs). A PDK is an essential prerequisite for electronic design automation of digital circuits. In the case of POE, an advanced PDK should also enable yield and ageing predictions, e.g., under repeated bending and stretching. For the present study hundreds of different circuit model parameter sets are required, reflecting the increased variability of POE technologies. Moreover, no circuit model is currently available that includes a bias dependent contact resistance. To circumvent both challenges, the absence of an appropriate circuit model and the repeated complex parameter extraction in the presence of r_{c} [10], we

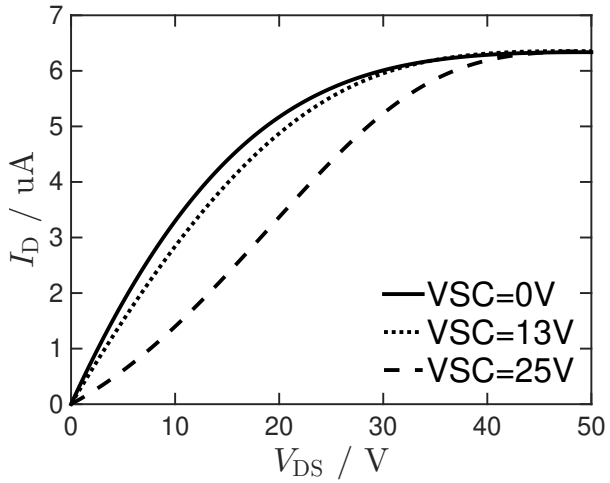

Fig. 1. Output curve with ohmic ($V_{\rm eff} = 0\,{\rm V}$) and non-ohmic ($V_{\rm eff} > 0\,{\rm V}$) contacts.

rely on table models and describe their use.

II. Modeling Approach

A. Phenomenological Model for Non-Ohmic Contacts

For the present study, first appropriate computational data sets needed to be generated that phenomenologically describe OTFT output curves impacted by a contact resistance dependent on the DC working point. A commonly used smoothing function describing the transition between the transistor's linear and saturation operation region is a hyperbolic tangent [11]. An S-shaped output curve can be obtained from any calibrated compact model employing a hyperbolic tangent function by substituting:

$$\tanh\left(\frac{V_{\rm DS}}{V_{\rm G,eff}}\right) \longrightarrow \tanh\left(\frac{v_{\rm scal}[V_{\rm DS} - V_{\rm sc}]}{V_{\rm G,eff}}\right) \qquad (1)$$

A similar modification can be applied also to different transition functions. Here, $V_{\rm DS}$ is the internal drain-source voltage and $V_{\rm G,eff}$ the characteristic voltage for the transition set by the gate bias. Two phenomenological parameters, $V_{\rm sc}$ and $v_{\rm scal}$, determine the voltage dependence of $r_{\rm c}$. The parameter $V_{\rm sc}$ sets the scale for the non-ohmic behavior, i.e., for $V_{\rm DS} > V_{\rm sc}$ the contact resistances approaches its bias-independent limit. A large $v_{\rm scal}$ implies a larger change of r_c from low to high drain voltage.

In the present work, we are interested in analyzing the impact of the bias dependence of $r_{\rm c}$ and not its magnitude on the delay of digital circuit components. Thus, the maximum drive current $I_{\rm D}(V_{\rm DS} = V_{\rm sup})$ shall not change, i.e., $v_{\rm scal} = 1/(1 - V_{\rm sc}/V_{\rm sup})$. An example is shown in Fig. 1. With increasing $V_{\rm sc}$ and $v_{\rm scal}$ the bias dependence of $r_{\rm c}$ and the S-shape behavior of the output curves becomes more pronounced. However, as can be seen, a non-ohmic contact does not necessarily leads to a clearly visible non-linearity although $r_{\rm c}$ is increased at low drain voltages.

TABLE I
OTFT TECHNOLOGIES.

	Tech1	Tech2	Tech3
Geometry	TCBG [12]	BCTG [13]	BCTG [13]
	$W = 0.1\,{\rm cm}$	$W = 0.1\,{\rm cm}$	$W = 0.1115\,{\rm cm}$
	$L_{\rm ch} = 40\,\mu{\rm m}$	$L_{\rm ch} = 70\,\mu{\rm m}$	$L_{\rm ch} = 8.1\,\mu{\rm m}$
Channel	Pentacene	C16IDT-BT	FlexOS™
Gate	ITO/PET substrate	Al	Au
Source/Drain	Au evaporation	Ag	Au
Extracted $r_{\rm c}$	$50\,{\rm k\Omega\,cm}$	$24\,{\rm k\Omega\,cm}$	$349\,\Omega\,{\rm cm}$

To generate the data sets, we use the OTFT technologies with ohmic contacts described in [12] and [13] and summarized in Tab. I. The measured current-voltage characteristics of the three representative technologies were analyzed by the organic virtual-source emission-diffusion (OVSED) model introduced in [14]. The extracted ohmic contact resistance values are also listed in Tab. I. Further details are given in [14]. The OVSED model employs a hyperbolic tangent to model the linear-to-saturation transition. The transition function has been substituted according to the rule (1). Then, $v_{\rm scal}$ and $V_{\rm sc}$ are varied to generate twenty data sets for each OTFT technology. In the following, these computational data sets are treated as "experimental" data to demonstrate the usefulness of table based circuit models when analyzing variability in emergent electronic technologies.

B. Table Circuit Model

A table model for circuit simulations consists of the device characteristics tables and the use of some appropriate numerical techniques to obtain device operating point values from the tables during the simulation process. The table model must be compatible with the numerical methods such that the table preserve the monotonicity and shape of the measured device characteristics. Table models are considered to be faster than analytical models of similar conditions; the models are highly accurate and device independent and they expedite simulations because they are based directly on the measured data. More care should be taken while extracting data because the model can give unexpected results when operated out of the specified range. In our paper we use two-dimensional (2D) tables with a fixed reference source voltage for reproducing the device characteristics, i.e., the 2D model uses data tables with grids for the drain and gate voltage. The voltage-current characteristics are saved in the model table as a single file. We have generated 20 to 30 table models for reproducing the device characteristics for different OTFT technologies and varying degree of non-linear $r_{\rm c}$. For p-type and n-type models separate table models were generated to reproduce the device characteristics. Care should be taken while matching the grid variables in the tables to the OTFT terminals for p- and n-type transistors. Fig. 2 shows the output characteristics of three different OTFT technologies with ohmic and non-ohmic contacts. The output characteristics with ohmic contacts have a

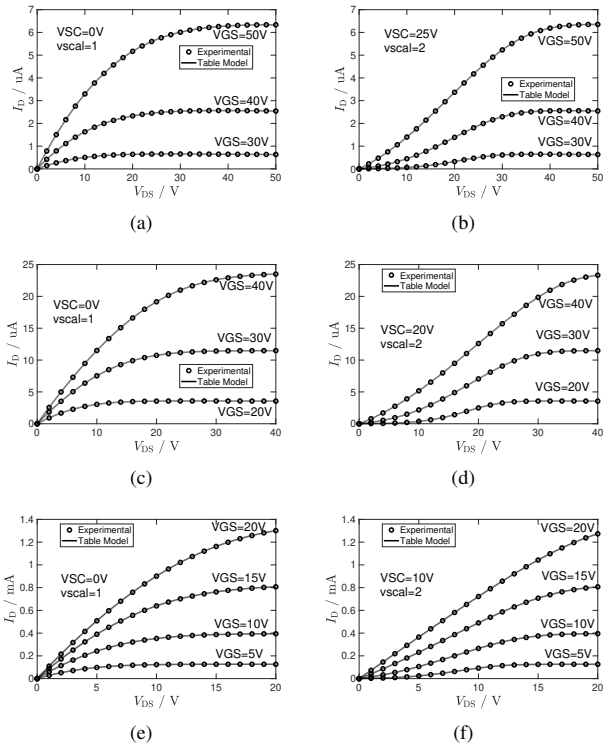

Fig. 2. Output voltage of a complementary inverter (arbitrary load) of different OTFT technologies (rows) with ohmic (left column) and non-ohmic contacts (right column).

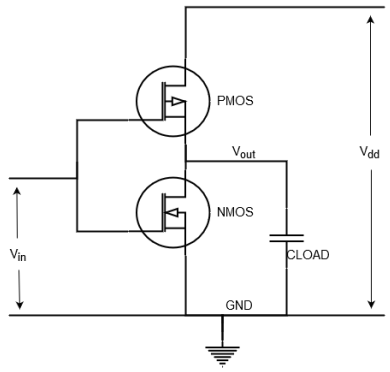

Fig. 3. Schematic of a complementary inverter with a capacitive load

good agreement between the experimental data and the table model. Similarly, the output characteristics with non-ohmic contacts have a good agreement between the experimental data and the table model.

C. Inverter simulations

We have studied the behaviour of an complementary inverter circuit for three different OTFT technologies as shown in Fig. 3. We have taken arbitrary load values for the three different technologies. The supply voltage for the inverter circuit is set individually according to the OTFT technology under consideration. The table model netlist commands for the complementary inverter circuit are as shown below. We have created separated netlist entries for p- and n-type transistors using the table models as can be seen. It is important in the table model netlist entry to indicate the node variables carefully for the n- and p-type models, which are called here `nmostabmod` and `pmostabmod`, respectively. The complementary inverter circuit can be extended to an ring oscillator circuit.

```
.model nmostabmod table2d (offset=0.0
gain=1 order=3 file="s1modeln.txt")
.model pmostabmod table2d (offset=0.0
gain=1 order=3 file="s1modelp.txt")
atab0 vout vin %id(vss vout) pmostabmod
atab1 vout vin %id(vout 0) nmostabmod
```

III. Results

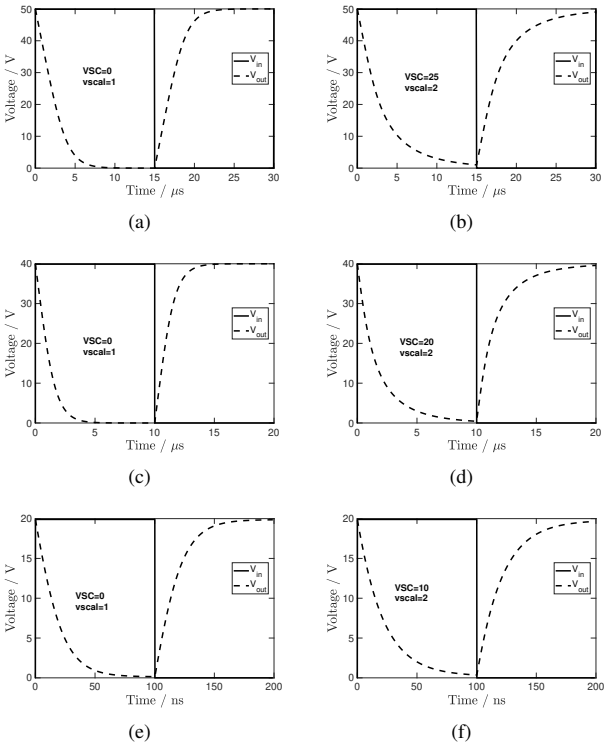

Fig. 4. Transient response of a complementary inverter (arbitrary load) of different OTFT technologies (rows) with ohmic (left column) and non-ohmic contacts (right column).

Fig. 4 shows the transient response of arbitrarily-loaded complementary inverters based on different OTFT technologies featuring ohmic as well as non-ohmic contacts. It can be observed that the rise time in the case of non-ohmic contacts is longer than the one obtained in the case of ohmic contacts for all the considered different OTFT technologies. Likewise, the time required to reach 90% of the input voltage is longer for ohmic compared to non-ohmic OTFTs independent of the process technology.

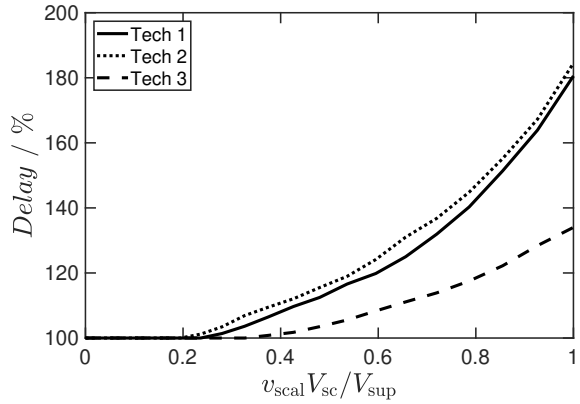

Fig. 5. Relative increase of the fall/rise time of complementary inverters based on different OTFT technologies with increasingly non-ohmic contacts. As measure of the non-linearity the parameter $v_{\mathrm{scal}} V_{\mathrm{sc}}/V_{\mathrm{sup}}$ has been used.

Fig. 5 shows the resulting relative increase of the fall/rise time of complementary inverters with an increasingly non-ohmic contact resistance. The non-linearity of r_{c} has a significant negative impact on the fall/rise times, which can be clearly seen for all the three considered OTFT technologies. The fall/rise time can increase to up to 190% under the influence of non-ohmic contacts.

IV. Conclusions

Charge injection across an organic metal-to-semiconductor interface is dominated by thermionic and tunneling processes. Contrary to silicon-based technologies, the modulation of the injection barrier with the DC bias point is difficult to control. Even interfacial layers specifically introduced to improve the charge injection may add additional complications like increased charge trap density and may not lead to ohmic contacts with a bias independent value r_{c}. Thus, it is interesting to ask how a non-ohmic contact resistance that increases with decreasing source-to-drain electrical field slows down digital circuits.

We estimated that the fall/rise time of complementary inverters increases by up to 190% in the presence of non-ohmic contacts. The estimation was based on the generic observation that the linear-to-saturation transition of a thin-film transistor is shifted to higher drain voltages for non-ohmic contacts. We argued that the phenomenological description of such a shift may be included in existing compact models by adding only a few additional parameters contrary to the number of required parameters when physically modeling the bias dependence of r_{c}. The obtained increase in the inverter delay is only caused by the non-linearity introduced by a bias-dependent r_{c} and not by a reduction of the current drive. The non-ohmic slowing down is obtained for different high-field resistance values. However, a low r_{c} at high interfacial fields also decreases the deteriorative effect of a non-ohmic contact.

Finally, we demonstrated the use of table models for circuits based on devices with complex physics like organic thin-film transistors with non-ohmic contacts. For such devices, reliable physical models and parameter extraction strategies are often absent and table models represent a true alternative.

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