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Prefetcher's Impact Over Parallel Architecture Simulation

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Summary

In computer architecture research, the use of simulators is predominant. There are diverse approaches and implementations of modern simulators. However, validation studies lack a detailed analysis of parallel behavior in high-performance architecture simulators. We could observe that, due to the lack of prefetching simulation, the memory hierarchy statistics are inaccurate. Thereby, this study analyzes the impact of the prefetcher in the parallel simulation methodology used by ZSim.

KEYWORDS:
computer architecture, parallel architecture, prefetcher, architecture simulation,

1 | INTRODUCTION

2 | THOUGHTS

We already observed the impact in the simulation accuracy when the prefetcher is not modeled by the simulator. Zsim registers a high number of LLC accesses that would be prevented by the prefetcher, similar to the results observed in the real execution with the prefetcher disabled. However, in a simulator that do model the prefetcher, how accurate its implementation is? In order to be able to determine this accuracy, we must at first understand how we can quantify it. Accuracy is defined by which parameters? Number of LLC accesses? And what about the cache pollution? And the usefulness of the prefetched lines?

Since both L1 and L2 data prefetchers impact in the number of requests that reach the uncore, they were both disabled for the real executions without the prefetcher.

Something that we must ensure is to test with applications with a bigger input size and different communication patterns (preferably more heterogeneous applications). Shall we consider different prefetchers in the real executions? For example, different prefetchers in different cache levels? If so, is that an option also in the simulators? If it is, then shall we perform a comparison among the accuracy of the different possible configurations?

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FIGURE 1 This is the sample figure caption

TABLE 1 This is the sample table caption

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3 | FOURTH PROBLEM

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